

# NVD5890N

## Power MOSFET

40 V, 123 A, Single N-Channel DPAK

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- MSL 1/260°C
- AEC Q101 Qualified and PPAP Capable
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Motor Drivers
- Pump Drivers for Automotive Braking, Steering and Other High Current Systems

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter                                                                                                                                                    |                      |                       | Symbol                            | Value      | Unit |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----------------------|-----------------------------------|------------|------|
| Drain-to-Source Voltage                                                                                                                                      |                      |                       | V <sub>DSS</sub>                  | 40         | V    |
| Gate-to-Source Voltage                                                                                                                                       |                      |                       | V <sub>GS</sub>                   | ± 20       | V    |
| Continuous Drain Current (R <sub>θJC</sub> )                                                                                                                 | Steady State         | T <sub>C</sub> = 25°C | I <sub>D</sub>                    | 123        | A    |
|                                                                                                                                                              |                      | T <sub>C</sub> = 85°C |                                   | 95         |      |
| Power Dissipation (R <sub>θJC</sub> )                                                                                                                        |                      | T <sub>C</sub> = 25°C | P <sub>D</sub>                    | 107        | W    |
| Continuous Drain Current (R <sub>θJA</sub> ) (Note 1)                                                                                                        |                      | T <sub>A</sub> = 25°C | I <sub>D</sub>                    | 24         | A    |
|                                                                                                                                                              |                      | T <sub>A</sub> = 85°C |                                   | 18.5       |      |
| Power Dissipation (R <sub>θJA</sub> ) (Note 1)                                                                                                               |                      | T <sub>A</sub> = 25°C | P <sub>D</sub>                    | 4.0        | W    |
| Pulsed Drain Current                                                                                                                                         | t <sub>p</sub> =10μs | T <sub>A</sub> = 25°C | I <sub>DM</sub>                   | 400        | A    |
| Current Limited by Package                                                                                                                                   |                      | T <sub>A</sub> = 25°C | I <sub>DmaxPkg</sub>              | 100        | A    |
| Operating Junction and Storage Temperature                                                                                                                   |                      |                       | T <sub>J</sub> , T <sub>stg</sub> | –55 to 175 | °C   |
| Source Current (Body Diode)                                                                                                                                  |                      |                       | I <sub>S</sub>                    | 100        | A    |
| Drain to Source dV/dt                                                                                                                                        |                      |                       | dV/dt                             | 6.0        | V/ns |
| Single Pulse Drain-to-Source Avalanche Energy (V <sub>DD</sub> = 32 V, V <sub>GS</sub> = 10 V, L = 0.3 mH, I <sub>L(pk)</sub> = 40 A, R <sub>G</sub> = 25 Ω) |                      |                       | E <sub>AS</sub>                   | 240        | mJ   |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s)                                                                                            |                      |                       | T <sub>L</sub>                    | 260        | °C   |

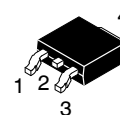
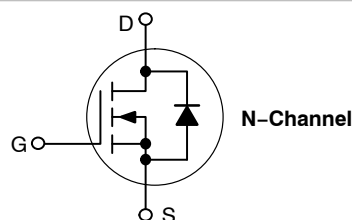
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



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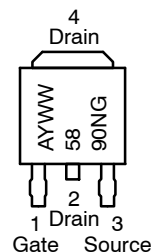
[www.onsemi.com](http://www.onsemi.com)

| $V_{(BR)DSS}$ | $R_{DS(on)}$          | $I_D$ |
|---------------|-----------------------|-------|
| 40 V          | 3.7 m $\Omega$ @ 10 V | 123 A |



CASE 369C  
DPAK  
(Bent Lead)  
STYLE 2

### MARKING DIAGRAMS & PIN ASSIGNMENT



A = Assembly Location\*  
Y = Year  
WW = Work Week  
5890N = Device Code  
G = Pb-Free Package

\* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejector pin), the front side assembly code may be blank.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

**THERMAL RESISTANCE MAXIMUM RATINGS**

| Parameter                                   | Symbol          | Value | Unit |
|---------------------------------------------|-----------------|-------|------|
| Junction-to-Case (Drain)                    | $R_{\theta JC}$ | 1.4   | °C/W |
| Junction-to-Ambient - Steady State (Note 1) | $R_{\theta JA}$ | 37    |      |
| Junction-to-Ambient - Steady State (Note 2) | $R_{\theta JA}$ | 76    |      |

1. Surface-mounted on FR4 board using 650 mm<sup>2</sup> pad size, 2 oz Cu.
2. Surface-mounted on FR4 board using 36 mm<sup>2</sup> pad size.

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

**OFF CHARACTERISTICS**

|                                                           |                   |                                                     |                           |    |           |               |
|-----------------------------------------------------------|-------------------|-----------------------------------------------------|---------------------------|----|-----------|---------------|
| Drain-to-Source Breakdown Voltage                         | $V_{(BR)DSS}$     | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | 40                        |    |           | V             |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ |                                                     |                           | 40 |           | mV/°C         |
| Zero Gate Voltage Drain Current                           | $I_{DSS}$         | $V_{GS} = 0\text{ V},$<br>$V_{DS} = 40\text{ V}$    | $T_J = 25^\circ\text{C}$  |    | 1.0       | $\mu\text{A}$ |
|                                                           |                   |                                                     | $T_J = 150^\circ\text{C}$ |    | 100       |               |
| Gate-to-Source Leakage Current                            | $I_{GSS}$         | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$     |                           |    | $\pm 100$ | nA            |

**ON CHARACTERISTICS** (Note 3)

|                                             |                  |                                                 |     |      |     |            |
|---------------------------------------------|------------------|-------------------------------------------------|-----|------|-----|------------|
| Gate Threshold Voltage                      | $V_{GS(TH)}$     | $V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$ | 1.5 |      | 3.5 | V          |
| Negative Threshold Temperature Co-efficient | $V_{GS(TH)}/T_J$ |                                                 |     | 7.4  |     | mV/°C      |
| Drain-to-Source On Resistance               | $R_{DS(on)}$     | $V_{GS} = 10\text{ V}, I_D = 50\text{ A}$       |     | 2.9  | 3.7 | m $\Omega$ |
| Forward Transconductance                    | gFS              | $V_{DS} = 15\text{ V}, I_D = 15\text{ A}$       |     | 16.8 |     | S          |

**CHARGES AND CAPACITANCES**

|                              |              |                                                                      |  |      |     |    |
|------------------------------|--------------|----------------------------------------------------------------------|--|------|-----|----|
| Input Capacitance            | $C_{iss}$    | $V_{GS} = 0\text{ V}, f = 1.0\text{ MHz},$<br>$V_{DS} = 12\text{ V}$ |  | 4975 |     | pF |
| Output Capacitance           | $C_{oss}$    |                                                                      |  | 785  |     |    |
| Reverse Transfer Capacitance | $C_{rss}$    |                                                                      |  | 490  |     |    |
| Input Capacitance            | $C_{iss}$    | $V_{GS} = 0\text{ V}, f = 1.0\text{ MHz},$<br>$V_{DS} = 25\text{ V}$ |  | 4760 |     | pF |
| Output Capacitance           | $C_{oss}$    |                                                                      |  | 580  |     |    |
| Reverse Transfer Capacitance | $C_{rss}$    |                                                                      |  | 385  |     |    |
| Total Gate Charge            | $Q_{G(TOT)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$<br>$I_D = 50\text{ A}$ |  | 74   | 100 | nC |
| Threshold Gate Charge        | $Q_{G(TH)}$  |                                                                      |  | 5.0  |     |    |
| Gate-to-Source Charge        | $Q_{GS}$     |                                                                      |  | 17   |     |    |
| Gate-to-Drain Charge         | $Q_{GD}$     |                                                                      |  | 16   |     |    |

**SWITCHING CHARACTERISTICS** (Note 4)

|                     |              |                                                                                               |  |     |  |    |
|---------------------|--------------|-----------------------------------------------------------------------------------------------|--|-----|--|----|
| Turn-On Delay Time  | $t_{d(on)}$  | $V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V},$<br>$I_D = 50\text{ A}, R_G = 2.0\text{ }\Omega$ |  | 14  |  | ns |
| Rise Time           | $t_r$        |                                                                                               |  | 55  |  |    |
| Turn-Off Delay Time | $t_{d(off)}$ |                                                                                               |  | 35  |  |    |
| Fall Time           | $t_f$        |                                                                                               |  | 7.0 |  |    |

3. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Switching characteristics are independent of operating junction temperatures.

# NVD5890N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

### DRAIN-SOURCE DIODE CHARACTERISTICS

|                         |                 |                                                                                 |                       |  |     |     |    |
|-------------------------|-----------------|---------------------------------------------------------------------------------|-----------------------|--|-----|-----|----|
| Forward Diode Voltage   | V <sub>SD</sub> | V <sub>GS</sub> = 0 V,<br>I <sub>S</sub> = 50 A                                 | T <sub>J</sub> = 25°C |  | 0.9 | 1.2 | V  |
|                         |                 | V <sub>GS</sub> = 0 V,<br>I <sub>S</sub> = 20 A                                 | T <sub>J</sub> = 25°C |  | 0.8 | 1.0 |    |
| Reverse Recovery Time   | t <sub>RR</sub> | V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs,<br>I <sub>S</sub> = 50 A |                       |  | 35  |     | ns |
| Charge Time             | t <sub>a</sub>  |                                                                                 |                       |  | 20  |     |    |
| Discharge Time          | t <sub>b</sub>  |                                                                                 |                       |  | 15  |     |    |
| Reverse Recovery Charge | Q <sub>RR</sub> |                                                                                 |                       |  | 40  |     | nC |

TYPICAL PERFORMANCE CURVES

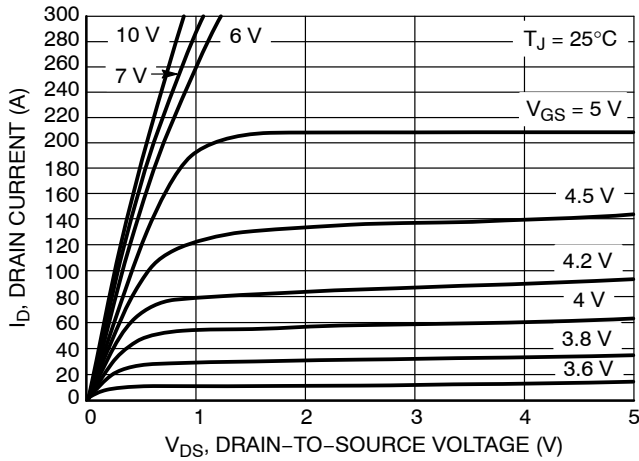


Figure 1. On-Region Characteristics

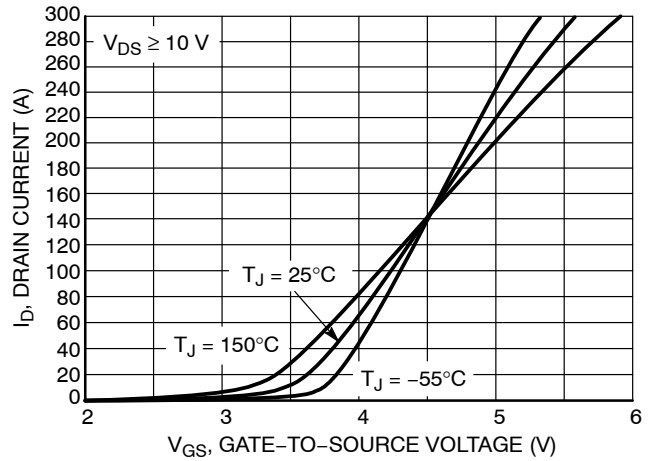


Figure 2. Transfer Characteristics

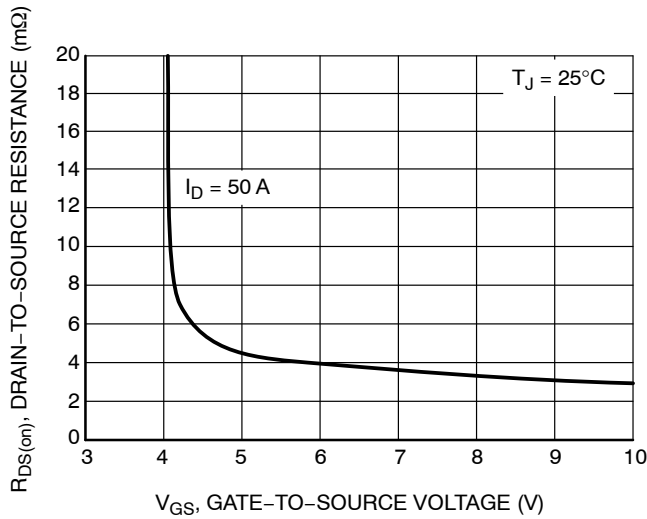


Figure 3. On-Resistance vs. Drain Current

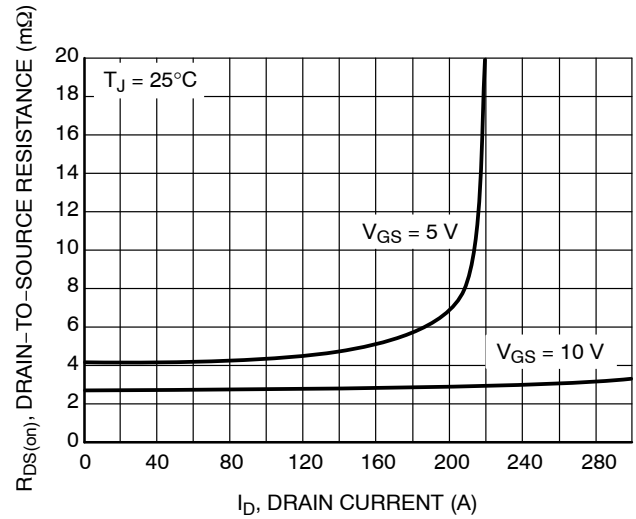


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

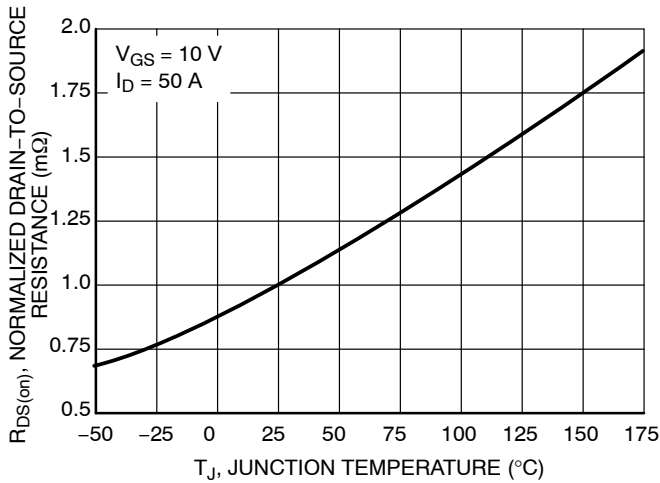


Figure 5. On-Resistance Variation with Temperature

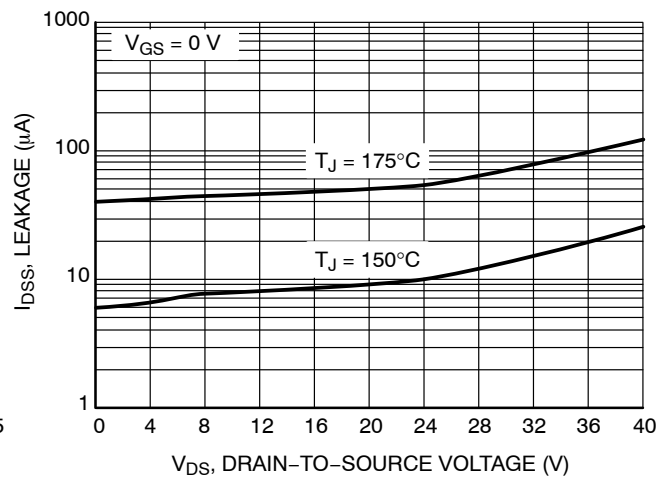


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

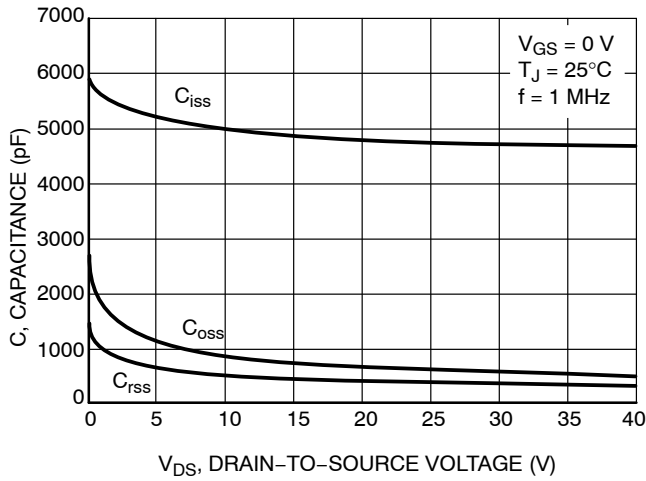


Figure 7. Capacitance Variation

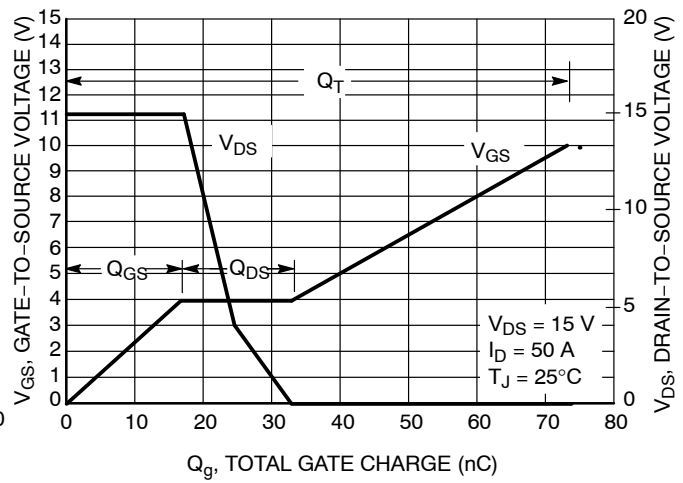


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

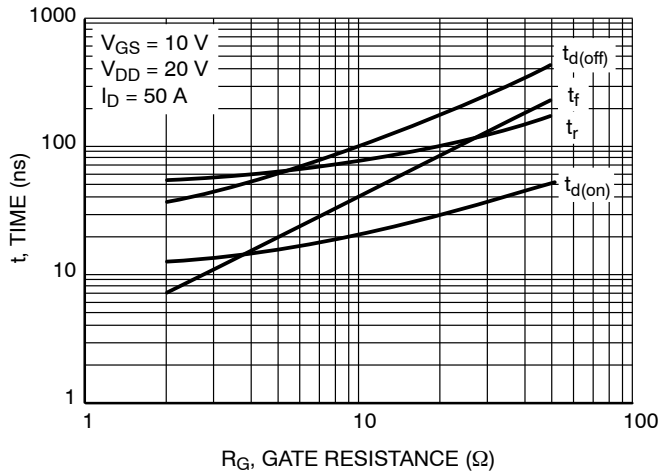


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

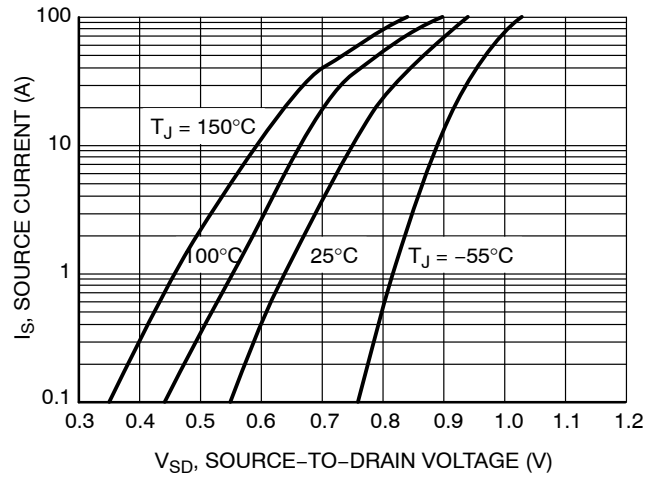


Figure 10. Diode Forward Voltage vs. Current

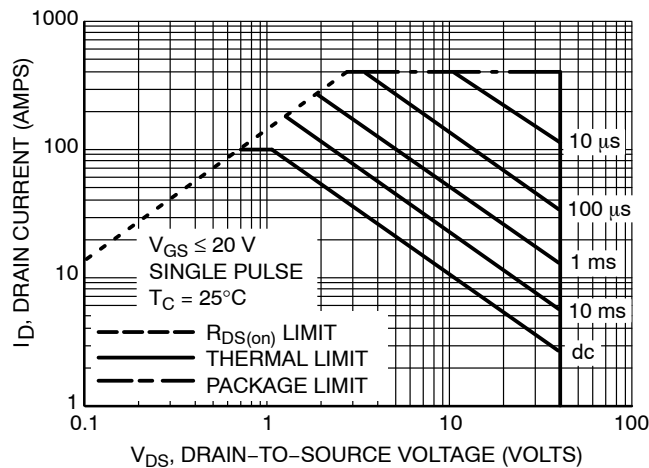


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NVD5890N

## TYPICAL PERFORMANCE CURVES

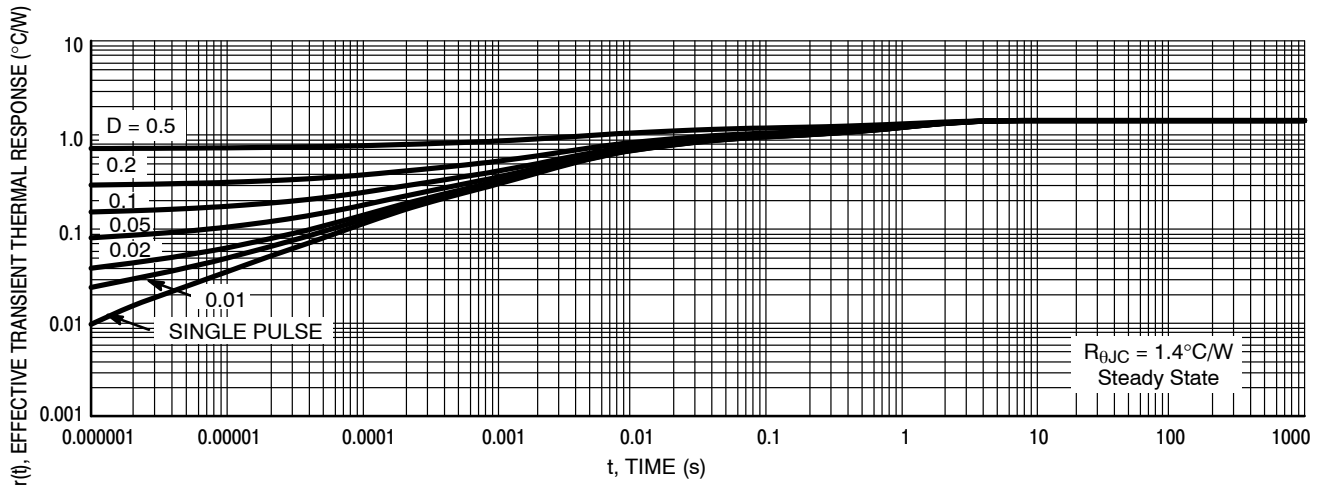


Figure 12. Thermal Response

### ORDERING INFORMATION

| Order Number     | Package           | Shipping <sup>†</sup> |
|------------------|-------------------|-----------------------|
| NVD5890NT4G      | DPAK<br>(Pb-Free) | 2500/Tape & Reel      |
| NVD5890NT4G-VF01 | DPAK<br>(Pb-Free) | 2500/Tape & Reel      |

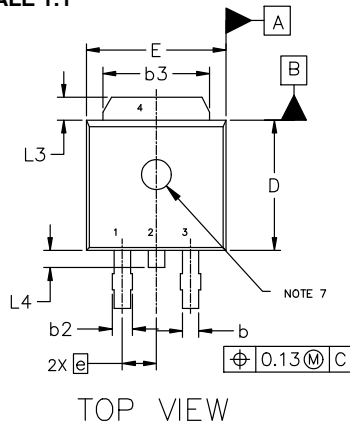
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



DPAK3 6.10x6.54x2.28, 2.29P  
CASE 369C  
ISSUE J

DATE 12 AUG 2025

SCALE 1:1



| MILLIMETERS |          |      |       |
|-------------|----------|------|-------|
| DIM         | MIN      | NOM  | MAX   |
| A           | 2.18     | 2.28 | 2.38  |
| A1          | 0.00     | ---  | 0.13  |
| b           | 0.63     | 0.76 | 0.89  |
| b2          | 0.72     | 0.93 | 1.14  |
| b3          | 4.57     | 5.02 | 5.46  |
| c           | 0.46     | 0.54 | 0.61  |
| c2          | 0.46     | 0.54 | 0.61  |
| D           | 5.97     | 6.10 | 6.22  |
| E           | 6.35     | 6.54 | 6.73  |
| e           | 2.29 BSC |      |       |
| H           | 9.40     | 9.91 | 10.41 |
| L           | 1.40     | 1.59 | 1.78  |
| L1          | 2.90 REF |      |       |
| L2          | 0.51 BSC |      |       |
| L3          | 0.89     | ---  | 1.27  |
| L4          | ---      | ---  | 1.01  |
| Z           | 3.93     | ---  | ---   |



NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

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**DPAK3 6.10x6.54x2.28, 2.29P**  
CASE 369C  
ISSUE J

DATE 12 AUG 2025

**GENERIC  
MARKING DIAGRAM\***



XXXXXX = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                                                                       |                                                                       |                                                                  |                                                                            |                                                                   |
|-----------------------------------------------------------------------|-----------------------------------------------------------------------|------------------------------------------------------------------|----------------------------------------------------------------------------|-------------------------------------------------------------------|
| STYLE 1:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | STYLE 2:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN          | STYLE 3:<br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | STYLE 4:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE              | STYLE 5:<br>PIN 1. GATE<br>2. ANODE<br>3. CATHODE<br>4. ANODE     |
| STYLE 6:<br>PIN 1. MT1<br>2. MT2<br>3. GATE<br>4. MT2                 | STYLE 7:<br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | STYLE 8:<br>PIN 1. N/C<br>2. CATHODE<br>3. ANODE<br>4. CATHODE   | STYLE 9:<br>PIN 1. ANODE<br>2. CATHODE<br>3. RESISTOR ADJUST<br>4. CATHODE | STYLE 10:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE |

|                         |                                    |                                                                                                                                                                                     |
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