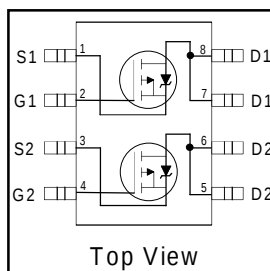


- Generation V Technology
- Ultra Low On-Resistance
- Dual P-Channel MOSFET
- Surface Mount
- Fully Avalanche Rated



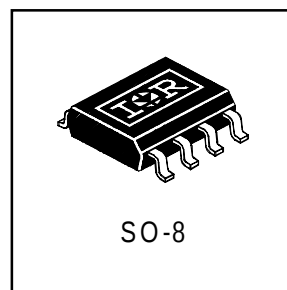
$$V_{DS} = -20V$$

$$R_{DS(on)} = 0.058\Omega$$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques.



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ^⑤	$T_A = 25^\circ\text{C}$	I_D	-5.3	A
	$T_A = 70^\circ\text{C}$		-4.3	
Pulsed Drain Current		I_{DM}	-21	
Continuous Source Current (Diode Conduction)		I_S	-2.5	
Maximum Power Dissipation ^⑤	$T_A = 25^\circ\text{C}$	P_D	2.0	W
	$T_A = 70^\circ\text{C}$		1.3	
Single Pulse Avalanche Energy		E_{AS}	150	mJ
Avalanche Current		I_{AR}	-2.9	A
Repetitive Avalanche Energy		E_{AR}	0.20	mJ
Peak Diode Recovery dv/dt ^③		dv/dt	-5.0	V/ ns
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to + 150	$^\circ\text{C}$

Thermal Resistance Ratings

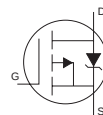
Parameter	Symbol	Limit	Units
Maximum Junction-to-Ambient ^⑤	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.031	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.049	0.058	Ω	$V_{GS} = -4.5V, I_D = -2.9A$ ④
		—	0.082	0.098		$V_{GS} = -2.7V, I_D = -1.5A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-0.70	—	—	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	—	5.9	—	S	$V_{DS} = -10V, I_D = -1.5A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -16V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -16V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = -12V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = 12V$
Q_g	Total Gate Charge	—	19	29	nC	$I_D = -2.9A$
Q_{gs}	Gate-to-Source Charge	—	4.0	6.1		$V_{DS} = -16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	7.7	12		$V_{GS} = -4.5V$, See Fig. 10 ④
$t_{d(on)}$	Turn-On Delay Time	—	15	22	ns	$V_{DD} = -10V$
t_r	Rise Time	—	40	60		$I_D = -2.9A$
$t_{d(off)}$	Turn-Off Delay Time	—	42	63		$R_G = 6.0\Omega$
t_f	Fall Time	—	49	73		$R_D = 3.4\Omega$ ④
C_{iss}	Input Capacitance	—	780	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	470	—		$V_{DS} = -15V$
C_{rss}	Reverse Transfer Capacitance	—	240	—		$f = 1.0MHz$, See Fig. 5

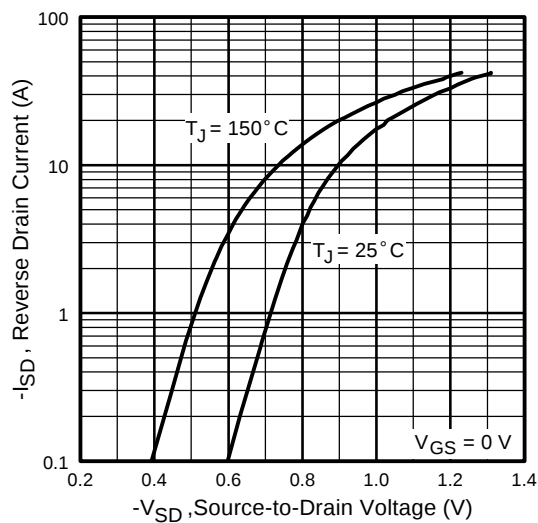
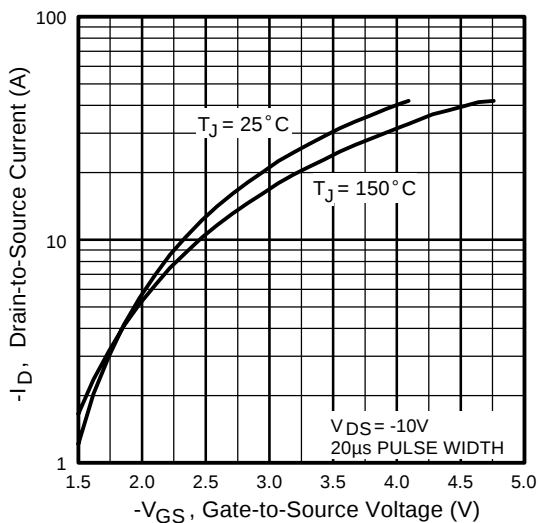
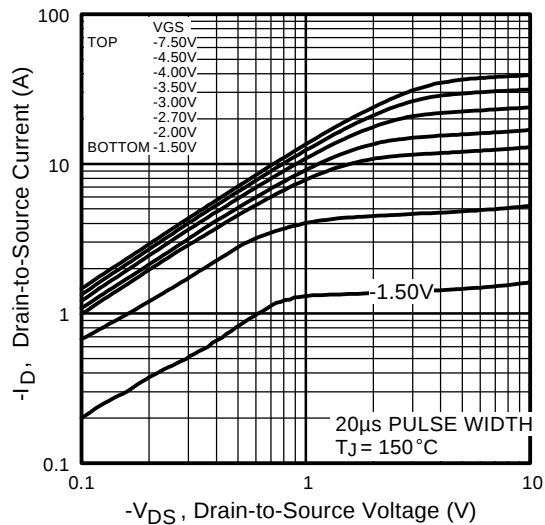
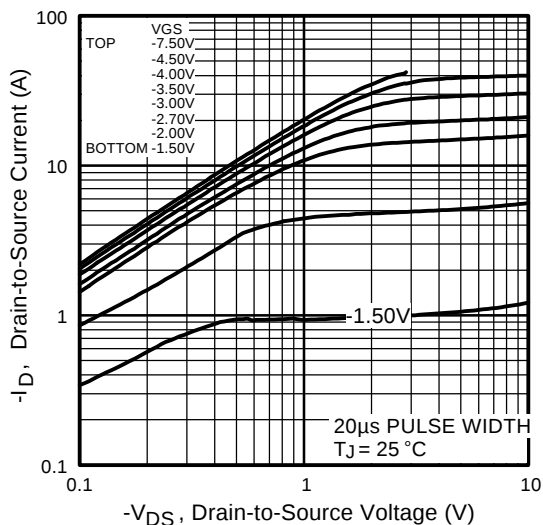
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-21		
V_{SD}	Diode Forward Voltage	—	-0.78	-1.0	V	$T_J = 25^\circ\text{C}$, $I_S = -2.9A$, $V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	47	71	ns	$T_J = 25^\circ\text{C}$, $I_F = -2.9A$
Q_{rr}	Reverse Recovery Charge	—	49	73	nC	$di/dt = 100A/\mu s$ ③



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 35mH$
 $R_G = 25\Omega$, $I_{AS} = -2.9A$.
- ③ $I_{SD} \leq -2.9A$, $di/dt \leq -77A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Surface mounted on FR-4 board, $t \leq 10sec$.



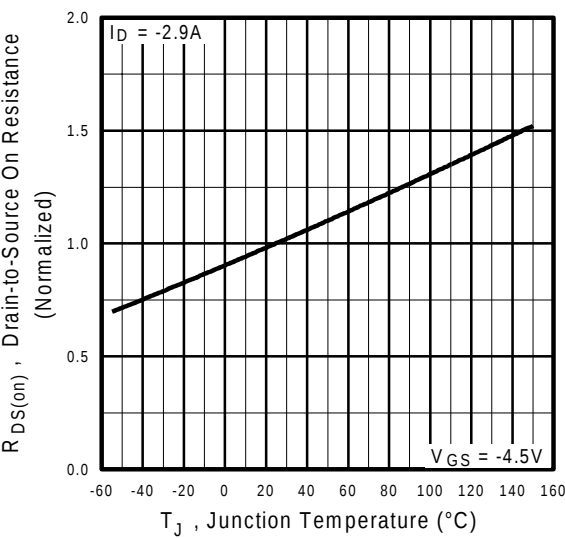


Fig 5. Normalized On-Resistance Vs. Temperature

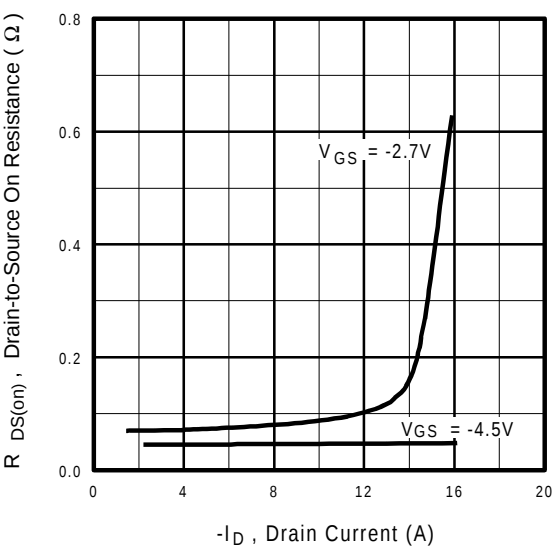


Fig 6. Typical On-Resistance Vs. Drain Current

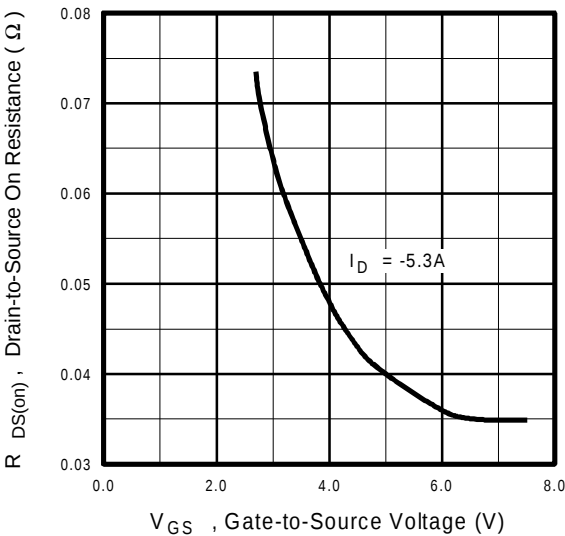


Fig 7. Typical On-Resistance Vs. Gate Voltage

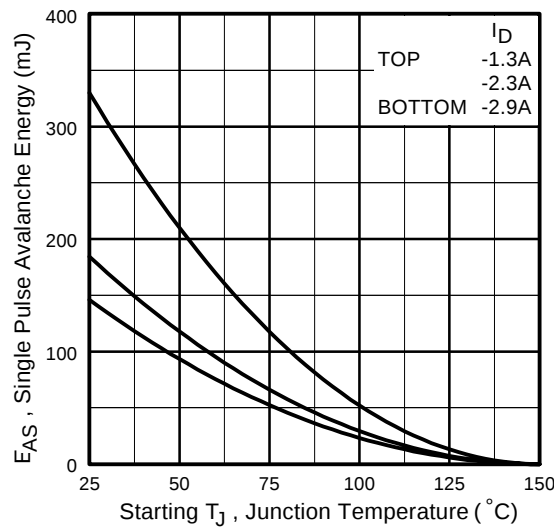


Fig 8. Maximum Avalanche Energy Vs. Drain Current

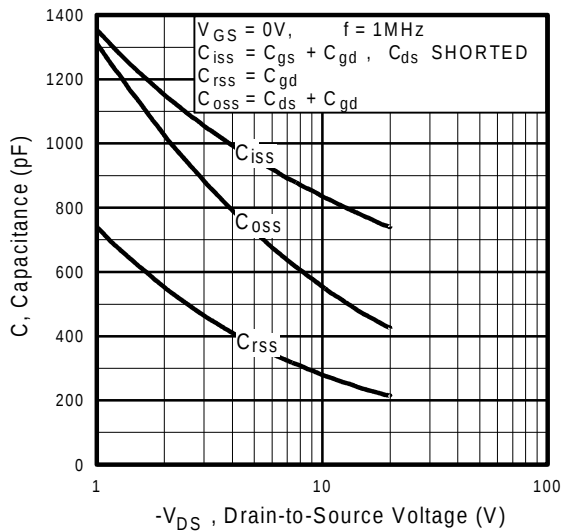


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

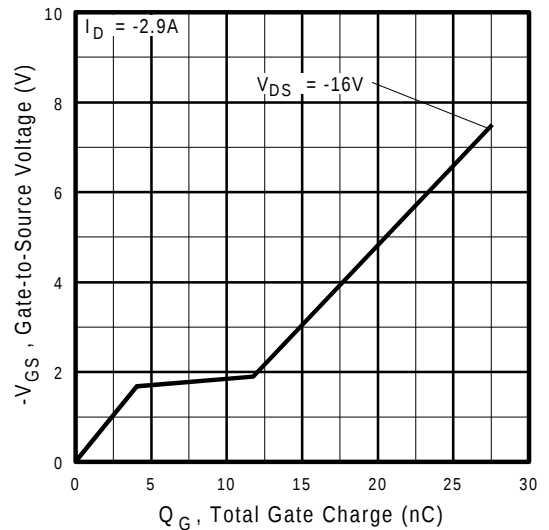


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

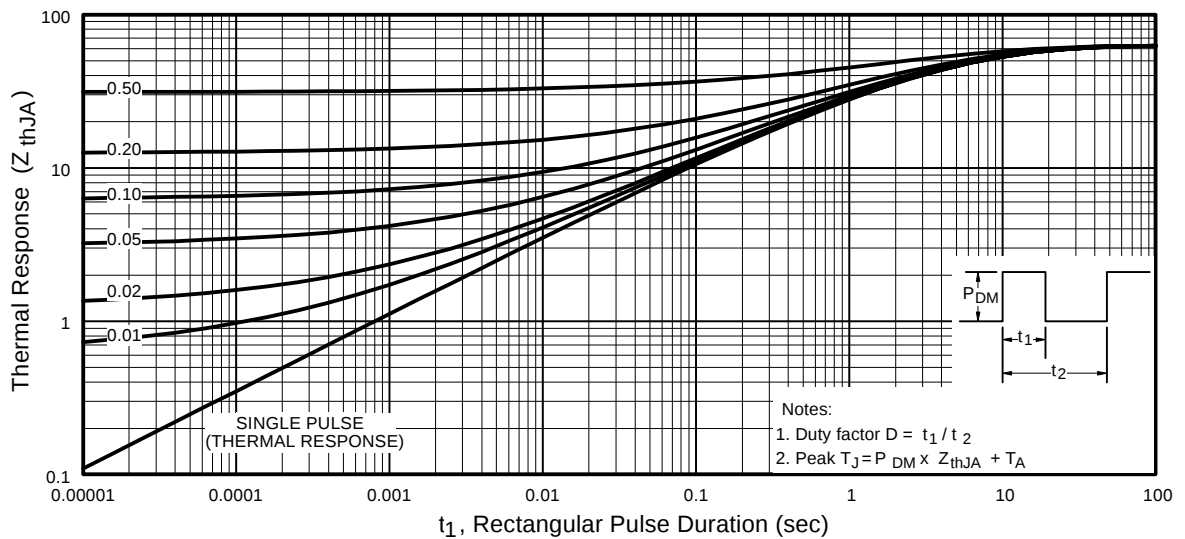
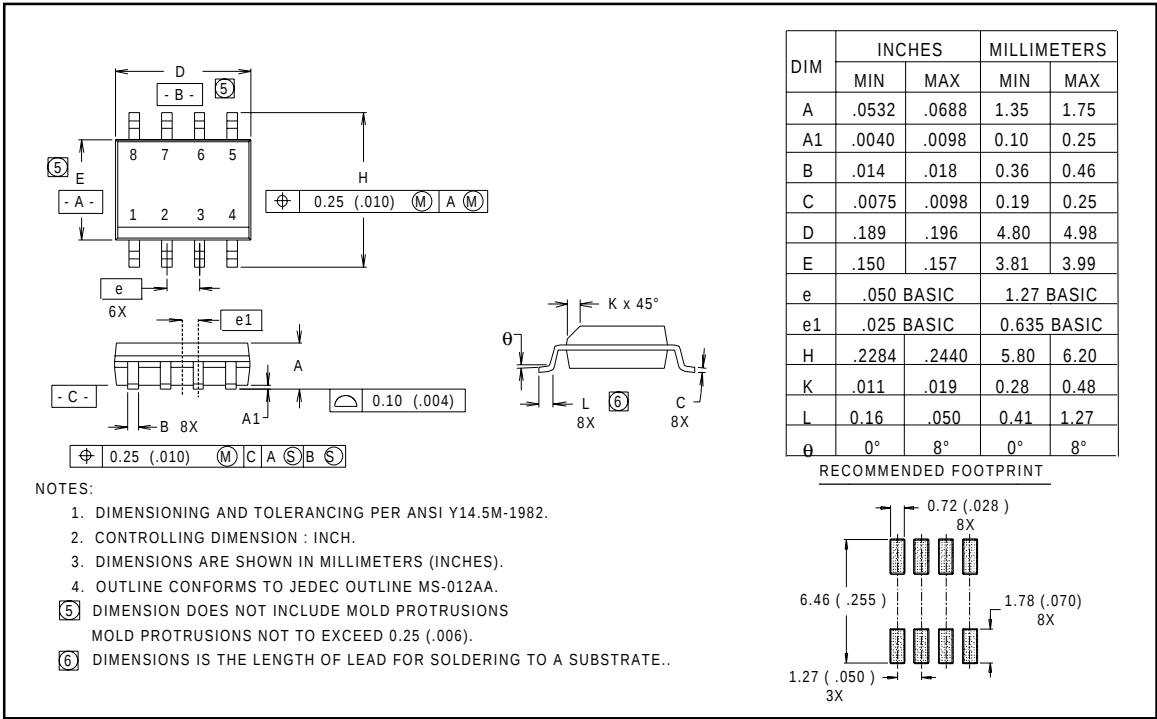


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

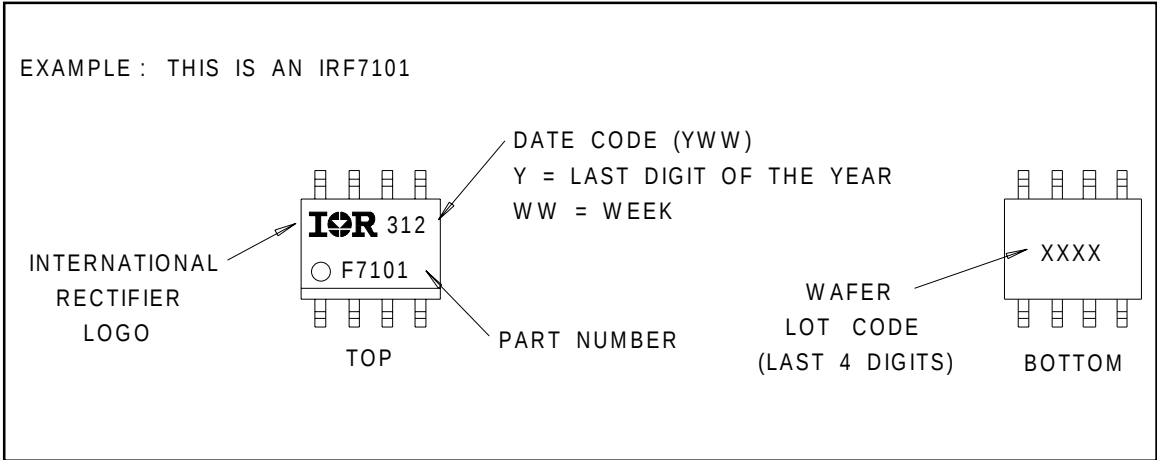
Package Outline

SO8 Outline



Part Marking Information

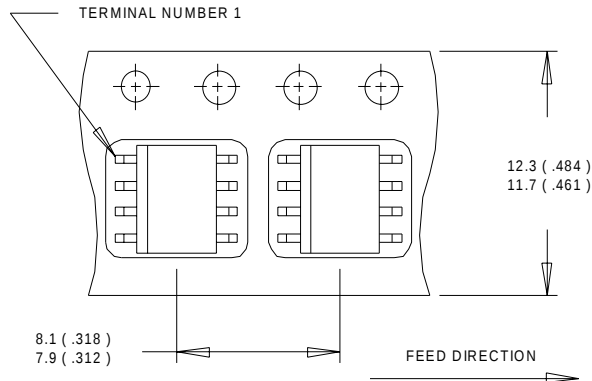
SO8



Tape & Reel Information

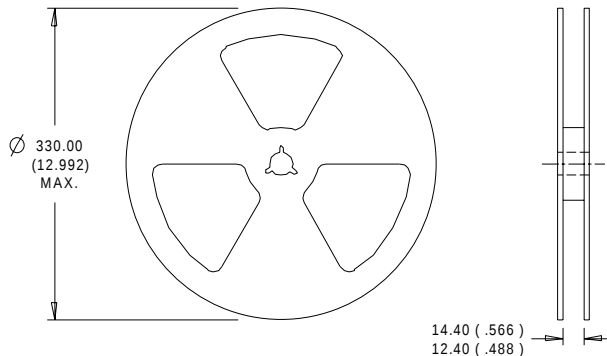
S08

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331

EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020

IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

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