TEXAS INSTRUMENTS

ADS8331, ADS8332

SBAS363E – DECEMBER 2009 – REVISED AUGUST 2016

ADS833x Low-Power, 16-Bit, 500-kSPS, 4- and 8-Channel Unipolar Input Analog-to-Digital Converters With Serial Interface

1 Features

- Low-Power, Flexible Supply Range:
  - 2.7-V to 5.5-V Analog Supply
  - 8.7 mW (250 kSPS in Auto-NAP Mode, VA = 2.7 V, VBD = 1.65 V)
  - 14.2 mW (500 kSPS, VA = 2.7 V, VBD = 1.65 V)
- Up to 500-kSPS Sampling Rate
- Excellent DC Performance:
  - ±1.2 LSB Typical, ±2 LSB Maximum INL at 2.7 V
  - ±0.6 LSB Typical, –1, 1.5 LSB Maximum DNL at 2.7 V
  - 16-Bit NMC Over Temperature
- Excellent AC Performance at 5 V, f_{IN} = 1 kHz:
  - 91.5-dB SNR, 101-dB SFDR, –100-dB THD
- Flexible Analog Input Arrangement:
  - On-Chip 4-, 8-Channel Mux With Breakout
  - Auto, Manual Channel Select and Trigger
- Other Hardware Features:
  - On-Chip Conversion Clock (CCLK)
  - Software, Hardware Reset
  - Programmable Status, Polarity EOC/$\overline{INT}$
  - Daisy-Chain Mode
  - Global $\overline{CONVST}$ (Independent of $\overline{CS}$)
  - Deep, Nap, and Auto-NAP Powerdown Modes
  - SPI™, DSP Compatible Serial Interface
  - Separate I/O Supply: 1.65 V to VA
  - SCLK up to 40 MHz (VA = VBD = 5 V)
- 24-Pin 4-mm × 4-mm VQFN and 24-Pin TSSOP Packages

2 Applications

- Communications
- Transducer Interfaces
- Medical Instruments
- Magnetometers
- Industrial Process Controls
- Data Acquisition Systems
- Automatic Test Equipment

3 Description

The ADS8331 is a low-power, 16-bit, 500-k samples-per-second (SPS) analog-to-digital converter (ADC) with a unipolar, 4-to-1 multiplexer (mux) input. The device includes a 16-bit capacitor-based successive approximation register (SAR) ADC with inherent sample and hold.

The ADS8332 is based on the same core and includes a unipolar 8-to-1 input mux. Both devices offer a high-speed, wide-voltage serial interface and are capable of daisy-chain operation when multiple converters are used.

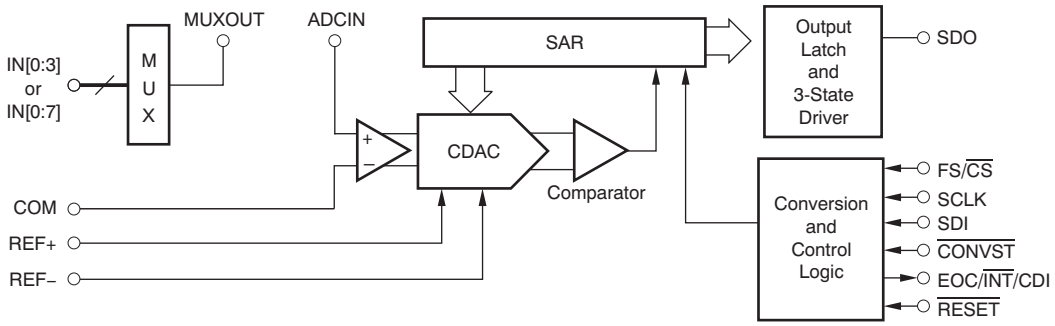
These converters are available in 24-pin, 4 × 4 VQFN and 24-pin TSSOP packages and are fully specified for operation over the industrial –40°C to 85°C temperature range.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS833x	VQFN (24)	4.00 mm × 4.00 mm
	TSSOP (24)	7.80 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2015) to Revision E — **Page**

- Changed VA parameter maximum specification in *Recommended Operating Conditions* table ... 6

Changes from Revision C (May 2012) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (December 2010) to Revision C — **Page**

- Changed name of last column in Low-Power, High-Speed, SAR Converter Family table ... 4
- Deleted 4-channel and 8-channel rows from 14-Bit Pseudo-Diff resolution in Low-Power, High-Speed, SAR Converter Family table ... 4
- Added last paragraph to *Start of a Conversion* section ... 25
- Changed VA value from 3.3 V to 2.7 V and V_{REF} value from 4.096 V to 2.5 V ... 38

Changes from Revision A (November 2010) to Revision B — **Page**

- Deleted Ordering Information table ... 6

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5 Companion Products

Part number	Name
REF3240	4.096V 4ppm/°C, 100uA SOT23-6 Series (Bandgap) Voltage Reference
DAC8562	16-bit, dual-channel, low-power, ultra-low glitch, buffered voltage output DAC with 2.5V,4ppm/°C ref
DAC8568	16-bit, octal-channel, ultra-low glitch, voltage output DAC with 2.5V, 2ppm/°C internal reference
LM5160	Wide Input 65V, 1.5A Synchronous Step-Down DC-DC Conv
OPA2348	1MHz, 45uA, RRIO, Dual Op Amp

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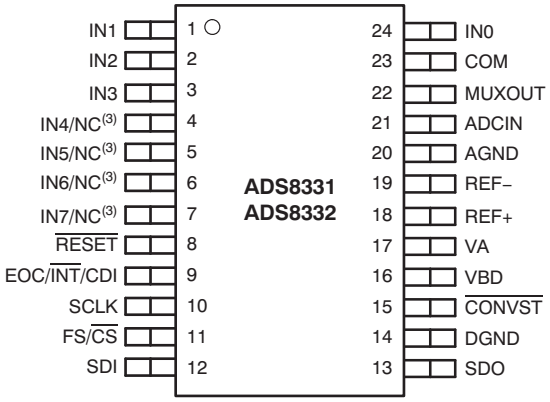
6 Device Comparison

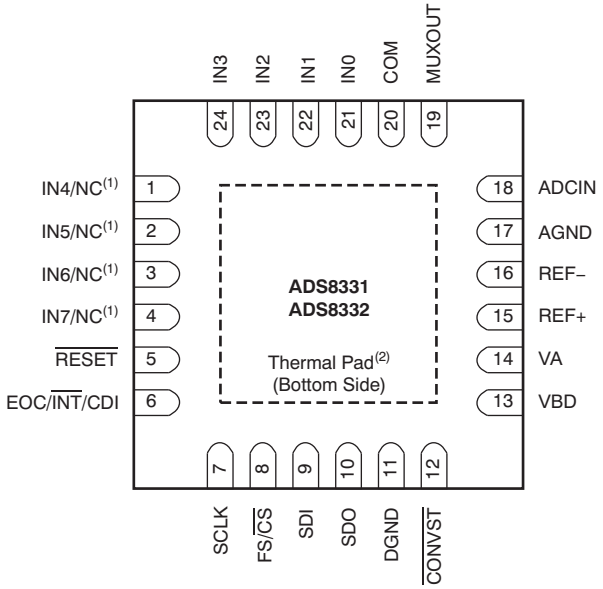
RESOLUTION	CHANNELS	$f_S \le 250$ kSPS	250 kSPS < $f_S \le 500$ kSPS	500 kSPS < $f_S \le 1$ MSPS
18 bits	8	—	ADS8698	—
	4	—	ADS8694	—
16 bits	8	ADS8344	ADS8688	—
		ADS8345	ADS8688A	
	4	ADS8341	ADS8684	—
		ADS8342	ADS8684A	
		ADS8343		
14 bits	8	TLC3548	ADS8678	—
		TLC3578		
	4	TLC3544	ADS8674	ADS7263
		TLC3574		

7 Pin Configuration and Functions

PW Package
24-Pin TSSOP
Top View



RGE Package
24-Pin VQFN With Exposed Thermal Pad
Top View



(1) NC = No internal connection (ADS8331 only).
(2) Connect thermal pad to analog ground.
(3) NC = No internal connection (ADS8331 only).

Pin Functions: ADS8331

PIN			I/O	DESCRIPTION
NAME	TSSOP	VQFN		
ADCIN	21	18	I	ADC input
AGND	20	17	—	Analog ground
DGND	14	11	—	Digital interface ground
COM	23	20	I	Common ADC input (usually connected to AGND)
$\overline{\text{CONVST}}$	15	12	I	Conversion start. Freezes sample and hold, starts conversion.

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Pin Functions: ADS8331 (continued)

PIN			I/O	DESCRIPTION
NAME	TSSOP	VQFN		
EOC/$\overline{\text{INT}}$/CDI	9	6	O/O/I	Status output. If programmed as end-of-conversion (EOC), this pin is low (default) when a conversion is in progress. If programmed as an interrupt ($\overline{\text{INT}}$), this pin is low (default) after the end of conversion and returns high after FS/$\overline{\text{CS}}$ goes low. The polarity of EOC or $\overline{\text{INT}}$ is programmable. This pin can also be used as a chain data input (CDI) when operated in daisy-chain mode.
FS/$\overline{\text{CS}}$	11	8	I	Frame sync signal for DSP (such as TMS320™ DSP) or chip select input for SPI.
$IN_{[0:3]}$	1-3, 24	21-24	I	Mux inputs
NC	4-7	1-4	—	No connection
MUXOUT	22	19	O	Mux output
REF+	18	15	I	External reference input
REF–	19	16	—	External reference ground (connect to AGND through an individual via on the printed-circuit-board)
$\overline{\text{RESET}}$	8	5	I	External reset (active low)
SCLK	10	7	I	SPI clock for serial interface
SDI	12	9	I	SPI serial data in
SDO	13	10	O	SPI serial data out
VA	17	14	—	Analog supply, 2.7 V to 5.5 V
VBD	16	13	—	Digital interface supply

Pin Functions: ADS8332

PIN			I/O	DESCRIPTION
NAME	TSSOP	VQFN		
ADCIN	21	18	I	ADC input
AGND	20	17	—	Analog ground
DGND	14	11	—	Digital interface ground
COM	23	20	I	Common ADC input (usually connected to AGND)
$\overline{\text{CONVST}}$	15	12	I	Conversion start. Freezes sample and hold, starts conversion.
EOC/$\overline{\text{INT}}$/CDI	9	6	O/O/I	Status output. If programmed as end-of-conversion (EOC), this pin is low (default) when a conversion is in progress. If programmed as an interrupt ($\overline{\text{INT}}$), this pin is low (default) after the end of conversion and returns high after FS/$\overline{\text{CS}}$ goes low. The polarity of EOC or $\overline{\text{INT}}$ is programmable. This pin can also be used as a chain data input (CDI) when operated in daisy-chain mode.
FS/$\overline{\text{CS}}$	11	8	I	Frame sync signal for DSP (such as TMS320™ DSP) or chip select input for SPI.
$IN_{[0:7]}$	1-7, 24	1-4, 21-24	I	Mux inputs
MUXOUT	22	19	O	Mux output
REF+	18	15	I	External reference input
REF–	19	16	—	External reference ground (connect to AGND through an individual via on the printed-circuit-board)
$\overline{\text{RESET}}$	8	5	I	External reset (active low)
SCLK	10	7	I	SPI clock for serial interface
SDI	12	9	I	SPI serial data in
SDO	13	10	O	SPI serial data out
VA	17	14	—	Analog supply, 2.7 V to 5.5 V
VBD	16	13	—	Digital interface supply

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN_X, MUXOUT, ADCIN, REF+ to AGND	–0.3	VA + 0.3	V
	COM, REF– to AGND	–0.3	0.3	
	VA to AGND	–0.3	7	
	VBD to DGND	–0.3	7	
	AGND to DGND	–0.3	0.3	
Digital input voltage to DGND		–0.3	VBD + 0.3	V
Digital output voltage to DGND		–0.3	VBD + 0.3	V
4 × 4 VQFN-24 Package	Power dissipation	$(T_J Max – T_A) / R_{\theta JA}$		W
	$R_{\theta JA}$ thermal impedance		47	°C/W
TSSOP-24 Package	Power dissipation	$(T_J Max – T_A) / \theta_{JA}$		W
	$R_{\theta JA}$ thermal impedance		47	°C/W
Operating free-air temperature, T_A		–40	85	°C
Junction temperature, T_J Max			150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VA	Analog supply voltage	2.7	3	5.5	V
VBD	Digital supply voltage	1.65	3	VA + 0.2	V

8.4 Thermal Information

THERMAL METRIC(1)		ADS833x		UNIT
		RGE (VQFN)	PW (TSSOP)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.9	78.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.2	12.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	33.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.7	33.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.25	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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8.5 Electrical Characteristics: VA = 2.7 V

at T_A = –40°C to 85°C, VA = 2.7 V, VBD = 1.65 V to 2.7 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUT							
	Full-scale input voltage (1)	IN_X – COM, ADCIN – COM		0		V_{REF}	V
	Absolute input voltage	IN_X, ADCIN		AGND – 0.2		VA + 0.2	V
		COM		AGND – 0.2		AGND + 0.2	
	Input capacitance	ADCIN			40	45	pF
	Input leakage current	Unselected ADC input			±1		nA
SYSTEM PERFORMANCE							
	Resolution				16		Bits
	No missing codes			16			Bits
INL	Integral linearity	ADS8331I, ADS8332I		–3	±2	3	LSB(2)
		ADS8331IB, ADS8332IB		–2	±1.2	2	
DNL	Differential linearity	ADS8331I, ADS8332I		–1	±0.6	2	LSB(2)
		ADS8331IB, ADS8332IB		–1	±0.6	1.5	
E_O	Offset error(3)			–0.5	±0.15	0.5	mV
	Offset error drift				±1		PPM/°C
	Offset error matching			–0.2		0.2	mV
E_G	Gain error			–0.25	–0.06	0.25	%FSR
	Gain error drift				±0.4		PPM/°C
	Gain error matching			–0.003		0.003	%FSR
	Transition noise				28		μV RMS
PSRR	Power-supply rejection ratio				74		dB
SAMPLING DYNAMICS							
t_{CONV}	Conversion time				18		CCLK
$t_{SAMPLE1}$	Acquisition time	Manual-trigger mode		3			CCLK
$t_{SAMPLE2}$		Auto-trigger mode			3		
	Throughput rate					500	kSPS
DYNAMIC CHARACTERISTICS							
THD	Total harmonic distortion (4)	V_{IN} = 2.5 V_{PP} at 1 kHz			–101		dB
		V_{IN} = 2.5 V_{PP} at 10 kHz			–95		
SNR	Signal-to-noise ratio	V_{IN} = 2.5 V_{PP} at 1 kHz	ADS8331I, ADS8332I		88		dB
			ADS8331IB, ADS8332IB		89		
		V_{IN} = 2.5 V_{PP} at 10 kHz	ADS8331I, ADS8332I		86.5		
			ADS8331IB, ADS8332IB		87.5		
SINAD	Signal-to-noise + distortion	V_{IN} = 2.5 V_{PP} at 1 kHz	ADS8331I, ADS8332I		87.5		dB
			ADS8331IB, ADS8332IB		88.5		
		V_{IN} = 2.5 V_{PP} at 10 kHz	ADS8331I, ADS8332I		86		
			ADS8331IB, ADS8332IB		87		
SFDR	Spurious-free dynamic range	V_{IN} = 2.5 V_{PP} at 1 kHz			103		dB
		V_{IN} = 2.5 V_{PP} at 10 kHz			98		
	Crosstalk	V_{IN} = 2.5 V_{PP} at 1 kHz			125		dB
		V_{IN} = 2.5 V_{PP} at 100 kHz			108		
	–3-dB small-signal bandwidth	IN_X – COM with MUXOUT tied to ADCIN			17		MHz
		ADCIN – COM			30		

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input (IN_X – COM) of 2.5 V when VA = 2.7 V.
(4) Calculated on the first nine harmonics of the input frequency.

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Electrical Characteristics: VA = 2.7 V (continued)

at T_A = –40°C to 85°C, VA = 2.7 V, VBD = 1.65 V to 2.7 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK							
	Internal conversion clock frequency			10.5	11	12.2	MHz
	SCLK external serial clock		Used as I/O clock only			25	MHz
			Used as both I/O clock and conversion clock	1		21	MHz
EXTERNAL VOLTAGE REFERENCE INPUT							
V_{REF}	Input reference range(5)	(REF+) – (REF–)		1.2		2.525	V
		(REF–) – AGND		–0.1		0.1	
	Resistance (6)		Reference input		20		kΩ
DIGITAL INPUT/OUTPUT							
	Logic family				CMOS		
V_{IH}	High-level input voltage		1.65 V < VBD < 2.5 V	0.8 × VBD		VBD + 0.3	V
			2.5 V ≤ VBD ≤ VA	0.65 × VBD		VBD + 0.3	
V_{IL}	Low-level input voltage		1.65 < VBD < 2.5 V	–0.3		0.1 × VBD	V
			2.5 V ≤ VBD ≤ VA	–0.3		0.25 × VBD	
I_I	Input current		V_{IN} = VBD or DGND	–1		1	µA
C_I	Input capacitance				5		pF
V_{OH}	High-level output voltage		VA ≥ VBD ≥ 1.65V, I_O = 100 µA	VBD – 0.6		VBD	V
V_{OL}	Low-level output voltage		VA ≥ VBD ≥ 1.65 V, I_O = –100 µA	0		0.4	V
C_O	SDO pin capacitance		Hi-Z state		5		pF
C_L	Load capacitance					30	pF
	Data format				Straight binary		
POWER-SUPPLY REQUIREMENTS							
VA	Analog supply voltage(5)			2.7		3.6	V
VBD	Digital I/O supply voltage			1.65		VA + 0.2	V
IA	Analog supply current		f_{SAMPLE} = 500 kSPS		5.2	6.5	mA
			f_{SAMPLE} = 250 kSPS in Auto-NAP mode		3.2		
			Nap mode, SCLK = VBD or DGND		325	400	µA
			Deep PD mode, SCLK = VBD or DGND		50	250	nA
IBD	Digital I/O supply current		f_{SAMPLE} = 500 kilobytes per second		0.1	0.4	mA
			f_{SAMPLE} = 250 kSPS in Auto-NAP mode		0.05		
	Power dissipation		VA = 2.7 V, VBD = 1.65 V, f_{SAMPLE} = 500 kSPS		14.2	18.2	mW
			VA = 2.7V, VBD = 1.65 V, f_{SAMPLE} = 250 kSPS in Auto-NAP mode		8.72		
TEMPERATURE RANGE							
T_A	Operating free-air temperature			–40		85	°C

(5) The ADS8331, ADS8332 operates with VA from 2.7 V to 5.5 V, and V_{REF} between 1.2 V and VA. However, the device may not meet the specifications listed in the *Electrical Characteristics* when VA is from 3.6 V to 4.5 V.
(6) Can vary ±30%.

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8.6 Electrical Characteristics: VA = 5 V

at T_A = –40°C to 85°C, VA = 5 V, VBD = 1.65 V to 5 V, V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUT							
	Full-scale input voltage (1)	IN_X – COM, ADCIN – COM		0		V_{REF}	V
	Absolute input voltage	IN_X, ADCIN		AGND – 0.2		VA + 0.2	V
		COM		AGND – 0.2		AGND + 0.2	
	Input capacitance	ADCIN			40	45	pF
	Input leakage current	Unselected ADC input			±1		nA
SYSTEM PERFORMANCE							
	Resolution				16		Bits
	No missing codes			16			Bits
INL	Integral linearity	ADS8331I, ADS8332I		–3	±2	3	LSB(2)
		ADS8331IB, ADS8332IB		–2	±1	2	
DNL	Differential linearity	ADS8331I, ADS8332I		–1	±1	2	LSB(2)
		ADS8331IB, ADS8332IB		–1	±0.5	1.5	
E_O	Offset error(3)			–1	±0.23	1	mV
	Offset error drift				±1		PPM/°C
	Offset error matching			–0.125		0.125	mV
E_G	Gain error			–0.25	–0.06	0.25	%FSR
	Gain error drift				±0.02		PPM/°C
	Gain error matching			–0.003		0.003	%FSR
	Transition noise				30		μV RMS
PSRR	Power-supply rejection ratio				78		dB
SAMPLING DYNAMICS							
t_{CONV}	Conversion time				18		CCLK
$t_{SAMPLE1}$	Acquisition time	Manual-trigger mode		3			CCLK
$t_{SAMPLE2}$		Auto-trigger mode			3		
	Throughput rate					500	kSPS
DYNAMIC CHARACTERISTICS							
THD	Total harmonic distortion (4)	V_{IN} = 4.096 V_{PP} at 1 kHz			–100		dB
		V_{IN} = 4.096 V_{PP} at 10 kHz	ADS8331I, ADS8332I		–94		
			ADS8331IB, ADS8332IB		–95		
SNR	Signal-to-noise ratio	V_{IN} = 4.096 V_{PP} at 1 kHz	ADS8331I, ADS8332I		90.5		dB
			ADS8331IB, ADS8332IB		91.5		
		V_{IN} = 4.096 V_{PP} at 10 kHz			88		
SINAD	Signal-to-noise + distortion	V_{IN} = 4.096 V_{PP} at 1 kHz	ADS8331I, ADS8332I		90		dB
			ADS8331IB, ADS8332IB		91		
		V_{IN} = 4.096 V_{PP} at 10 kHz			87		
SFDR	Spurious-free dynamic range	V_{IN} = 4.096 V_{PP} at 1 kHz			101		dB
		V_{IN} = 4.096 V_{PP} at 10 kHz			96		
	Crosstalk	V_{IN} = 4.096 V_{PP} at 1 kHz			119		dB
		V_{IN} = 4.096 V_{PP} at 100 kHz			107		
	–3-dB small-signal bandwidth	IN_X – COM with MUXOUT tied to ADCIN			22		MHz
		ADCIN – COM			40		

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input (IN_X – COM) of 4.096 V when VA = 5 V.
(4) Calculated on the first nine harmonics of the input frequency.

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Electrical Characteristics: VA = 5 V (continued)

at T_A = –40°C to 85°C, VA = 5 V, VBD = 1.65 V to 5 V, V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK							
	Internal conversion clock frequency			10.9	11.5	12.6	MHz
	SCLK external serial clock		Used as I/O clock only			40	MHz
			Used as both I/O clock and conversion clock	1		21	
EXTERNAL VOLTAGE REFERENCE INPUT							
V_{REF}	Input reference range(5)	(REF+) – (REF–)		1.2	4.096	4.2	V
		(REF–) – AGND		–0.1		0.1	
	Resistance (6)		Reference input		20		kΩ
DIGITAL INPUT/OUTPUT							
	Logic family				CMOS		
V_{IH}	High-level input voltage		1.65 < VBD < 2.5 V	0.8 × VBD		VBD + 0.3	V
			2.5 V ≤ VBD ≤ VA	0.65 × VBD		VBD + 0.3	
V_{IL}	Low-level input voltage		1.65 < VBD < 2.5 V	–0.3		0.1 × VBD	V
			2.5 V ≤ VBD ≤ VA	–0.3		0.25 × VBD	
I_I	Input current		V_{IN} = VBD or DGND	–1		1	µA
C_I	Input capacitance				5		pF
V_{OH}	High-level output voltage		VA ≥ VBD ≥ 1.65 V, I_O = 100 µA	VBD – 0.6		VBD	V
V_{OL}	Low-level output voltage		VA ≥ VBD ≥ 1.65 V, I_O = –100 µA	0		0.4	V
C_O	SDO pin capacitance		Hi-Z state		5		pF
C_L	Load capacitance					30	pF
	Data format				Straight binary		
POWER-SUPPLY REQUIREMENTS							
VA	Analog supply voltage(5)			4.5	5	5.5	V
VBD	Digital I/O supply voltage			1.65		VA + 0.2	V
IA	Analog supply current		f_{SAMPLE} = 500 kSPS		6.6	7.75	mA
			f_{SAMPLE} = 250 kSPS in Auto-NAP mode		4.2		
			Nap mode, SCLK = VBD or DGND		390	500	µA
			Deep PD mode, SCLK = VBD or DGND		80	250	nA
IBD	Digital I/O supply current		f_{SAMPLE} = 500 kSPS		1.2	2	mA
			f_{SAMPLE} = 250 kSPS in Auto-NAP mode		0.7		
	Power dissipation		VA = 5 V, VBD = 5 V, f_{SAMPLE} = 500 kSPS		39	48.75	mW
			VA = 5 V, VBD = 5 V, f_{SAMPLE} = 250 kSPS in Auto-NAP mode		24.5		
TEMPERATURE RANGE							
T_A	Operating free-air temperature			–40		85	°C

(5) The ADS8331, ADS8332 operates with VA from 2.7 V to 5.5 V, and V_{REF} between 1.2 V and VA. However, the device may not meet the specifications listed in the *Electrical Characteristics* when VA is from 3.6 V to 4.5 V.
(6) Can vary ±30%.

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8.7 Timing Requirements: VA = 2.7 V

at T_A = –40°C to 85°C, VA = 2.7 V, and VBD = 1.65 V (unless otherwise noted)(1)(2)

			MIN	NOM	MAX	UNIT
f_{CCLK}	Frequency, conversion clock, CCLK	External, f_{CCLK} = 1/2 f_{SCLK}	0.5		10.5	MHz
		Internal	10.5	11	12.2	
t_{SU1}	Setup time, rising edge of $\overline{CS}$ to EOC(3)	Read while converting	1			CCLK
t_{H1}	$\overline{CS}$ hold time with respect to EOC(3)	Read while sampling	25			ns
t_{WL1}	Pulse duration, $\overline{CONVST}$ low		40			ns
t_{WH1}	Pulse duration, $\overline{CS}$ high		40			ns
t_{SU2}	Setup time, rising edge of $\overline{CS}$ to EOS	Read while sampling	25			ns
t_{H2}	$\overline{CS}$ hold time with respect to EOS	Read while converting	25			ns
t_{SU3}	Setup time, falling edge of $\overline{CS}$ to first falling edge of SCLK		14			ns
t_{WL2}	Pulse duration, SCLK low		17		$t_{SCLK} - t_{WH2}$	ns
t_{WH2}	Pulse duration, SCLK high		12		$t_{SCLK} - t_{WL2}$	ns
t_{SCLK}	Cycle time, SCLK	I/O clock only	40			ns
		I/O and conversion clocks	47.6		1000	
		I/O clock, daisy-chain mode	40			
		I/O and conversion clocks, daisy-chain mode	47.6		1000	
t_{D1}	Delay time, falling edge of SCLK to SDO invalid	10-pF load	8			ns
t_{D2}	Delay time, falling edge of SCLK to SDO valid	10-pF load			35	ns
t_{D3}	Delay time, falling edge of $\overline{CS}$ to SDO valid, SDO MSB output	10-pF load			35	ns
t_{SU4}	Setup time, SDI to falling edge of SCLK		8			ns
t_{H3}	Hold time, SDI to falling edge of SCLK		8			ns
t_{D4}	Delay time, rising edge of $\overline{CS}$ to SDO 3-state	10-pF load			15	ns
t_{SU5}	Setup time, last falling edge of SCLK before rising edge of $\overline{CS}$		15			ns
t_{H4}	Hold time, last falling edge of SCLK before rising edge of $\overline{CS}$		2			ns
t_{SU6}(4)	Setup time, rising edge of SCLK to rising edge of $\overline{CS}$		10			ns
t_{H5}(4)	Hold time, rising edge of SCLK to rising edge of $\overline{CS}$		2			ns
t_{D5}	Delay time, falling edge of $\overline{CS}$ to deactivation of $\overline{INT}$	10-pF load			40	ns

(1) All input signals are specified with $t_r = t_f$ = 1.5 ns (10% to 90% of VBD) and timed from a voltage level of (V_{IL} + V_{IH}) / 2.
(2) See the timing diagrams.
(3) The EOC and EOS signals are the inverse of each other.
(4) Applies to the 5th or 17th rising SCLK when sending 4-bit or 16-bit commands, respectively, to the ADS8331, ADS8332.

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8.8 Timing Characteristics: VA = 5 V

at T_A = –40°C to 85°C, and VA = VBD = 5 V (unless otherwise noted)(1)(2)

			MIN	TYP	MAX	UNIT
f_{CCLK}	Frequency, conversion clock, CCLK	External, f_{CCLK} = 1/2 f_{SCLK}	0.5		10.5	MHz
		Internal	10.9	11.5	12.6	
t_{SU1}	Setup time, rising edge of $\overline{CS}$ to EOC(3)	Read while converting	1			CCLK
t_{H1}	$\overline{CS}$ hold time with respect to EOC(3)	Read while sampling	20			ns
t_{WL1}	Pulse duration, $\overline{CONVST}$ low		40			ns
t_{WH1}	Pulse duration, $\overline{CS}$ high		40			ns
t_{SU2}	Setup time, rising edge of $\overline{CS}$ to EOS	Read while sampling	20			ns
t_{H2}	$\overline{CS}$ hold time with respect to EOS	Read while converting	20			ns
t_{SU3}	Setup time, falling edge of $\overline{CS}$ to first falling edge of SCLK		8			ns
t_{WL2}	Pulse duration, SCLK low		12		$t_{SCLK} - t_{WH2}$	ns
t_{WH2}	Pulse duration, SCLK high		11		$t_{SCLK} - t_{WL2}$	ns
t_{SCLK}	Cycle time, SCLK	I/O clock only	25			ns
		I/O and conversion clocks	47.6		1000	
		I/O clock, daisy-chain mode	25			
		I/O and conversion clocks, daisy-chain mode	47.6		1000	
t_{D1}	Delay time, falling edge of SCLK to SDO invalid	10-pF load	5			ns
t_{D2}	Delay time, falling edge of SCLK to SDO valid	10-pF load			20	ns
t_{D3}	Delay time, falling edge of $\overline{CS}$ to SDO valid, SDO MSB output	10-pF load			20	ns
t_{SU4}	Setup time, SDI to falling edge of SCLK		8			ns
t_{H3}	Hold time, SDI to falling edge of SCLK		8			ns
t_{D4}	Delay time, rising edge of $\overline{CS}$ to SDO 3-state	10-pF load			10	ns
t_{SU5}	Setup time, last falling edge of SCLK before rising edge of $\overline{CS}$		10			ns
t_{H4}	Hold time, last falling edge of SCLK before rising edge of $\overline{CS}$		2			ns
t_{SU6}(4)	Setup time, rising edge of SCLK to rising edge of $\overline{CS}$		10			ns
t_{H5}(4)	Hold time, rising edge of SCLK to rising edge of $\overline{CS}$		2			ns
t_{D5}	Delay time, falling edge of $\overline{CS}$ to deactivation of $\overline{INT}$	10-pF load			20	ns

(1) All input signals are specified with $t_r = t_f$ = 1.5 ns (10% to 90% of VBD) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$.
(2) See the timing diagrams.
(3) The EOC and EOS signals are the inverse of each other.
(4) Applies to the 5th or 17th rising SCLK when sending 4-bit or 16-bit commands, respectively, to the ADS8331, ADS8332.

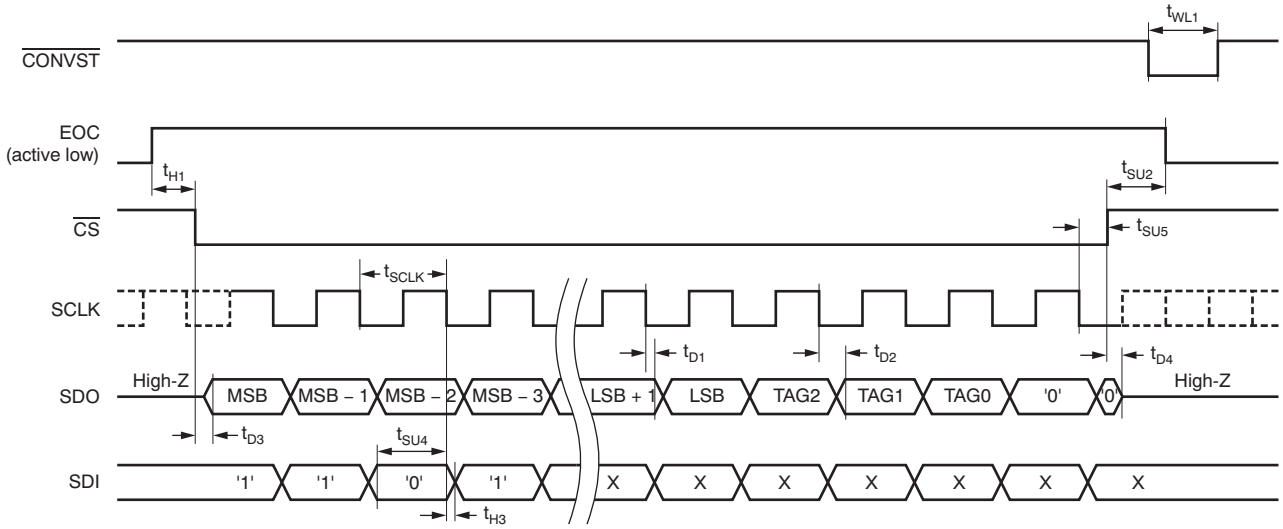

Figure 1. Read While Sampling (Shown With Manual-Trigger Mode)

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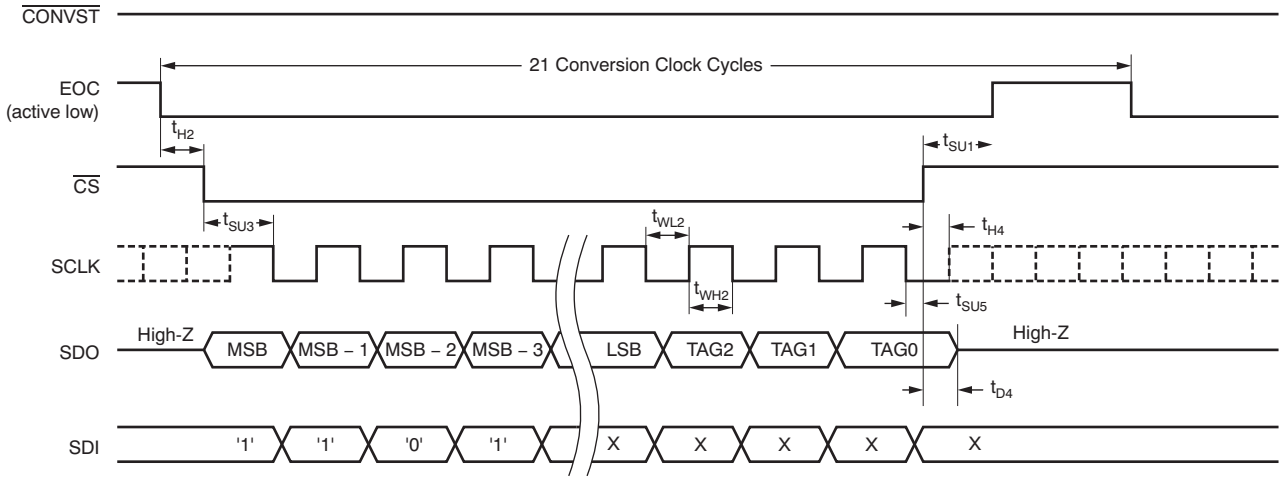

Figure 2. Read While Converting (Shown With Auto-Trigger Mode at 500 kSPS)

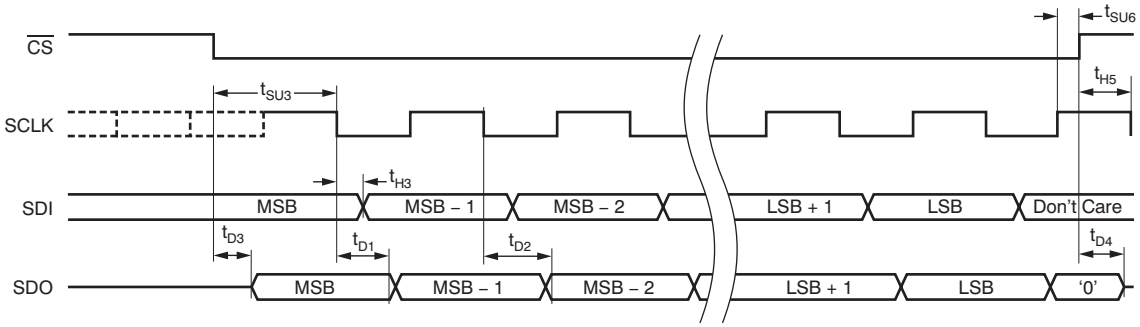

Figure 3. SPI I/O

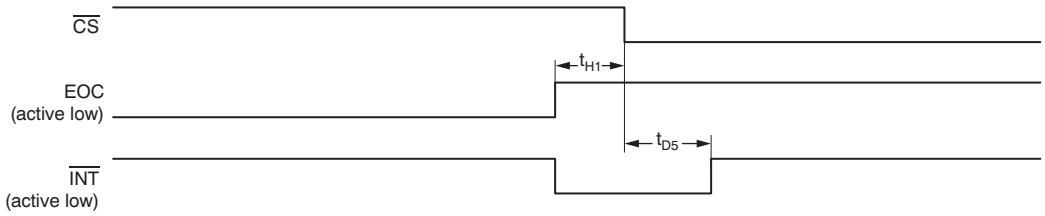

Figure 4. Relationship among $\overline{CS}$, EOC, and $\overline{INT}$

8.9 Typical Characteristics: DC Performance

at T_A = 25°C, V_{REF} (REF+ – REF–) = 4.096 V when VA = VBD = 5 V or V_{REF} (REF+ – REF–) = 2.5 V when VA = VBD = 2.7 V, f_{SCLK} = 21 MHz, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

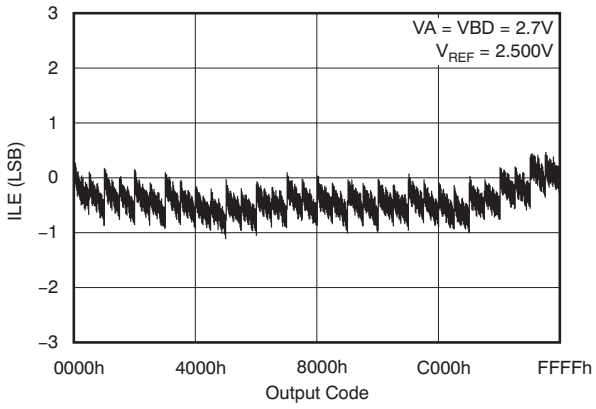

Figure 5. Integral Linearity Error vs Code

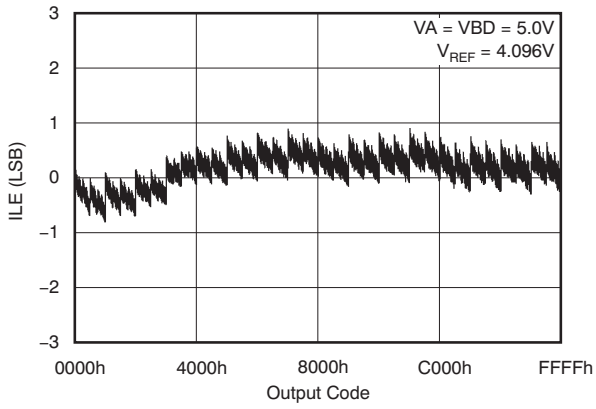

Figure 6. Integral Linearity Error vs Code

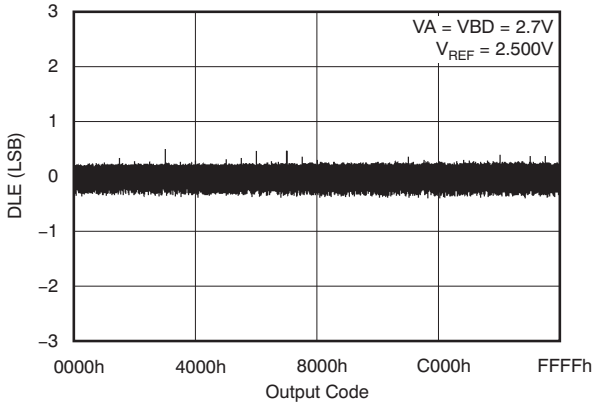

Figure 7. Differential Linearity Error vs Code

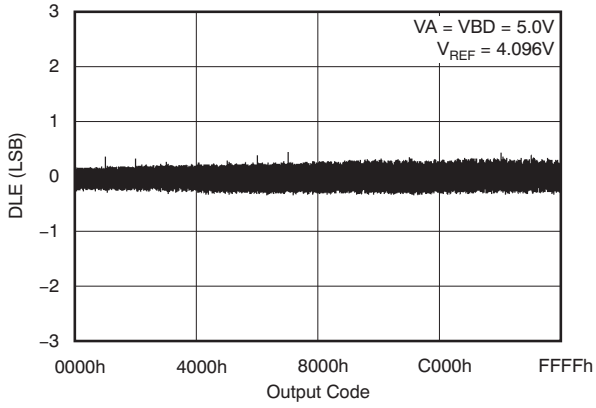

Figure 8. Differential Linearity Error vs Code

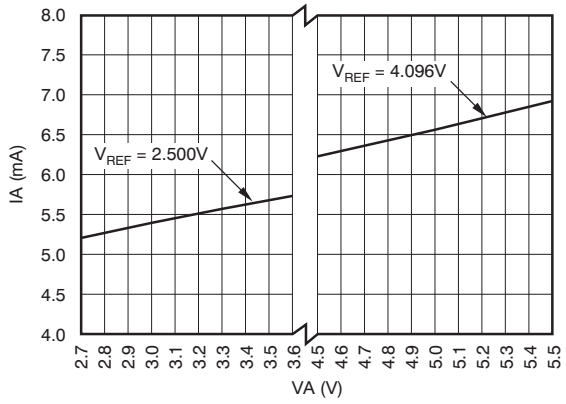

Figure 9. Analog Supply Current vs Analog Supply Voltage

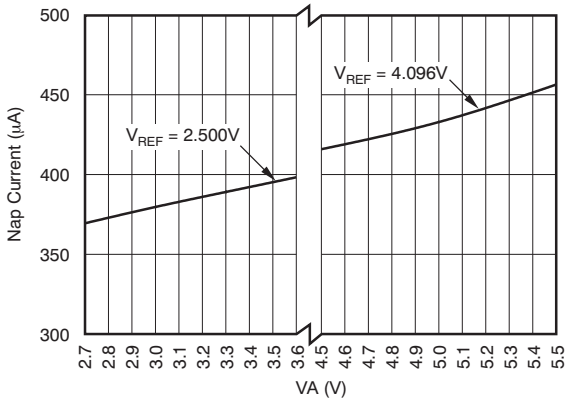

Figure 10. Analog Supply Current in NAP Mode vs Analog Supply Voltage

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Typical Characteristics: DC Performance (continued)

at T_A = 25°C, V_{REF} (REF+ – REF–) = 4.096 V when VA = VBD = 5 V or V_{REF} (REF+ – REF–) = 2.5 V when VA = VBD = 2.7 V, f_{SCLK} = 21 MHz, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

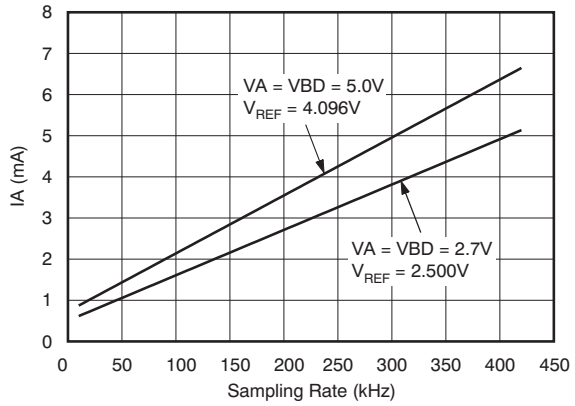

Figure 11. Analog Supply Current vs Sampling Rate in Auto-NAP Mode

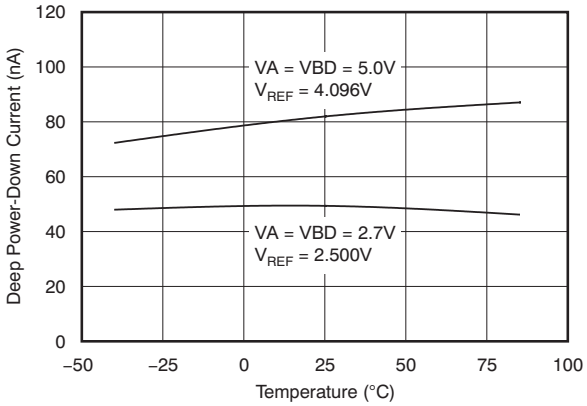

Figure 12. Deep Power-Down Current vs Temperature

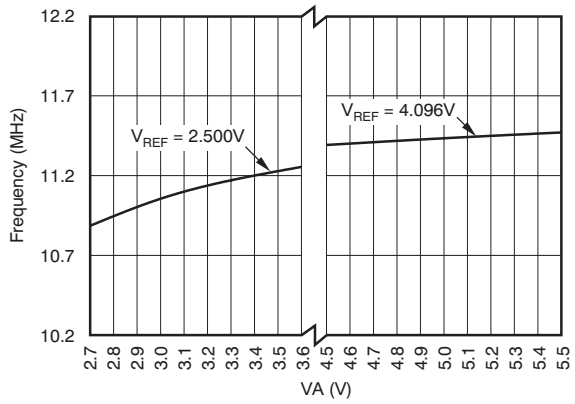

Figure 13. Internal Clock Frequency vs Analog Supply Voltage

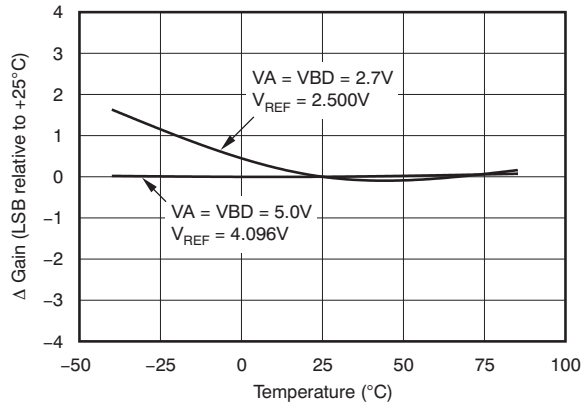

Figure 14. Change in Gain vs Temperature

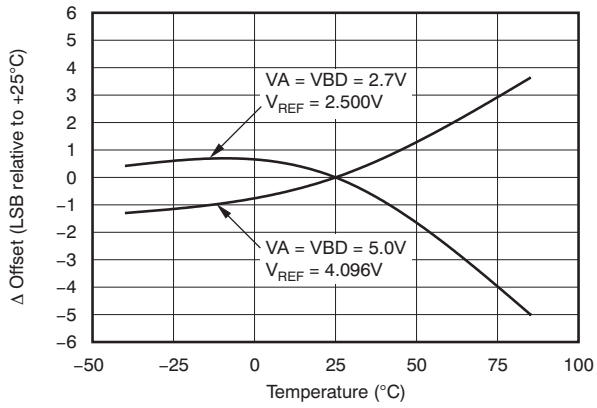

Figure 15. Change in Offset vs Temperature

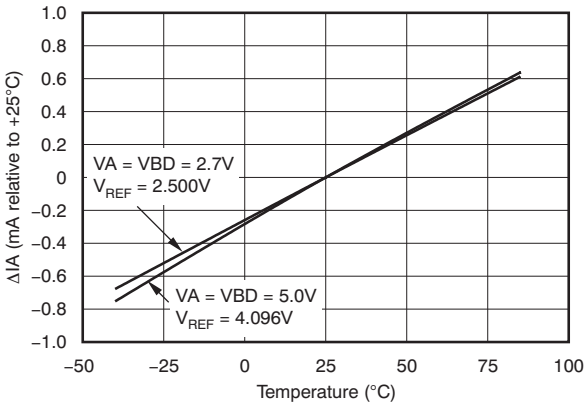

Figure 16. Change in Analog Supply Current vs Temperature

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Typical Characteristics: DC Performance (continued)

at T_A = 25°C, V_{REF} (REF+ – REF–) = 4.096 V when VA = VBD = 5 V or V_{REF} (REF+ – REF–) = 2.5 V when VA = VBD = 2.7 V, f_{SCLK} = 21 MHz, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

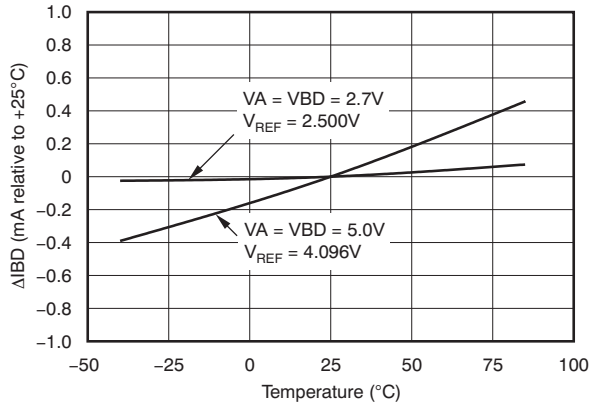

Figure 17. Change in Digital Supply Current vs Temperature

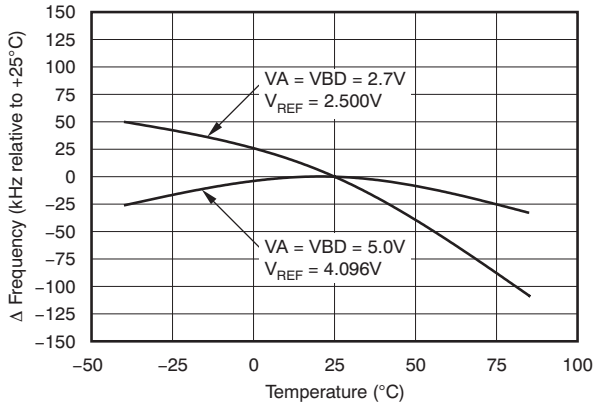

Figure 18. Change in Internal Clock Frequency vs Temperature

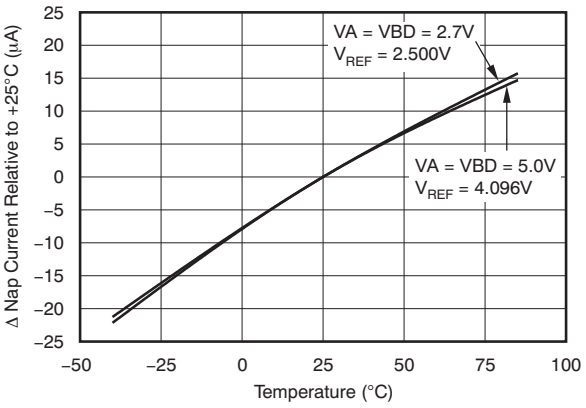

Figure 19. Change in Analog Supply Current in NAP Mode vs Temperature

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8.10 Typical Characteristics: AC Performance

at T_A = 25°C, V_{REF} (REF+ – REF–) = 4.096 V when VA = VBD = 5 V or V_{REF} (REF+ – REF–) = 2.5 V when VA = VBD = 2.7 V, f_{SCLK} = 21 MHz, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

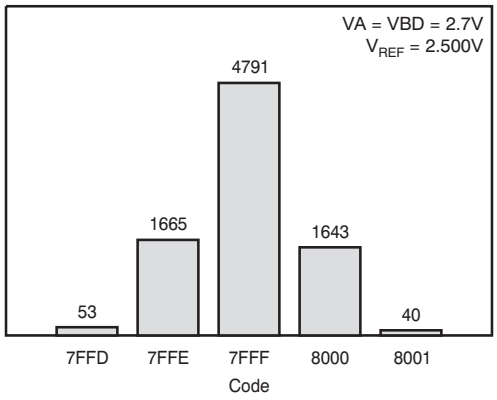

Figure 20. Output Code Histogram for a DC Input (8192 Conversions)

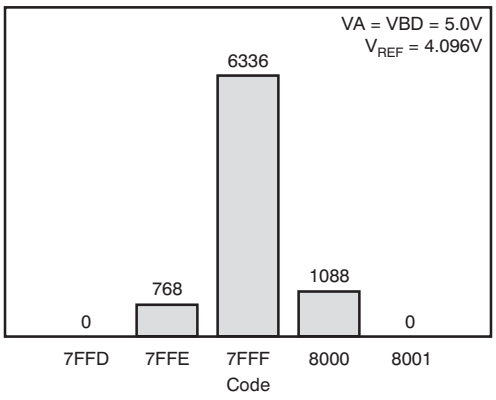

Figure 21. Output Code Histogram for a DC Input (8192 Conversions)

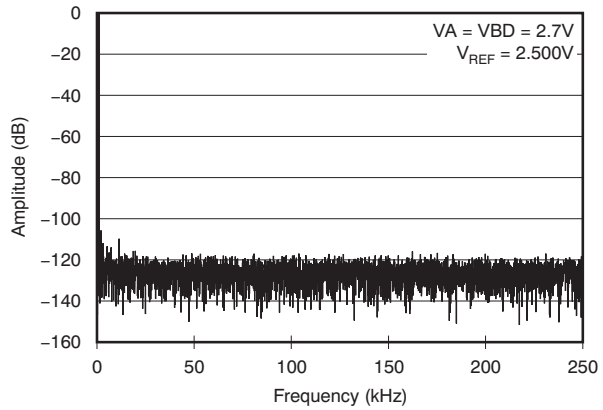

Figure 22. Frequency Spectrum (8192 Point FFT, f_{IN} = 1.0376 kHz, –0.2 dB)

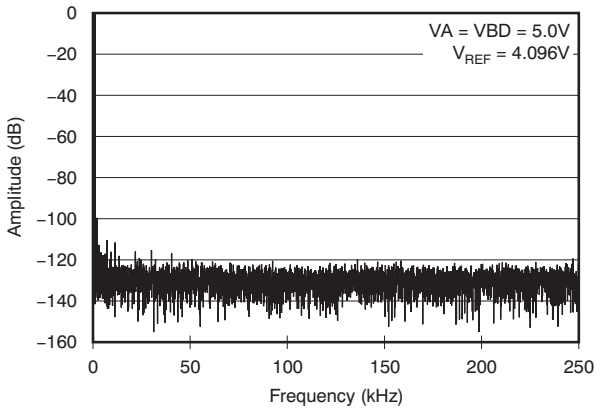

Figure 23. Frequency Spectrum (8192 Point FFT, f_{IN} = 1.0376 kHz, –0.2 dB)

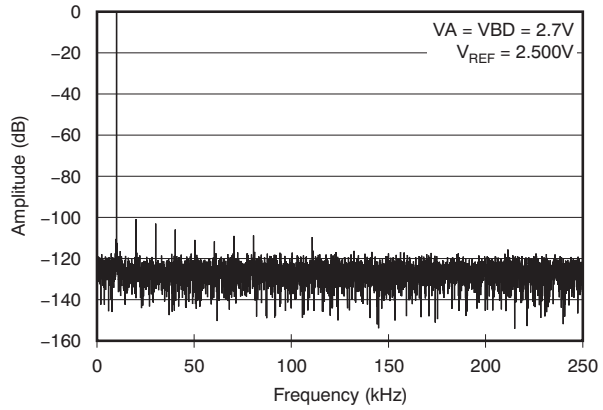

Figure 24. Frequency Spectrum (8192 Point FFT, f_{IN} = 10.0708 kHz, –0.2 dB)

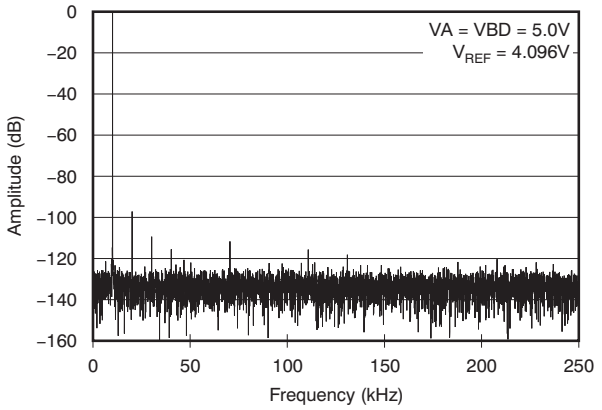

Figure 25. Frequency Spectrum (8192 Point FFT, f_{IN} = 10.0708 kHz, –0.2 dB)

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Typical Characteristics: AC Performance (continued)

at T_A = 25°C, V_{REF} (REF+ – REF–) = 4.096 V when VA = VBD = 5 V or V_{REF} (REF+ – REF–) = 2.5 V when VA = VBD = 2.7 V, f_{SCLK} = 21 MHz, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

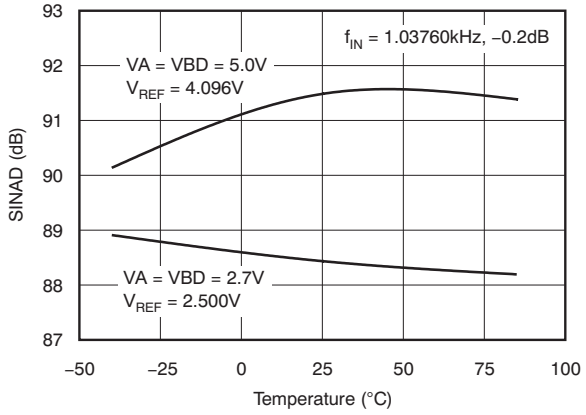

Figure 26. Signal-to-Noise + Distortion vs Temperature

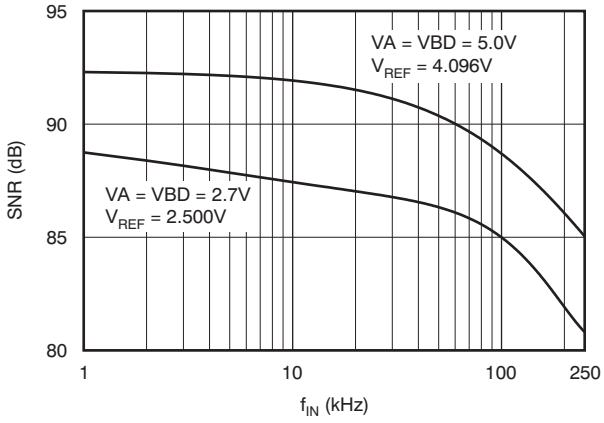

Figure 27. Signal-to-Noise Ratio vs Input Frequency

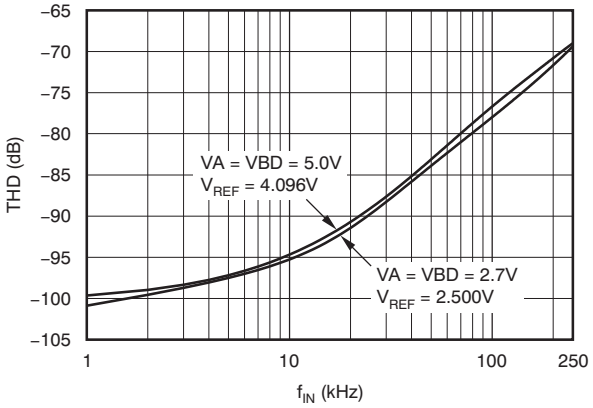

Figure 28. Total Harmonic Distortion vs Input Frequency

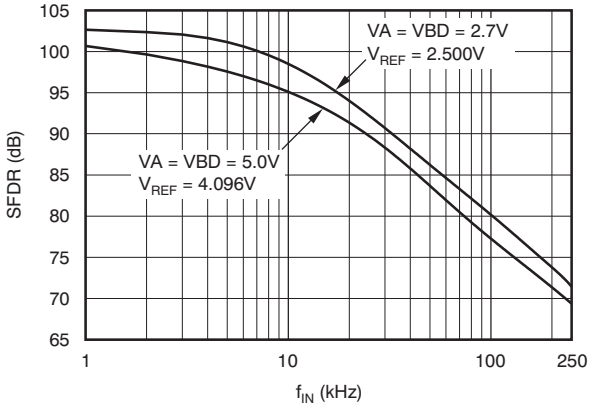

Figure 29. Spurious-Free Dynamic Range vs Input Frequency

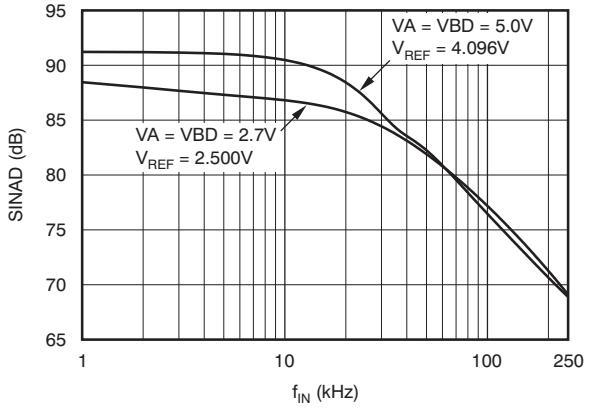

Figure 30. Signal-to-Noise + Distortion vs Input Frequency

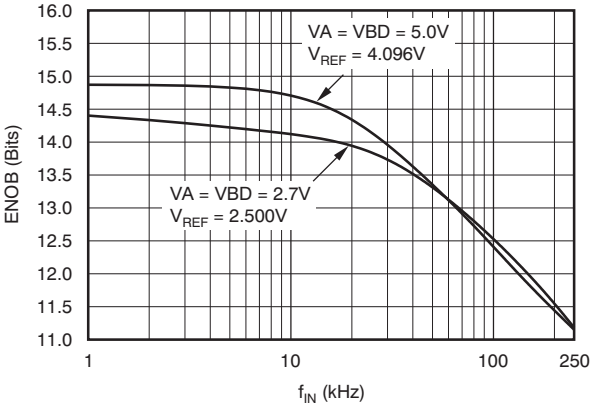

Figure 31. Effective Number of Bits vs Input Frequency

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Typical Characteristics: AC Performance (continued)

at T_A = 25°C, V_{REF} (REF+ – REF–) = 4.096 V when VA = VBD = 5 V or V_{REF} (REF+ – REF–) = 2.5 V when VA = VBD = 2.7 V, f_{SCLK} = 21 MHz, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

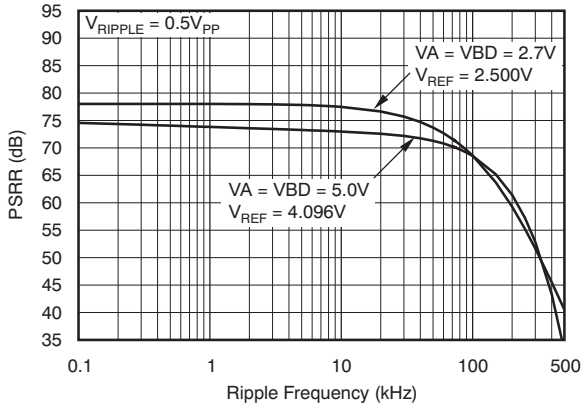

Figure 32. Power-Supply Rejection Ratio vs Power-Supply Ripple Frequency

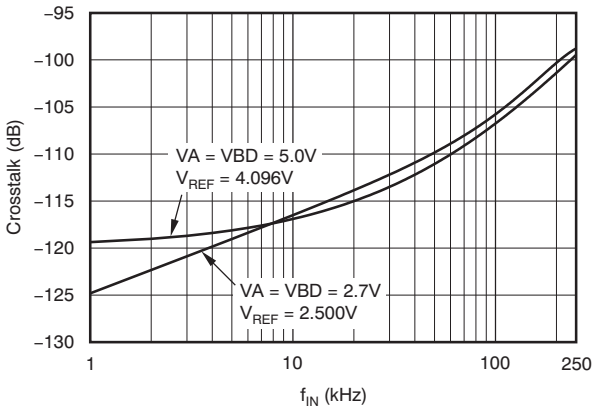

Figure 33. Crosstalk vs Input Frequency

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9 Detailed Description

9.1 Overview

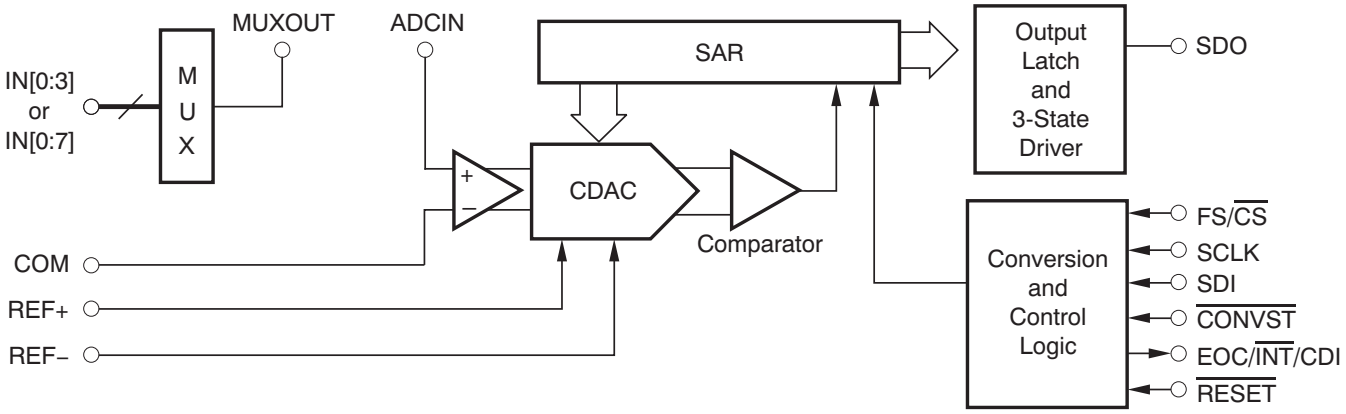
The ADS833x is a high-speed, low-power, successive approximation register (SAR) analog-to-digital converter (ADC) that uses an external reference. The architecture is based on charge redistribution, which inherently includes a sample/hold function.

The ADS833x has an internal clock that is used to run the conversion. However, the ADS833x can be programmed to run the conversion based on the external serial clock (SCLK).

The analog input to the ADS833x is provided to two input pins: one of the IN_X input channels and the shared COM pin. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both IN_X and COM inputs are disconnected from any internal function.

The ADS8331 has four analog inputs while the ADS8332 has eight inputs. All inputs share the same common pin, COM. Both the ADS8331 and ADS8332 can be programmed to select a channel manually or can be programmed into the auto channel select mode to sweep through the input channels automatically.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Signal Conditioning

The ADS833x has the flexibility to add signal conditioning between the MUXOUT and ADCIN pins, such as a programmable gain amplifier (PGA) or filter. This feature reduces the system component count and cost because each input channel does not require separate signal conditioning circuits, especially if the source impedance connected to each channel is similar in value.

9.3.2 Analog Input

When the converter enters the hold mode, the voltage difference between the IN_X and COM inputs is captured on the internal capacitor array. The voltage on the COM pin is limited from (AGND – 0.2 V) to (AGND + 0.2 V). This limitation allows the ADS833x to reject small signals that are common to both the IN_X and COM inputs. The IN_X inputs have a range of –0.2 V to (VA + 0.2 V). The input span of (IN_X – COM) is limited to 0 V to V_{REF}.

The peak input current through the analog inputs depends upon a number of factors: reference voltage, sample rate, input voltage, and source impedance. The current flowing into the ADS833x charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the maximum input capacitance (45 pF) to a 16-bit settling level within the minimum acquisition time (238 ns). When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

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Feature Description (continued)

Take care when regarding the absolute analog input voltage. To maintain linearity of the converter, the IN_X inputs, the COM input, and the input span of (IN_X – COM) should be within the limits specified. If these inputs are outside of these ranges, the linearity of the converter may not meet specifications. To minimize noise, low-bandwidth input signals with low-pass filters should be used. Ensure that the output impedance of the sources driving the IN_X and COM inputs are matched, as shown in Figure 34. If this matching is not observed, the two inputs could have different settling times, which may result in an offset error, gain error, and linearity error that change with temperature and input voltage.

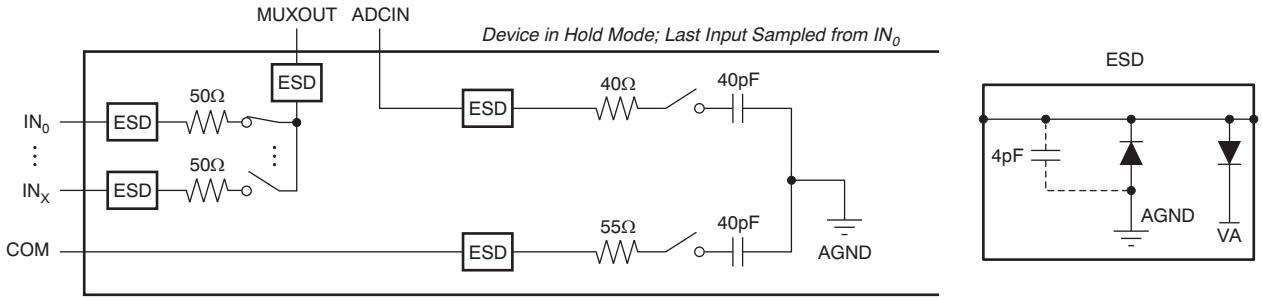

Figure 34. Input Equivalent Circuit

9.3.2.1 Driver Amplifier Choice

To take advantage of the high sample rate offered by the ADS833x, the analog inputs to the converter should be driven with low-noise operational amplifiers (op amps), such as the OPA365, OPA211, OPA827, or THS4031. TI recommends a RC filter at each of the input channels to low-pass filter noise generated by the input driving sources. These channels can accept unipolar signals with voltages between IN_X and COM in the range of 0 V to V_{REF}. If RC filters are not used between the op amps and the input channels, the minimum –3-dB bandwidth required by the driving op amps for the sampled signals to settle to within 1/2 LSB of the final voltage can be calculated using Equation 1:

$$f_{-3dB} \geq \frac{(n + 1) \times \ln(2)}{2\pi \times t_{SAMPLE_MIN}} \quad (1)$$

where

- n = resolution of the converter (n = 16 for the ADS833x).
- t_{SAMPLE_MIN} = minimum acquisition time.

The minimum value of t_{SAMPLE} in *Electrical Characteristics: VA = 2.7 V* and *Electrical Characteristics: VA = 5 V* is 238 ns (3 CCLKs with the internal oscillator at 12.6 MHz). Substituting these values for n and t_{SAMPLE_MIN} into Equation 1 shows $f_{-3\ dB}$ must be at least 7.9 MHz. This bandwidth can be relaxed if the acquisition time is increased or an RC filter is added between the driving operational amplifier and the corresponding input channel (see Texas Instruments' Application Report, *Determining Minimum Acquisition Times for SAR ADCs When a Step Function is Applied to the Input* (SBAA173) and associated references for additional information, available for download at www.ti.com). The OPA365 used in the source-follower (unity-gain) configuration is shown in Figure 35 with recommended values for the RC filter.

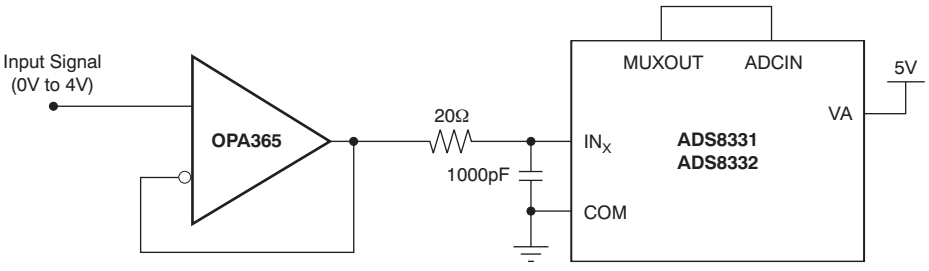

Figure 35. Unipolar Input Drive Configuration

Feature Description (continued)

9.3.2.2 Bipolar to Unipolar Driver

In systems where the input signal is bipolar, op amps such as the OPA365 and OPA211 can be used in the inverting configuration with a DC bias applied to the noninverting input to keep the input signal to the ADS833x within its rated operating voltage range. TI also recommends this configuration when the ADS833x is used in signal-processing applications where good SNR and THD performance is required. The DC bias can be derived from low-noise reference voltage ICs such as the REF5025 or REF5040. The input configuration shown in Figure 36 is capable of delivering better than 91-dB SNR and –99-dB THD at an input frequency of 1 kHz. If bandpass filters are used to filter the input to the driving operational amplifier, the signal swing at the input of the bandpass filter should be small enough to minimize the distortion introduced by the filter. In these cases, the gain of the circuit shown in Figure 36 can be increased to maintain a large enough input signal to the ADS833x to keep the system SNR as high as possible.

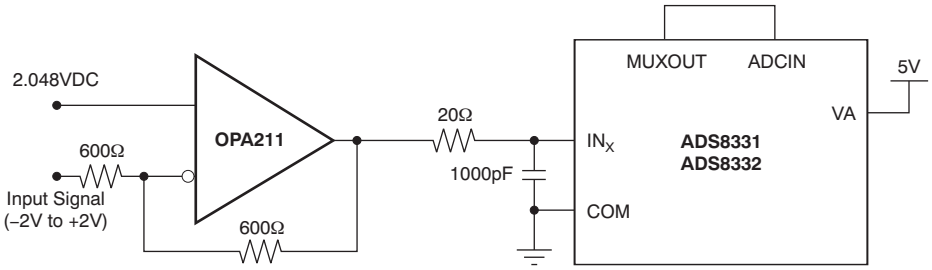

Figure 36. Bipolar Input Drive Configuration

9.4 Device Functional Modes

9.4.1 Reference

The ADS833x can operate with an external reference with a range from 1.2 V to 4.2 V. A clean, low-noise reference voltage on this pin is required to ensure good converter performance. A low-noise band-gap reference such as the REF5025 or REF5040 can be used to drive this pin. A 10-μF ceramic bypass capacitor is required between the REF+ and REF– pins of the converter. This capacitor should be placed as close as possible to the pins of the device. The REF– pin should not be connected to the AGND pin of the converter; instead, the REF– pin must be connected to the analog ground plane with a separate via.

9.4.2 Converter Operation

The ADS833x has an internal oscillator that can be used as the conversion clock (CCLK) source. The minimum frequency of this oscillator is 10.5 MHz. The internal oscillator is only active during the conversion period unless the converter is using Auto-Trigger or Auto-NAP modes. The minimum acquisition, sampling time for the ADS833x is 3 CCLKs (250 ns with a 12-MHz conversion clock), while the minimum conversion time is 18 CCLKs (1500 ns with a 12-MHz conversion clock).

As shown in Figure 37, the ADS833x can also be programmed to run conversions using the external serial clock (SCLK). This feature allows system designers to achieve system synchronization. Each rising edge of SCLK toggles the state of the conversion clock (CCLK), which reduces the frequency of SCLK by a factor of two before it is used as CCLK. For example, a 21-MHz SCLK provides a 10.5-MHz CCLK. If the start of a conversion must occur on a specific rising edge of SCLK when the external serial clock is used for the conversion clock (and Manual-Trigger mode is enabled), a minimum setup time of 20 ns between the falling edge of $\overline{\text{CONVST}}$ and the rising edge of SCLK must be met. This timing ensures the conversion is completed in 18 CCLKs (36 SCLKs).

The duty cycle of SCLK is not critical, as long as the minimum high and low times (11 ns for VA = 5 V) are satisfied. Because the ADS833x is designed for high-speed applications, a high-frequency serial clock must be supplied to maintain the high throughput of the interface. This requirement can be accomplished if the period of SCLK is at most 1 μs when SCLK is used as the conversion clock (CCLK). The 1-μs maximum period for SCLK is also set by the leakage of charge from the capacitors in the capacitive digital-to-analog converter (CDAC) block in the ADS833x. If SCLK is used as the conversion clock, the SCLK source must have minimal rise, fall times and low jitter to provide the best converter performance.

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Device Functional Modes (continued)

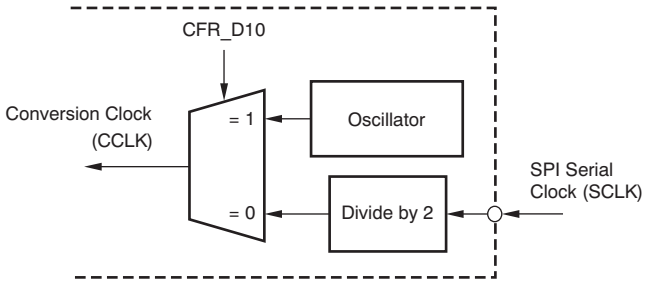

Figure 37. Conversion Clock Source

9.4.2.1 Manual Channel Select Mode

Manual Channel Select mode is enabled through the Configuration register (CFR) by setting the CFR_D11 bit to 0 (see Table 5). The acquisition process starts with selecting an input channel. This selection is done by writing the desired channel number to the Command register (CMR); see Table 4 for further details. The associated timing diagram is shown in Figure 38.

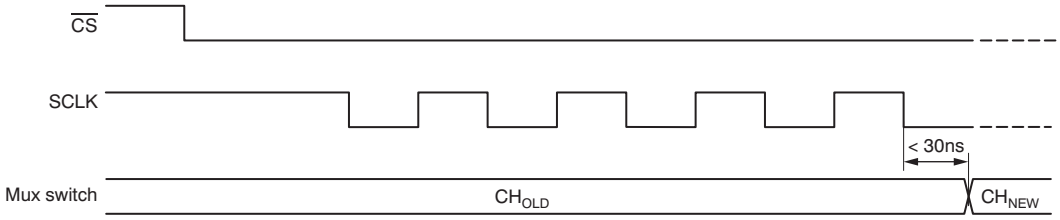

Figure 38. Manual Channel Select Timing

9.4.2.2 Auto Channel Select Mode

Channel selection can also be done automatically if Auto Channel Select mode (default) is enabled (CFR_D11 = 1). If the device is programmed for Auto Channel Select mode, then signals from all channels are acquired in a fixed order. In Auto Channel Select mode, the first conversion after entering this mode is always from the channel of the last conversion completed before this mode is enabled. The channels are then sequentially scanned up to and including the last channel (that is, channel 3 for the ADS8331 and channel 7 for the ADS8332) and then back to the channel that started the sequence. For example, if the last channel used in the conversion before enabling Auto Channel Select mode was channel 2, the sequence for the ADS8332 would be: 2, 3, 4, 5, 6, 7, 2, and so forth, as shown in Figure 39. If the last channel in Manual Channel Select mode happened to be channel 7, the sequence would be: 7, 7, 7, and so forth. Figure 40 shows when the next channel in the sequence activates during Auto Channel Select mode. This timing allows the next channel to settle before it is acquired. This automatic sequencing stops the cycle after CFR_D11 is set to 0.

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Device Functional Modes (continued)

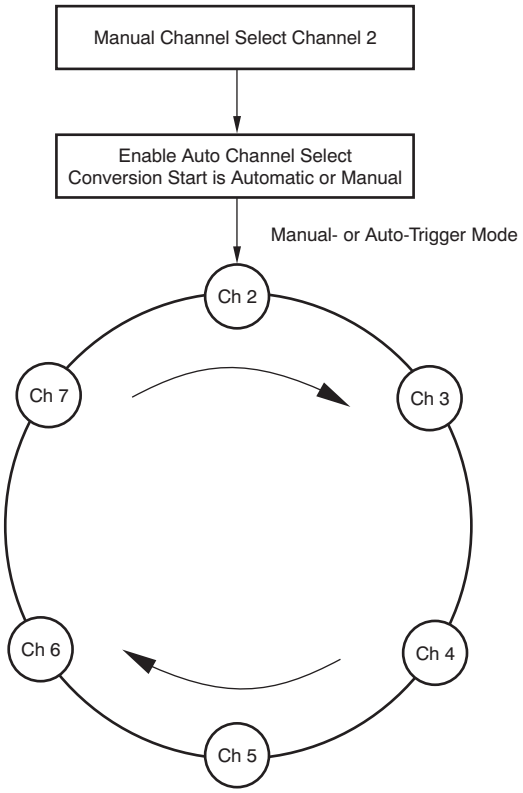

Figure 39. Auto Channel Select for the ADS8332

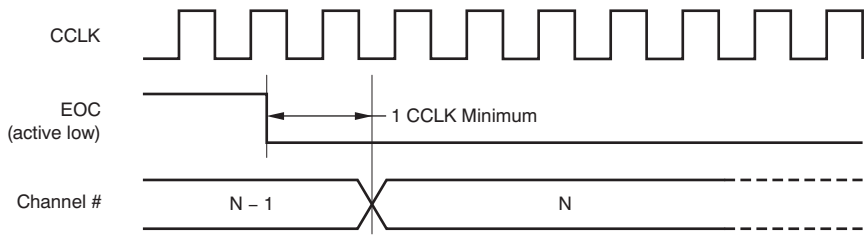

Figure 40. Channel-Number Update in Auto Channel Select Mode Timing

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Device Functional Modes (continued)

9.4.2.3 Start of a Conversion

The end of acquisition is the same as the start of a conversion. This process is initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 40 ns. After the minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high. $\overline{\text{CONVST}}$ acts independently of FS/$\overline{\text{CS}}$ so it is possible to use one common $\overline{\text{CONVST}}$ for applications that require simultaneous sample/hold with multiple converters. The ADS833x switches from sample to hold mode on the falling edge of the $\overline{\text{CONVST}}$ signal. The ADS833x requires 18 conversion clock (CCLK) cycles to complete a conversion. The conversion time is equivalent to 1500 ns with a 12-MHz internal clock. The minimum time between two consecutive $\overline{\text{CONVST}}$ signals is 21 CCLKs.

A conversion can also be initiated without using $\overline{\text{CONVST}}$ if the ADS833x is programmed for Auto-Trigger mode (CFR_D9 = 0). When the converter is configured in this mode, and with CFR_D8 = 0, the next conversion is automatically started three conversion clocks (CCLK) after the end of a conversion. These three conversion clocks (CCLK) are used for the acquisition time. In this case, the time to complete one acquisition and conversion cycle is 21 CCLKs. Table 1 summarizes the different conversion modes.

Table 1. Different Types of Conversion

MODE	SELECT CHANNEL	START CONVERSION
Automatic	**Auto Channel Select**(1)	**Auto-Trigger Mode**
	No need to write channel number to CMR. Use internal sequencer for ADS833x.	Start a conversion based on conversion clock CCLK
Manual	**Manual Channel Select**	**Manual-Trigger Mode**
	Write channel number to CMR	Start a conversion with $\overline{\text{CONVST}}$

(1) Auto channel select should be used with Auto-Trigger mode and TAG bit output enabled.

Manual Channel select with Auto-Trigger mode enabled is generally used when continuous conversions from a single channel are desired. In this mode, cycling the input mux to change the channel requires that conversions are halted by setting the converter to Manual-Trigger mode. When the proper input channel is selected, the converter can be placed back to Auto-Trigger mode to continue continuous conversions from the new channel.

9.4.2.4 Status Output Pin (EOC/$\overline{\text{INT}}$)

The status output pin is programmable. It can be used as an EOC output (CFR_D[7:6] = 11) where the low time is equal to the conversion time. When the status pin is programmed as EOC and the polarity is set as active low, the pin works in the following manner: the EOC output goes low immediately following $\overline{\text{CONVST}}$ going low with Manual-Trigger mode enabled. EOC stays low throughout the conversion process and returns high when the conversion has ended. If Auto-Trigger mode is enabled, the EOC output remains high for three conversion clocks (CCLK) after the previous rising edge of EOC.

This status pin can also be used as an interrupt output, $\overline{\text{INT}}$ (CFR_D[7:6] = 10), which is set low at the end of a conversion, and is brought high (cleared) by the next read cycle. The polarity of this pin, whether used as EOC or $\overline{\text{INT}}$, is programmable through the CFR_D7 bit.

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9.4.2.5 Power-Down Modes and Acquisition Time

There are three power-down modes that reduce power dissipation: Nap, Deep, and Auto-NAP. The first two, Nap and Deep Power-Down modes, are enabled or disabled by bits CFR_D3 and CFR_D2, respectively, in the Configuration register (see Table 5 for details).

Deep Power-Down mode provides maximum power savings. When this mode is enabled, the analog core in the converter is shut down, and the analog supply current falls from 6.6 mA (VA = 5 V) to 1 μA in 2 μs. The wake-up time from Deep Power-Down mode is 1 μs. The device can wake up from Deep Power-Down mode by either disabling this mode, issuing the wake-up command, loading the default value into the CFR, or performing a reset (either with the software reset command, CFR_D0 bit, or the external reset). See Table 4 and Table 5 along with the *Reset Function* section for further information.

In Nap Power-Down mode, the bias currents for the analog core of the device are significantly reduced. Because the bias currents are not completely shut off, the ADS833x can wake up from this power-down mode much faster than from Deep Power-Down mode. After Nap Power-Down mode is enabled, the analog supply current falls from 6.6 mA (VA = 5 V) to 0.39 mA in 200 ns. The wake-up time from this mode is three conversion clock cycles (CCLK). The device can wake up from Nap Power-Down mode in the same manner as waking up from Deep Power-Down mode.

The third power-down mode, Auto-NAP, is enabled or disabled by bit CFR_D4 in the Configuration register (see Table 5 for details). Once this mode is enabled, the device is controlled by the digital core logic on the chip. The device is automatically placed into Nap Power-Down mode after the next end of conversion (EOC). The analog supply current falls from 6.6mA (VA = 5 V) to 0.39 mA in 200 ns. A conversion start wakes up the device in three conversion clock cycles. Issuing the wake-up command, loading the default value into the CFR, disabling Auto-NAP Power-Down mode, issuing a manual channel select command, or resetting the device can wake the ADS833x from Auto-NAP Power-Down mode. A comparison of the three power-down modes is listed in Table 2.

Table 2. Comparison of Power-Down Modes

TYPE OF POWER-DOWN	POWER CONSUMPTION (VA = 5 V)	POWER-DOWN BY:	POWER-DOWN TIME	WAKEUP BY:	WAKE-UP TIME	ENABLE
Normal operation	6.6 mA	—	—	—	—	—
Deep power-down	1 μA	Setting CFR_D2	2 μs	Wakeup command 1011b	1 μs	Set CFR_D2
Nap power-down	0.39 mA	Setting CFR_D3	200 ns	Wakeup command 1011b	3 CCLKs	Set CFR_D3
Auto-NAP power-down	0.39 mA	EOC (end of conversion)	200 ns	$\overline{\text{CONVST}}$, any channel select command, default command 1111b, or wakeup command 1011b.	3 CCLKs	Set CFR_D4

The default acquisition time is three conversion clock (CCLK) cycles. Figure 41 shows the timing diagram for $\overline{\text{CONVST}}$, EOC, and Auto-NAP power-down signals in Manual-Trigger mode. As shown in the diagram, the device wakes up after a conversion is triggered by the $\overline{\text{CONVST}}$ pin going low. However, a conversion is not yet started at this time. The conversion start signal to the analog core of the chip is internally generated no less than six conversion clock (CCLK) cycles later, to allow at least three CCLKs for wake up and three CCLKs for acquisition. The ADS833x enters Nap Power-Down mode one conversion cycle after the end of conversion (EOC).

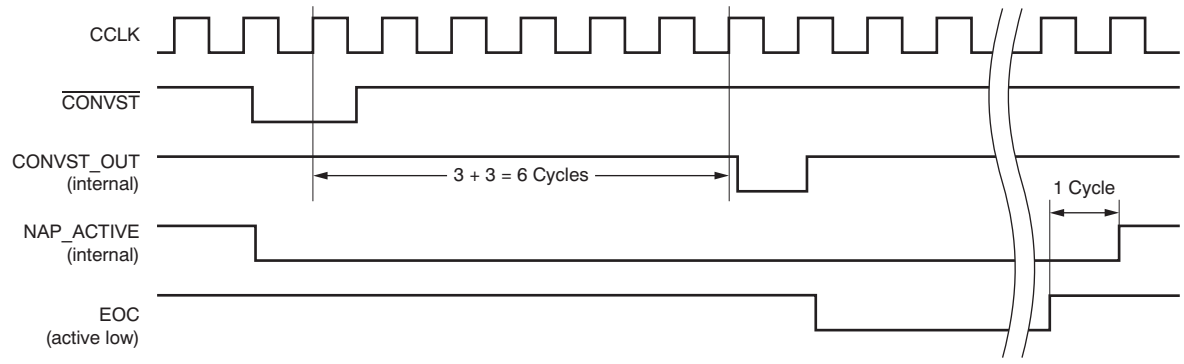

Figure 41. Timing for $\overline{\text{CONVST}}$, EOC, and Auto-NAP Power-Down Signals in Manual-Trigger Mode (Three Conversion Clock Cycles for Acquisition)

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The ADS833x can support sampling rates of up to 500 kSPS in Auto-Trigger mode. This rate is selectable by programming the CFR_D8 bit in the Configuration register. In 500-kSPS mode, consecutive conversion start pulses to the analog core are generated 21 conversion clock cycles apart. In 250-kSPS mode, consecutive conversion-start pulses are 42 conversion clock cycles apart. The Nap and Deep Power-Down modes are available with either sampling rate; however, Auto-NAP mode is available only with a sampling rate of 250 kSPS when Auto-Trigger mode is enabled. The analog core cannot be powered down when the Auto-NAP mode sampling rate is 500 kSPS because at that rate, there is no period of time when the analog core is not actively being used.

Figure 42 shows the timing diagram for conversion start and Auto-NAP power-down signals for a 250-kSPS sampling rate in Auto-Trigger mode. For a 16-bit ADC output word, consecutive new conversion start pulses are generated 2 × (18 + 3) cycles apart. NAP_ACTIVE (the signal to power down the analog core in Nap and Auto-NAP modes) goes low six (3 + 3) conversion clock cycles before the conversion start falling edge, thus powering up the analog core. It takes three conversion clock cycles after NAP_ACTIVE goes low to power up the analog core. The analog core is powered down a cycle after the end of a conversion. For a 16-bit ADC with a 500-kSPS sampling rate and three conversion clock cycle sampling, consecutive conversion start pulses are generated 21 conversion clock cycles apart.

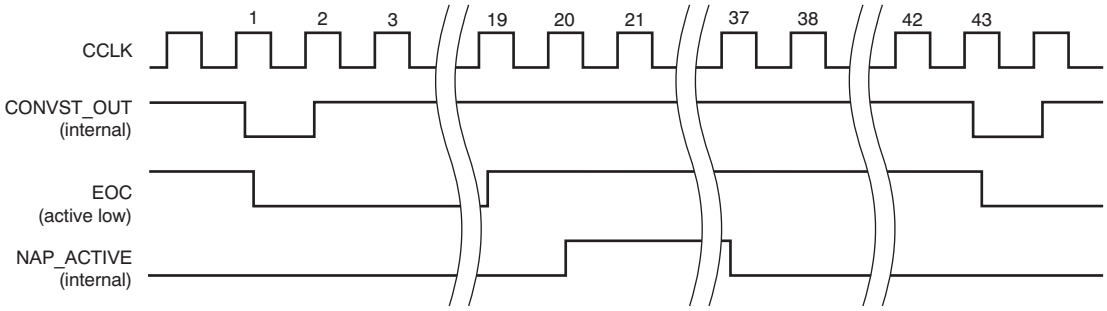

Figure 42. Timing for Conversion Start and Auto-NAP Power-Down Signals in Auto-Trigger Mode (250-kSPS Sampling and Three Conversion Clock Cycles for Acquisition)

Timing diagrams for reading from the ADS833x with various trigger and power-down modes are shown in Figure 43 through Figure 45. The total (acquisition + conversion) times for the different trigger and power-down modes are listed in Table 3.

Table 3. Total Acquisition + Conversion Times

MODE	ACQUISITION + CONVERSION TIME
Auto-Trigger at 500 kSPS	= 21 CCLK
Manual-Trigger	≥ 21 CCLK
Manual-Trigger with Deep Power Down	≥ 4 SCLK + 1 μs + 3 CCLK + 18 CCLK + 16 SCLK + 2 μs
Manual-Trigger with Nap Power Down	≥ 4 SCLK + 3 CCLK + 3 CCLK + 18 CCLK + 16 SCLK + 200 ns
Manual-Trigger with Auto-NAP Power Down	≥ 4 SCLK + 3 CCLK + 3 CCLK + 18 CCLK + 1 CCLK + 200 ns (using wakeup to resume)
	≥ 3 CCLK + 3 CCLK + 18 CCLK + 1 CCLK + 200 ns (using $\overline{\text{CONVST}}$ to resume)

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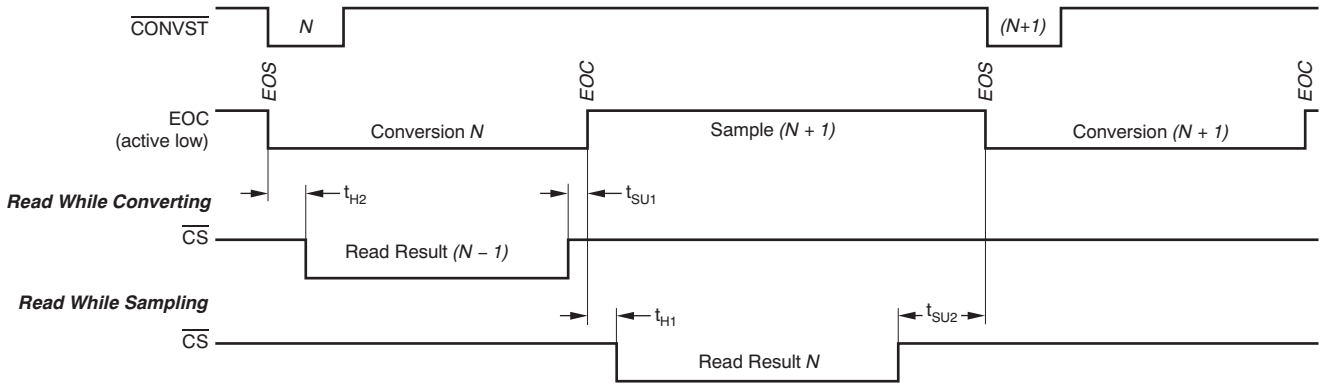
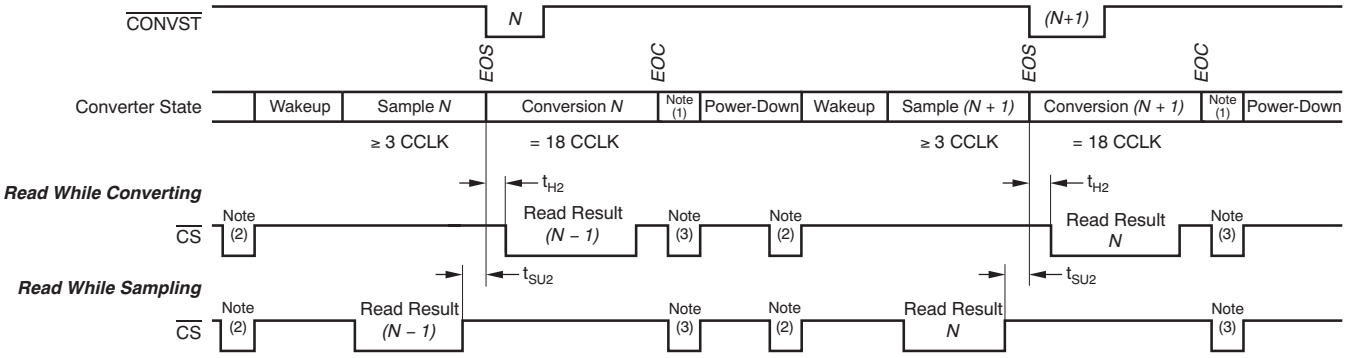


Figure 43. Read While Converting vs Read While Sampling (Manual-Trigger Mode)



(1) Converter is in acquisition mode between end of conversion and activation of Nap or Deep Power-Down mode.

(2) Command on SDI pin to wake-up converter (minimum of four SCLKs).

(3) Command on SDI pin to place converter into Nap or Deep Power-Down mode (minimum of 16 SCLKs).

Figure 44. Read While Converting vs Read While Sampling With Nap or Deep Power Down (Manual-Trigger Mode)

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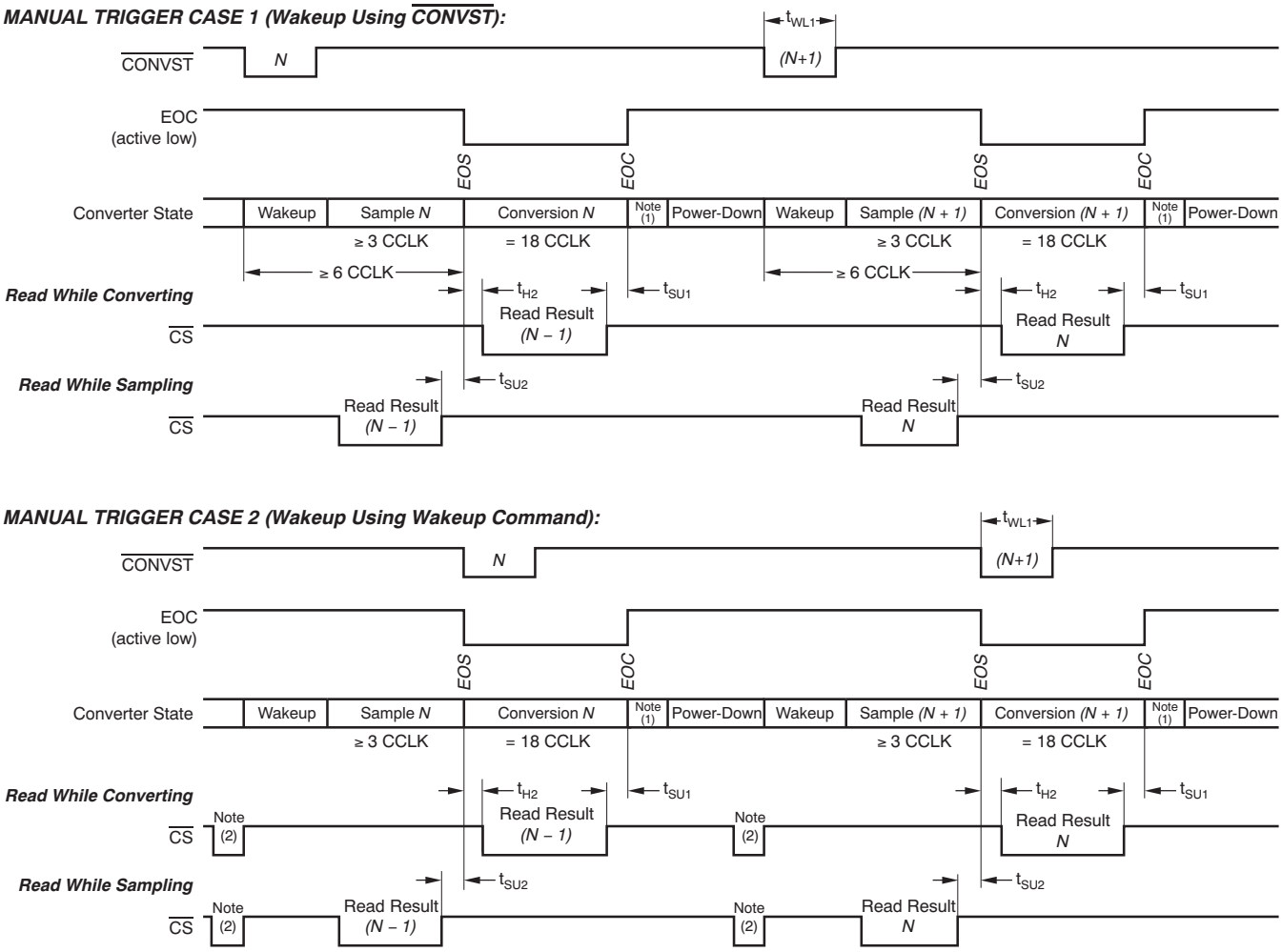

(1) Time between end of conversion and Nap Power Down mode is 1 CCLK.

(2) Command on SDI to wake-up converter (minimum of four SCLKs).

Figure 45. Read While Converting vs Read While Sampling With Auto-NAP Power Down

9.5 Programming

9.5.1 Digital Interface

The serial interface is designed to accommodate the latest high-speed processors with an SCLK frequency of up to 40 MHz (VA = VBD = 5 V). Each cycle starts with the falling edge of FS/$\overline{CS}$. The internal data register content, which is made available to the output register at the end of conversion, is presented on the SDO output pin on the falling edge of FS/$\overline{CS}$. The first bit is the most significant bit (MSB). The output data bits are valid on the falling edge of SCLK with the t_{D2} delay (see the *Timing Requirements: VA = 2.7 V* and *Timing Characteristics: VA = 5 V*) so that the host processor can read the data on the falling edge. Serial data input is also read on the falling edge of SCLK.

The complete serial I/O cycle starts after the falling edge of FS/$\overline{CS}$ and ends 16 falling edges of SCLK later (see NOTE). The serial interface works with CPOL = 1, CPHA = 0. This setting means the falling edge of FS/$\overline{CS}$ may fall while SCLK is high. The same timing relaxation applies to the rising edge of FS/$\overline{CS}$ where SCLK may be high or low as long as the last SCLK falling edge happens before the rising edge of FS/$\overline{CS}$.

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Programming (continued)

NOTE

There are cases where a cycle can be anywhere from 4 SCLKs up to 24 SCLKs, depending on the read mode combination. See Table 4 for details.

9.5.1.1 Internal Register

The internal register consists of two parts: four bits for the Command register (CMR) and 12 bits for the Configuration register (CFR).

Table 4. Command Set Defined by Command Register (CMR)(1)

D[15:12]	HEX	COMMAND	D[11:0]	WAKE UP FROM AUTO-NAP	MINIMUM SCLKs REQUIRED	R/W
0000b	0h	Select analog input channel 0	Don't care	Y	4	W
0001b	1h	Select analog input channel 1	Don't care	Y	4	W
0010b	2h	Select analog input channel 2	Don't care	Y	4	W
0011b	3h	Select analog input channel 3	Don't care	Y	4	W
0100b	4h	Select analog input channel 4(2)	Don't care	Y	4	W
0101b	5h	Select analog input channel 5(2)	Don't care	Y	4	W
0110b	6h	Select analog input channel 6(2)	Don't care	Y	4	W
0111b	7h	Select analog input channel 7(2)	Don't care	Y	4	W
1000b	8h	Reserved	Reserved	—	—	—
1001b	9h	Reserved	Reserved	—	—	—
1010b	Ah	Reserved	Reserved	—	—	—
1011b	Bh	Wake up	Don't care	Y	4	W
1100b	Ch	Read CFR	Don't care	—	16	R
1101b	Dh	Read data	Don't care	—	16	R
1110b	Eh	Write CFR	CFR Value	—	16	W
1111b	Fh	Default mode (load CFR with default value)	Don't care	Y	4	W

(1) The first four bits from SDO after the falling edge of FS/$\overline{CS}$ are the four MSBs from the previous conversion result. The next 12 bits from SDO are the contents of the CFR.
(2) These commands apply only to the ADS8332; they are reserved (not available) for the ADS8331.

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9.5.2 Writing to the Converter

There are two different types of writes to the register: a 4-bit write to the CMR and a full 16-bit write to the CMR plus CFR. The command set is listed in Table 4 and the configuration register map is listed in Table 5. A simple command requires only four SCLKs; the write takes effect on the fourth falling edge of SCLK. A 16-bit write or read takes at least 16 SCLKs (see Table 7 for exceptions that require more than 16 SCLKs).

9.5.2.1 Configuring the Converter and Default Mode

The converter can be configured with command 1110b (write to the CFR) or command 1111b (default mode). A write to the CFR requires a 4-bit command followed by 12 bits of data. A 4-bit command takes effect on the fourth falling edge of SCLK. A write to the CFR takes effect on the 16th falling edge of SCLK.

The CFR default value for each bit is 1. The default values are applied to the CFR after issuing command 1111b or when the device is reset with a power-on reset (POR), software reset, or external reset using the $\overline{\text{RESET}}$ pin (see the *Reset Function* section).

The communication protocol of the ADS833x is full duplex. That is, data are transmitted to and from the device simultaneously. For example, the input mux channel can be changed via the SDI pin while data are being read through the SDO pin. All commands, except *Read CFR*, output conversion data on the SDO pin. If a *Read CFR* command is issued, the *Read Data* command can then be used to read back the conversion result.

9.5.3 Reading the Configuration Register

The host processor can read back the value programmed in the CFR by issuing command 1100b. The timing is similar to reading a conversion result except $\overline{\text{CONVST}}$ is not used. There is also no activity on the EOC/$\overline{\text{INT}}$ pin. The CFR value readback contains the first four bits (MSBs) of the previous conversion data plus the 12-bit CFR contents.

Table 5. Configuration Register (CFR) Map

CFR SDI BIT (Default = FFFh)	DEFINITION	BIT = 0	BIT = 1
D11	Channel select mode	Manual channel select enabled. Use channel select commands to access a desired channel.	Auto channel select enabled. Channels are sampled and converted sequentially until the cycle after this bit is set to 0.
D10	Conversion clock (CCLK) source select	Conversion clock (CCLK) = SCLK / 2	Conversion clock (CCLK) = internal OSC
D9	Trigger (conversion start) select: start conversion at the end of sampling (EOS). If D9 = 0 and D8 = 0, the D4 setting is ignored.	Auto-Trigger: conversions automatically start three conversion clocks after EOC at 500 kSPS	Manual-Trigger: conversions manually start on falling edge of $\overline{\text{CONVST}}$
D8	Sample rate for Auto-Trigger mode	500kSPS (21 CCLKs)	250 kSPS (42 CCLKs)
D7	Pin 10 polarity select when used as an output (EOC/$\overline{\text{INT}}$)	EOC/$\overline{\text{INT}}$ active high	EOC/$\overline{\text{INT}}$ active low
D6	Pin 10 function select when used as an output (EOC/$\overline{\text{INT}}$)	Pin used as $\overline{\text{INT}}$	Pin used as EOC
D5	Pin 10 I/O select for daisy-chain mode operation	Pin 10 is used as CDI input (daisy-chain mode enabled)	Pin 10 is used as EOC/$\overline{\text{INT}}$ output
D4	Auto-NAP Power-Down enable or disable. This bit setting is ignored if D9 = 0 and D8 =0.	Auto-NAP Power-Down mode enabled (not activated)	Auto-NAP Power-Down mode disabled
D3	Nap Power Down. This bit is set to 1 automatically by wake-up command.	Nap Power-Down enabled	Nap Power-Down disabled (resume normal operation)
D2	Deep Power Down. This bit is set to 1 automatically by wake-up command.	Deep Power-Down enabled	Deep Power-Down disabled (resume normal operation)
D1	TAG bit output enable	TAG bit output disabled	TAG bit output enabled. TAG bits appear after conversion data
D0	Software reset	System reset, returns to 1 automatically	Normal operation

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9.5.4 Reading the Conversion Result

The conversion result is available to the input of the output data register (ODR) at EOC and presented to the output of the output register at the next falling edge of FS/$\overline{CS}$. The host processor can then shift the data out through the SDO pin at any time except during the quiet zone. This duration is 20 ns before and 20 ns after the end of sampling (EOS) period. End of sampling (EOS) is defined as the falling edge of $\overline{CONVST}$ when Manual-Trigger mode is used or the end of the third conversion clock (CCLK) after EOC if Auto-Trigger mode is used.

The falling edge of FS/$\overline{CS}$ should not be placed at the precise moment at the end of a conversion (by default when EOC goes high). Otherwise, the data could be corrupt. If FS/$\overline{CS}$ is placed before the end of a conversion, the previous conversion result is read. If FS/$\overline{CS}$ is placed after the end of a conversion, the current conversion result is read.

The conversion result is 16-bit data in straight binary format as shown in Table 6. Generally 16 SCLKs are necessary, but there are exceptions when more than 16 SCLKs are required (see Table 7). Data output from the serial output (SDO) is left-adjusted MSB first. The trailing bits are filled with three TAG bits first (if enabled) plus all 0s. SDO remains low until FS/$\overline{CS}$ is brought high again.

SDO is active when FS/$\overline{CS}$ is low. The rising edge of FS/$\overline{CS}$ 3-states the SDO output.

NOTE

Whenever SDO is not in 3-state (that is, when FS/$\overline{CS}$ is low and SCLK is running), a portion of the conversion result is output at the SDO pin. The number of bits depends on how many SCLKs are supplied. For example, a manual channel select command cycle requires 4 SCLKs. Therefore, four MSBs of the conversion result are output at SDO. The exception is when SDO outputs all 1s during the cycle immediately after any reset (POR, software reset, or external reset).

If SCLK is used as the conversion clock (CCLK) and a continuous SCLK is used, it is not possible to clock out all 16 bits from SDO during the sampling time (6 SCLKs) because of the quiet zone requirement. In this case, it is better to read the conversion result during the conversion time (36 SCLKs or 48 SCLKs in Auto-NAP mode).

Table 6. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
Full-scale range	V_{REF}	—	—
Least significant bit (LSB)	V_{REF} / 65536	—	—
Full-scale	V_{REF} – 1 LSB	1111 1111 1111 1111	FFFF
Midscale	V_{REF} / 2	1000 0000 0000 0000	8000
Midscale – 1 LSB	V_{REF} / 2– 1 LSB	0111 1111 1111 1111	7FFF
Zero	0 V	0000 0000 0000 0000	0000

9.5.4.1 TAG Mode

The ADS833x includes a TAG feature that can be used to indicate which channel sourced the converted result. If TAG mode is enabled, three address bits are added after the LSB of the conversion data is read out from SDO to indicate which channel corresponds to the result. These address bits are 000 for channel 0, 001 for channel 1, 010 for channel 2, 011 for channel 3, 100 for channel 4, 101 for channel 5, 110 for channel 6, and 111 for channel 7. The converter requires at least 19 SCLKs when TAG mode is enabled to transfer the 16-bit conversion result and the three TAG bits.

9.5.4.2 Daisy-Chain Mode

The ADS833x can operate as a single converter or in a system with multiple converters. System designers can take advantage of the simple, high-speed, SPI-compatible serial interface by cascading converters in a single chain when multiple converters are used. The CFR_D5 bit in the Configuration register is used to reconfigure the EOC/$\overline{INT}$ status pin as the chain data input (CDI) pin, a secondary serial data input, for the conversion result from an upstream converter. This configuration is called *daisy-chain mode* operation. A typical connection of three converters in daisy-chain mode is shown in Figure 46.

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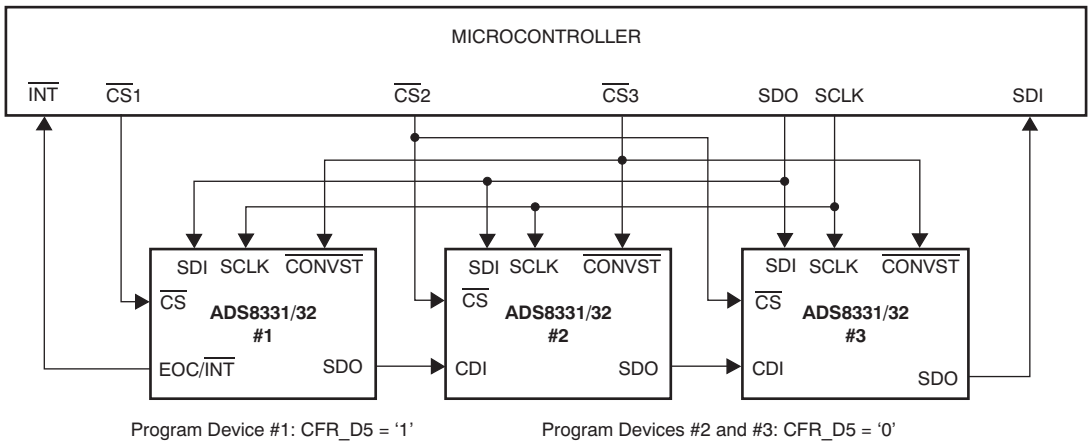

Figure 46. Multiple Converters Connected Using Daisy-Chain Mode

When multiple converters are used in daisy-chain mode, the first converter is configured in regular mode while the rest of the converters downstream are configured in daisy-chain mode. When a converter is configured in daisy-chain mode, the CDI input data go straight to the output register. Therefore, the serial input data passes through the converter with either a 16 SCLK (if the TAG feature is disabled) or 24-SCLK delay, as long as $\overline{CS}$ is active. See Figure 47 for detailed timing. In this timing diagram, the conversion in each converter is performed simultaneously.

Manual Trigger, Read While Sampling
(Use internal CCLK, EOC active low, and TAG mode disabled)

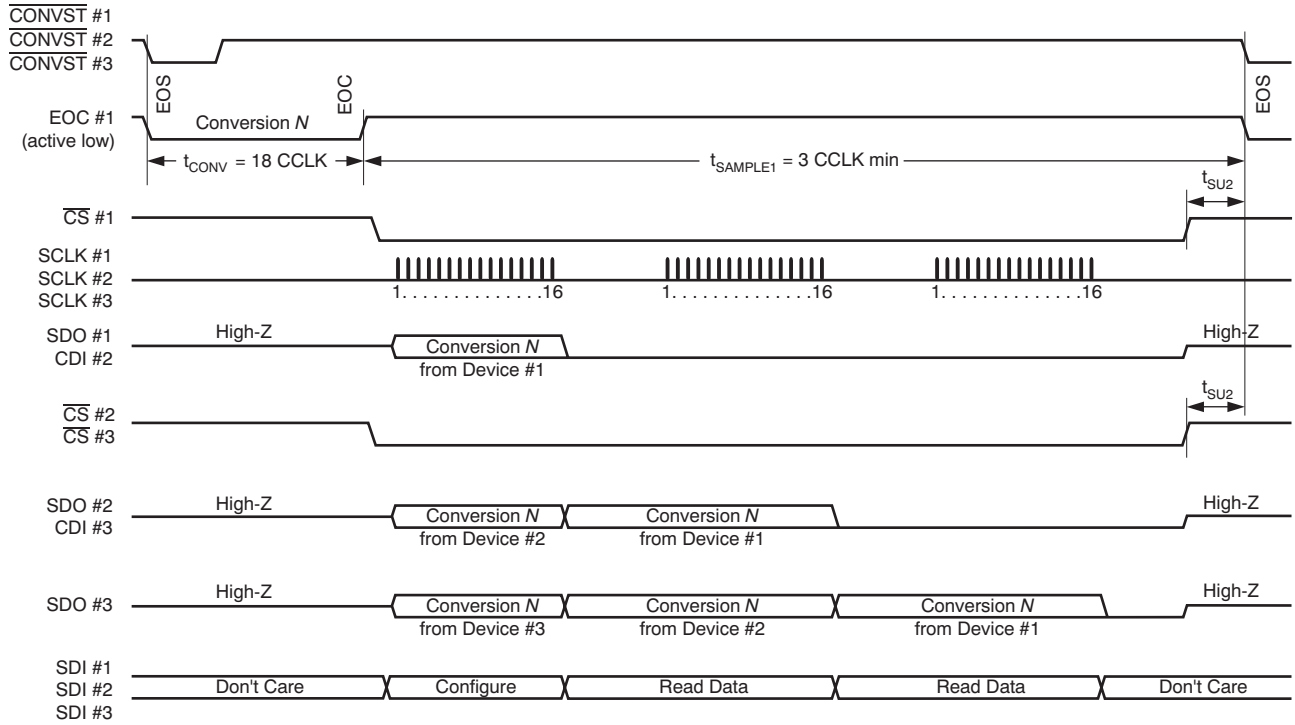

Figure 47. Simplified Dasiy-Chain Mode Timing With Shared $\overline{CONVST}$ and Continuous $\overline{CS}$

The multiple $\overline{CS}$ signals must be handled with care when the converters are operating in daisy-chain mode. The different chip select signals must be low for the entire data transfer (in this example, 48 bits for three conversions). The first 16-bit word after the falling chip select is always the data from the chip that received the chip select signal.

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Case 1: If chip select is not toggled ($\overline{CS}$ stays low), the next 16 bits of data are from the upstream converter, and so on. This configuration is shown in Figure 47.

Case 2: If the chip select is toggled during a daisy-chain mode data transfer cycle, as illustrated in Figure 48, the same data from the converter are read out again and again in all three discrete 16-bit cycles. This state is ***not*** a desired result.

Manual Trigger, Read While Sampling
(Use internal CCLK, EOC active low, and TAG mode disabled)

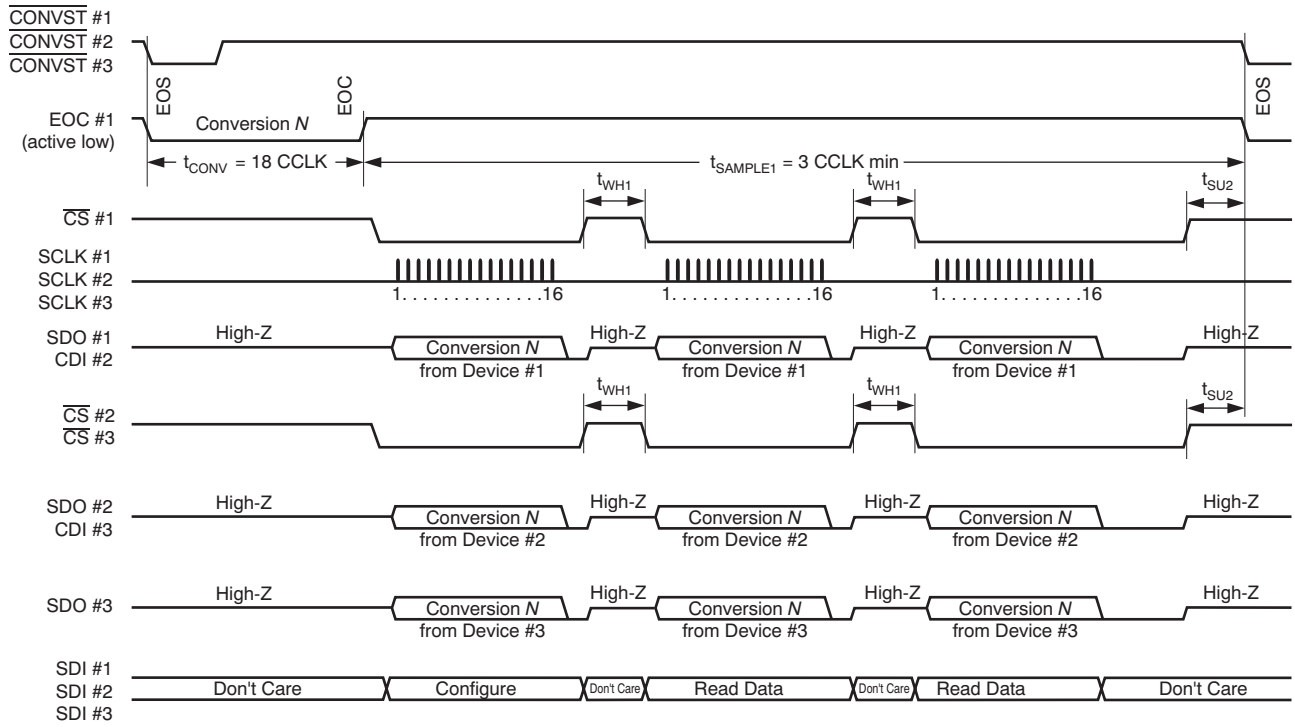

Figure 48. Simplified Daisy-Chain Mode Timing With Shared $\overline{CONVST}$ and Noncontinuous $\overline{CS}$

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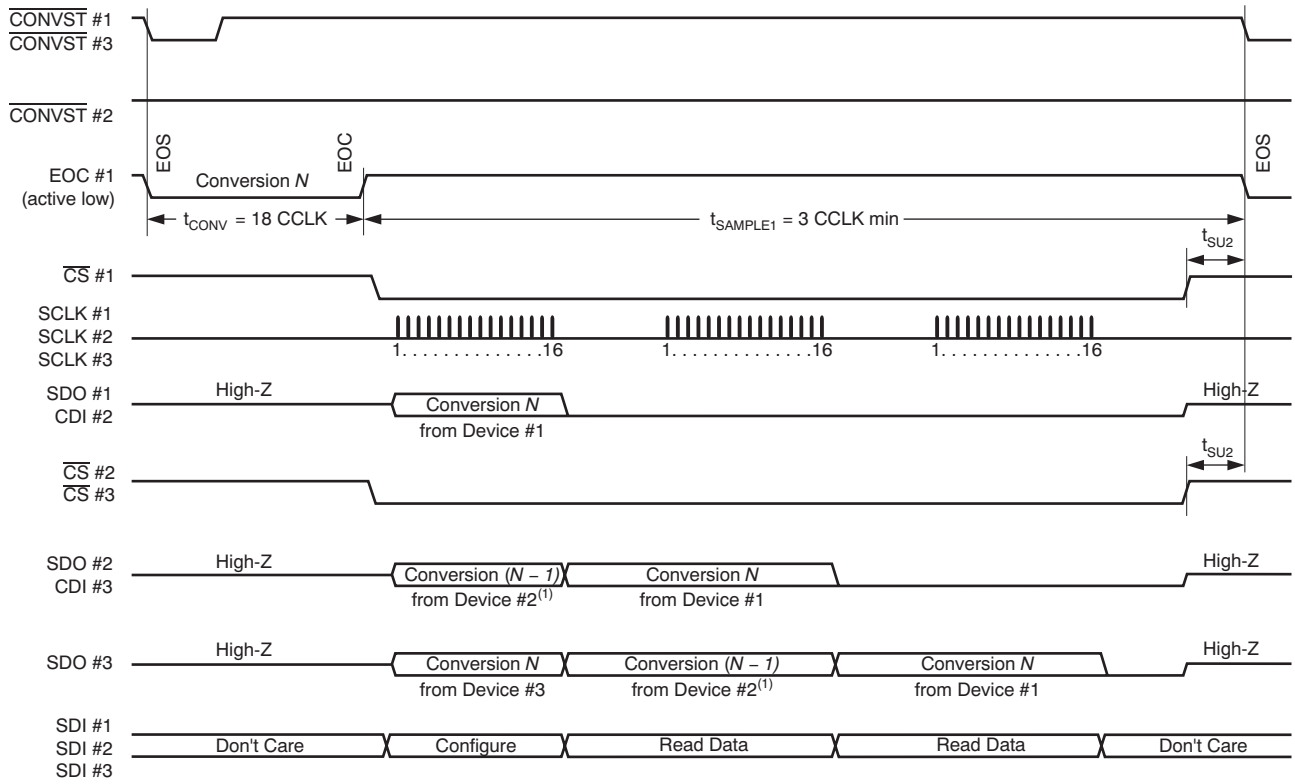
Figure 49 shows a slightly different scenario where $\overline{\text{CONVST}}$ is not shared with the second converter. Converters #1 and #3 have the same $\overline{\text{CONVST}}$ signal. In this case, converter #2 simply passes previous conversion data downstream.

Manual Trigger, Read While Sampling
(Use internal CCLK, EOC active low, and TAG mode disabled)



(1) Data from device #2 is from previous converison.

Figure 49. Simplified Daisy-Chain Mode Timing with Separate $\overline{\text{CONVST}}$ and Continuous $\overline{\text{CS}}$

The number of SCLKs required for a serial read cycle depends on the combination of different read modes, TAG mode, daisy-chain mode, and the manner in which a channel is selected (for example, Auto Channel Select mode). The required number of SCLKs for different readout modes are listed in Table 7.

Table 7. Required SCLKs kor Different Readout Mode Combinations

DAISY-CHAIN MODE CFR_D5	TAG MODE CFR_D1	NUMBER OF SCLK CYCLES PER SPI READ	TRAILING BITS
1	0	16	None
1	1	≥ 19	TAG bits plus up to 5 zeros
0	0	16	None
0	1	24	TAG bits plus 5 zeros

SCLK skew between converters in a daisy-chain configuration can affect the maximum frequency of SCLK. The skew can also be affected by supply voltage and loading. It may be necessary to slow down the SCLK when the devices are configured in daisy-chain mode.

9.5.5 Reset Function

The ADS833x can be reset with three different methods: internal POR, software reset, and external reset using the $\overline{\text{RESET}}$ pin.

The internal POR circuit is activated when power is initially applied to the converter. This internal circuit eliminates the need for commands to be sent to the converter after power on to set the default mode of operation (see the *Power-On Sequence Timing* section for further details).

Software reset can be used to place the converter in the default mode by setting the CFR_D0 bit to 0 in the Configuration register (see Table 5). This bit is automatically returned to 1 (default) after the converter is reset. This reset method is useful in systems that cannot dedicate a separate control signal to the $\overline{\text{RESET}}$ pin. In these situations, the RESET pin must be connected to VBD for the ADS833x to operate properly.

If communication in the system becomes corrupted and a software reset cannot be issued, the $\overline{\text{RESET}}$ pin can be used to reset the device manually. To reset the device and return the device to default mode, this pin must held low for a minimum of 25 ns.

After the ADS833x detects a reset condition, the minimum time before the device can be reconfigured by FS/$\overline{\text{CS}}$ going low and data clocking in on SDI is 2 μs.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The two primary circuits required to optimize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits, and some application circuits designed using these devices.

10.1.1 ADC Reference Driver

The reference source to the ADC must provide low drift, very accurate DC voltage and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise (typically in the order of a few 100 μV_{RMS}) of the reference source must be appropriately filtered by using a low pass filter with a cut-off frequency of a few hundred hertz. After band-limiting the noise from the reference source, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. At the start of each conversion, the reference buffer must regulate the voltage of the reference pin within 1 LSB of the intended value. This condition necessitates the use of a large 22-µF bypass capacitor at the reference pin of the ADC. The amplifier selected to drive the reference input pin must be stable while driving this large capacitor and should have low output impedance, low offset, and temperature drift specifications.

10.1.1.1 Reference Driver Circuit for V_{REF} = 4.096 V

The application circuit in Figure 50 shows the schematic of a complete reference driver circuit that generates a voltage of 4.096-V DC using a single 5-V supply. This circuit is suitable to drive the reference of the ADS8332 at the maximum throughput of 500 kSPS. The reference voltage of 4.096 V in this design is generated by the low-power, low drift, low-power REF2041 circuit. The output broadband noise of the reference is filtered by a low-pass filter with a 3-dB cutoff frequency of 159 Hz.

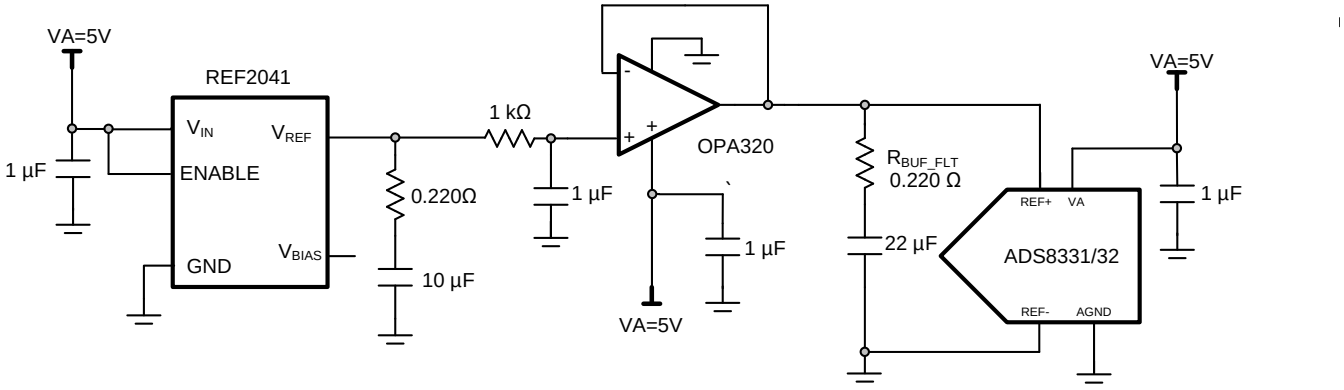

Figure 50. Reference Driver Schematic for VA = 5 V, V_{REF} = 4.096 V

The OPA320 is a precision, high bandwidth (20 MHz), low-noise (7 nV / $\sqrt{Hz}$) operational amplifier. The low-noise, and low power consumption of this amplifier makes the OPA320 a good choice to drive the reference input of the ADS833x. The REF+ input is bypassed with a 22-µF bypass capacitor. The 22-µF reference bypass capacitor is high enough to make the OPA320 amplifier unstable, therefore a small resistor (R_{BUF_FLT}) is required to isolate the amplifier output and improve stability. The value of R_{BUF_FLT} is dependent on the output impedance

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Application Information (continued)

of the driving amplifier as well as the circuit frequency response. Typical values of R_{BUF_FLT} range from 0.1 Ω to 2 Ω and the exact value can be found by using SPICE simulations. In the case of the OPA320 in the reference driver example in Figure 50, the value of R_{BUF_FLT} is 220 mΩ providing >55° of phase margin while driving the 22-µF bypass capacitor. It should be noted that higher values of R_{BUF_FLT} cause high voltage spikes at the reference pin which affects the conversion accuracy.

10.1.1.2 Reference Driver Circuit for V_{REF}=2.5 V, VA=2.7 V

The circuit shown in Figure 51 can be used to generate a 3-V reference using a 3.3-V supply. This circuit is suitable to drive the reference of the ADS8332 at the maximum throughput of 500 kSPS. The reference voltage of 3 V in this design is generated by the low-power, low drift, REF2025. The output broadband noise of the reference is filtered by a low-pass filter with a 3-dB cutoff frequency of 159 Hz.

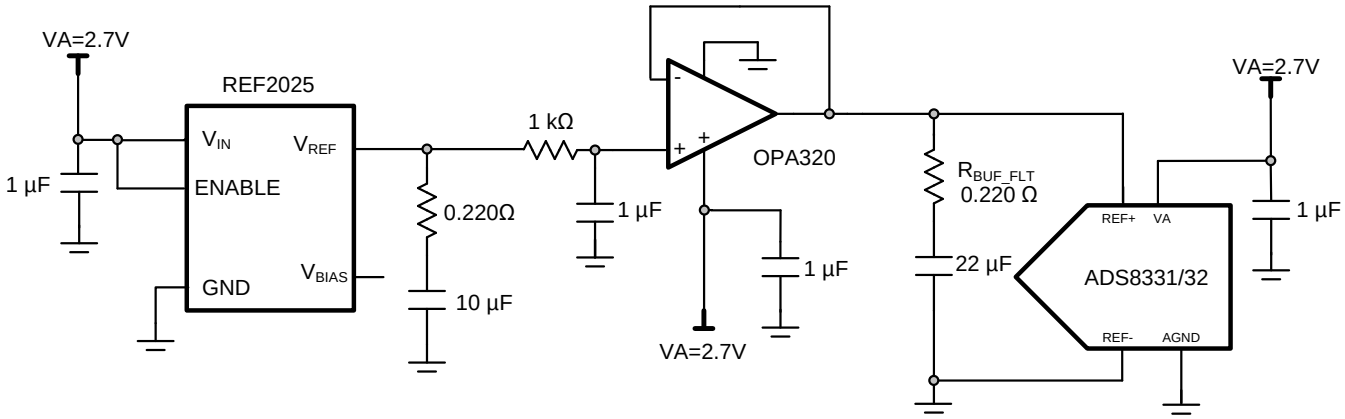

Figure 51. Reference Driver Schematic for VA = 2.7 V, V_{REF} = 2.5 V

10.1.2 ADC Input Driver

To take advantage of the high sample rate offered by the ADS833x, the analog inputs (INx) of the device should be driven with low noise operational amplifiers. The optimal input driver circuit for a high precision SAR ADC consists of a driving amplifier and a fly-wheel RC filter. The amplifier driving the ADC must have low output impedance and be able to charge the internal sampling capacitor (45pF) to a 16-bit settling level within the minimum acquisition time. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and helps to reduce the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

10.1.2.1 Input Amplifier Selection

The selection criteria for the input driver amplifier is dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- **Small-signal bandwidth**: Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. To maintain the overall stability of the input driver circuit, the amplifier bandwidth should be selected as described in Equation 2:

$$\text{Unity} - \text{GainBandwidth} \geq 4 \times \left(\frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \right) \quad (2)$$

- **Noise**: Noise contribution of the front-end amplifiers should be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit should be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency RC filter and is calculated by Equation 3:

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Application Information (continued)

$$NG \times \sqrt{\left(\frac{V_{1/f_AMP_PP}}{6.6}\right)^2 + e_{n_REF_RMS}^2 \times \frac{\pi}{2} \times f_{REF_3dB}} \le \frac{1}{3} \times \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\frac{SNR(dB)}{20}}$$

where

- $V_{1\ /\ f_AMP_PP}$ is the peak-to-peak flicker noise in µV
- e_{n_RMS} is the amplifier broadband noise density in nV / $\sqrt{Hz}$
- f_{-3dB} is the 3-dB bandwidth of the RC filter
- NG is the noise gain of the front-end circuit, which is equal to 1 in a buffer configuration (3)

- **Distortion**: Both the ADC and the input driver introduce non-linearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver should be at least 10-dB lower than the distortion of the ADC, as shown in Equation 4:

$$THD_{AMP} \le THD_{ADC} - 10(dB) \quad (4)$$

- **Settling Time**: For DC signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.01% with a resistive load which may not be sufficient for the desired accuracy. Therefore, the settling behavior of the input driver with the RC filter load should always be verified by TINA™- SPICE simulations before selecting the amplifier.

10.1.2.2 ADC Input RC Filter

An RC filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. For DC signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurate settling of the signal at the ADC inputs during the small acquisition time window. For AC signals, the filter bandwidth should be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to- noise ratio (SNR) of the system.

A filter capacitor, C_{FLT}, connected across the ADC inputs (as shown in Figure 52), reduces the noise from the front-end drive circuitry, minimizes the effects of the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor should be at least 10 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 45 pF. Thus, the value of C_{FLT} should be greater than 450 pF. For applications measuring AC signals, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

Driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For low distortion applications, TI recommends limiting the value of R_{FLT} to a maximum of 50 Ω to avoid any significant degradation in linearity and THD performance.

The input amplifier bandwidth should be much higher than the cutoff frequency of the anti-aliasing filter. TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected RC filter.

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Application Information (continued)

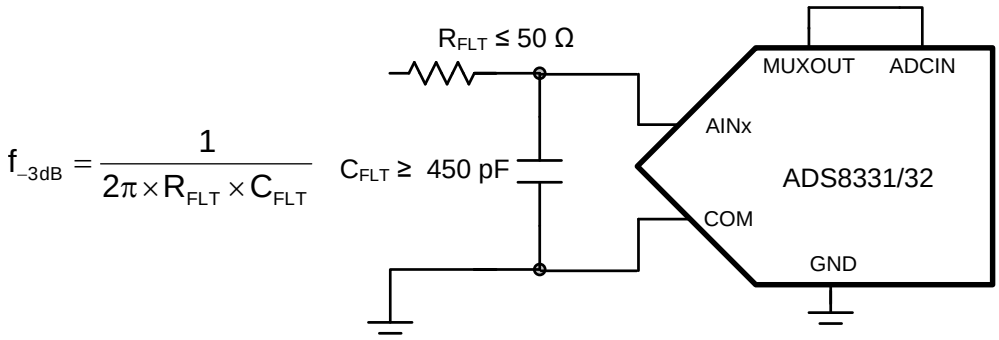

Figure 52. ADC Input RC Filter

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10.2 Typical Applications

10.2.1 DAQ Circuit for Low Noise and Distortion Performance for a 10-kHz Input Signal at 500 kSPS

Figure 53 illustrates a typical data acquisition circuit using the ADS833x for the lowest noise and distortion performance using a 10-kHz input signal at 500 kSPS.

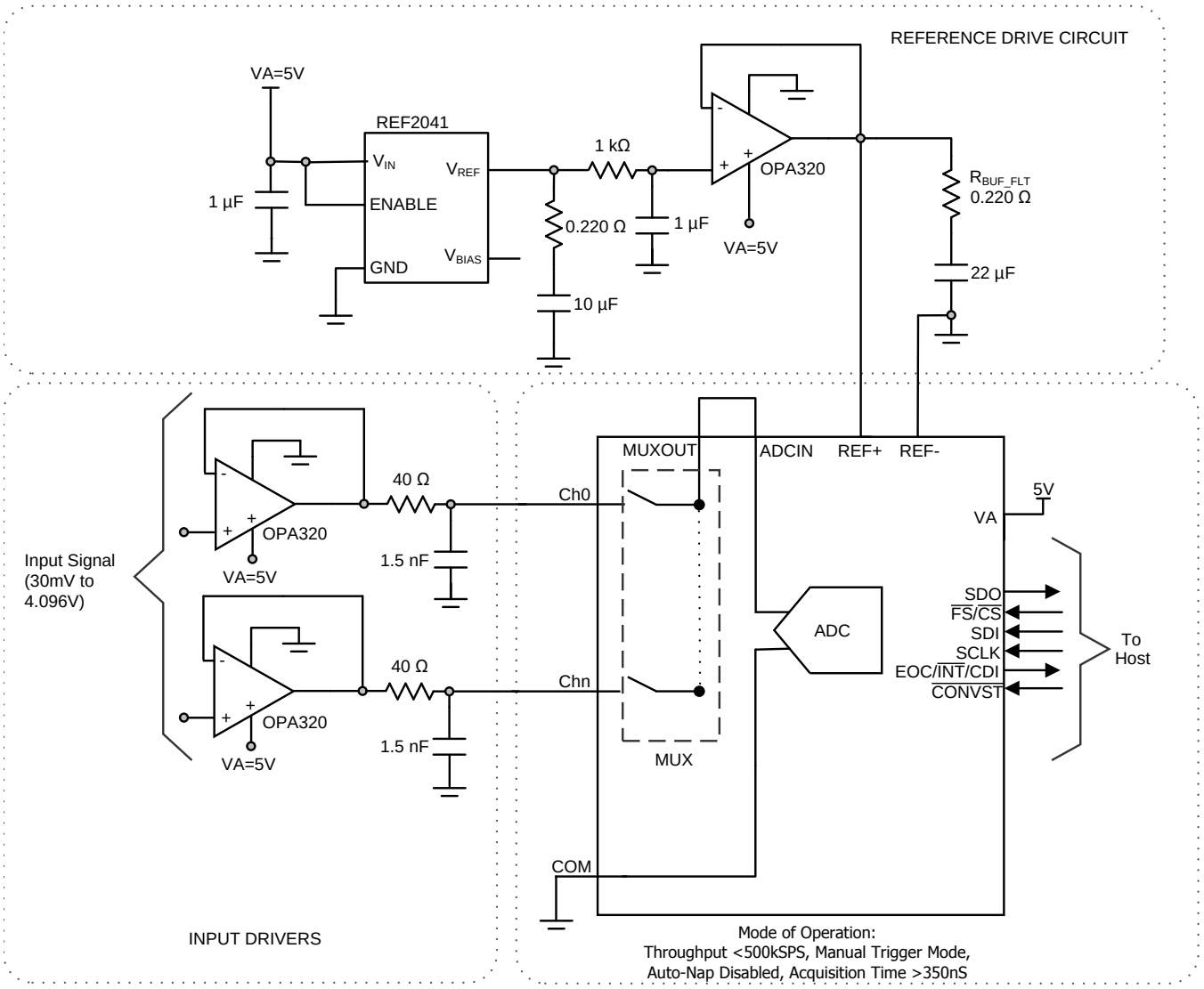

Figure 53. Typical Circuit Configuration

10.2.1.1 Design Requirements

This section describes an application circuit (Figure 53) optimized for using the ADS833x with lowest noise and distortion performance at ADC throughput of 500kSPS across all channels, using Manual Trigger mode with Auto-Nap mode disabled. The throughput per channel is dependent on the number of channels selected in the multiplexer scanning sequence. For example, the throughput per channel is equal to 250 kSPS if two channels are selected, but it is equal to 125 kSPS per channel if four channels are selected in the sequence and so forth.

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Typical Applications (continued)

10.2.1.2 Detailed Design Procedure

The signal is processed by a low noise, low distortion, operational amplifier in the non-inverting configuration and a low-pass RC filter before being fed into the ADC. The OPA320 features rail-to-rail input operation with a zero-crossover distortion topology that eliminates the transition region typical in many rail-to-rail complementary input stage amplifiers making it ideal to use in the non-inverting configuration. As a rule of thumb, the distortion from the input driver should be at least 10-dB less than the ADC distortion. Therefore, the driver circuit uses the low-power, wide bandwidth (20 MHz) OPA320 as an input driver, which provides exceptional AC performance because of its low-noise, and low distortion specifications. In addition, the components of the RC filter are selected such that the noise from the front-end circuit is limited without adding distortion to the input signal. *Driver Amplifier Choice* lists some more driver amplifier choices for applications that require high throughput operation with minimum acquisition time.

10.2.1.3 Application Curve

Figure 54 shows the FFT test results obtained with the ADS833x operating at full throughput of 500 kSPS and the circuit configuration of Figure 53.

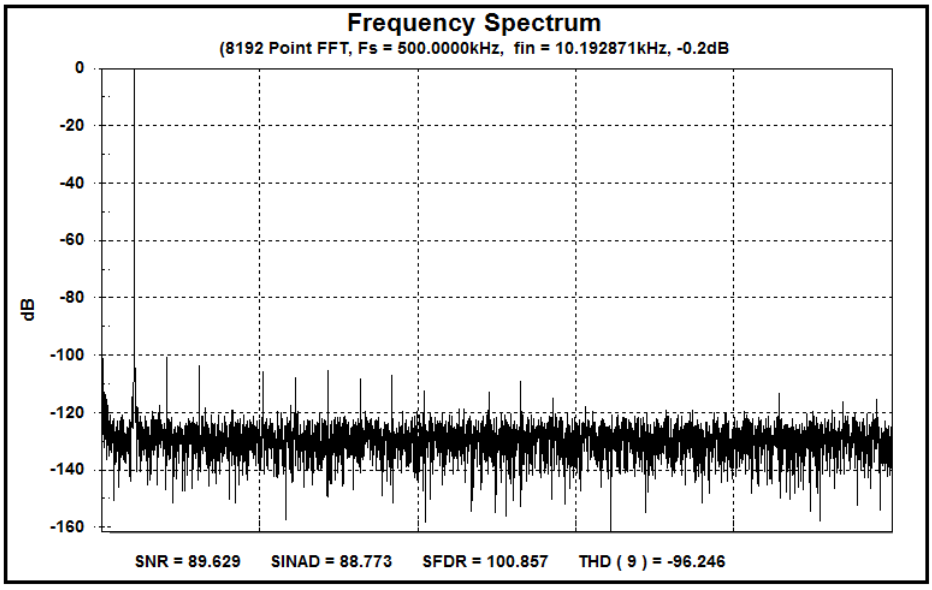

Figure 54. FFT Plot Showing Performance of ADS8331, ADS8332 With a 10-kHz Input Signal at 500 kSPS

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Typical Applications (continued)

10.2.2 Ultra Low-Power DAQ Circuit for DC Input Signals at 10 kSPS per Channel

Figure 55 illustrates a typical data acquisition circuit that is optimized for using the ADS833x in low power, low throughput applications for monitoring static or DC signals.

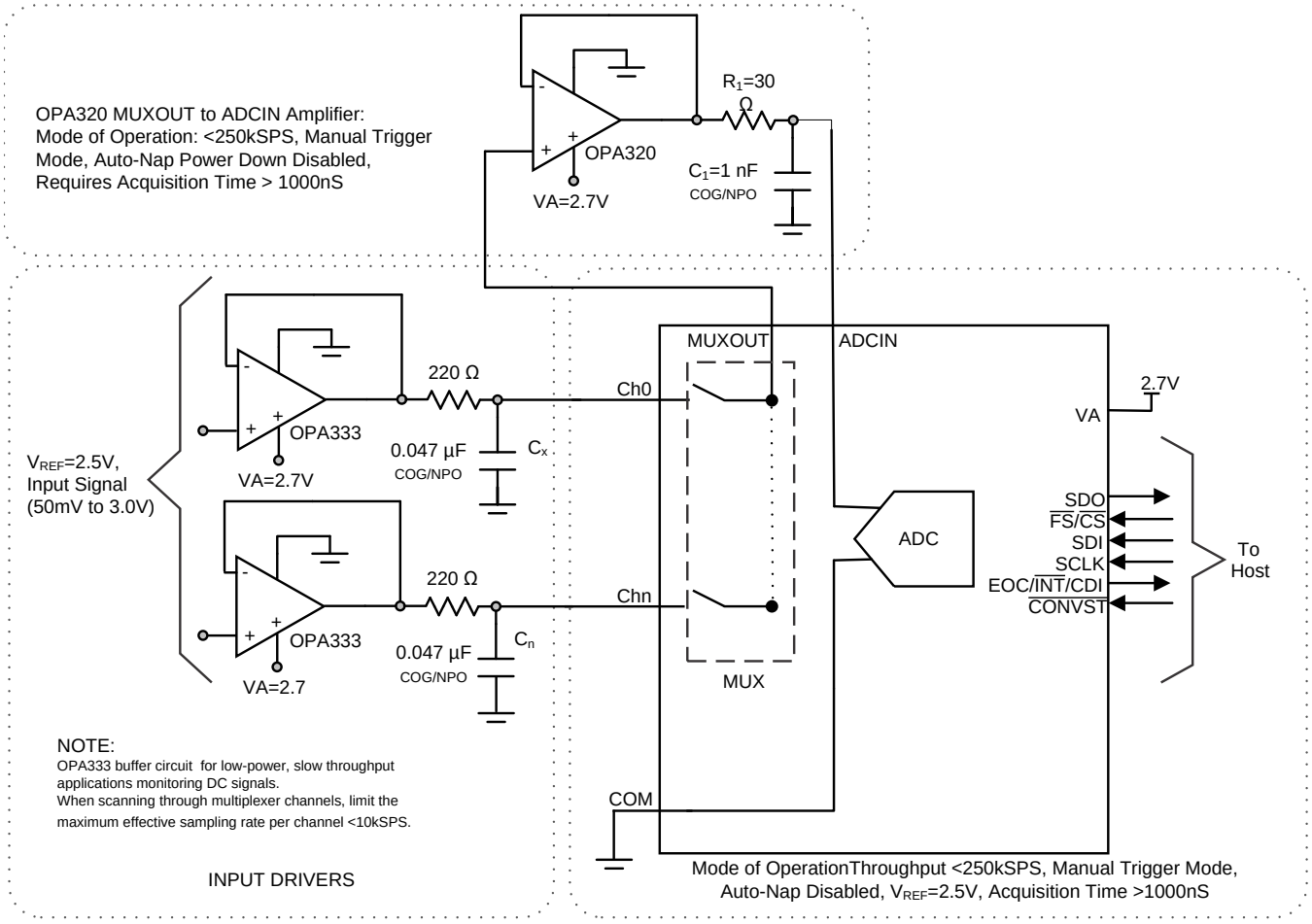

Figure 55. Typical Circuit Configuration

10.2.2.1 Design Requirements

This section describes an application circuit (Figure 55) optimized for using the ADS8332 in low power, low throughput applications for monitoring static or DC signals. A single OPA320 amplifier and passive filter (R_1, C_1) is placed between the MUXOUT and ADCIN inputs driving the ADS8332, while operating the ADC at a reduced data rate.

10.2.2.2 Detailed Design Procedure

The ADS833x offers the flexibility to place an amplifier between the MUXOUT and ADCIN pins. In this case, the operational amplifier between the multiplexer output and ADC input pin must have optimum transient response to charge the internal sampling capacitor (45 pF) and settle within 1 LSB after a full-scale step within the allowed acquisition time.

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Typical Applications (continued)

Placing an amplifier as a buffer between the multiplexer output and the ADC input helps to relax the source impedance requirements at the INx multiplexer inputs. However, it should be noted that there is a parasitic capacitance associated with the MUXOUT pin (approximately 5 pF). This is in addition to the input capacitance of the buffer amplifier placed between MUXOUT and ADCIN pins. This capacitance is switched from one channel to the next during the scan operation and must be recharged to new input channel voltage every time the multiplexer switches channels. Therefore, take care so the previously converted channel charge stored at the MUXOUT capacitance does not disturb the charge of the newly switched channel. This error can be reduced by placing a large enough capacitor at each (INx) multiplexer input.

The data acquisition circuit in Figure 55 is optimized for using the ADS8332 in low power, low throughput applications for monitoring static or DC signals. A single OPA320 amplifier and passive filter (R_1, C_1) is placed between the MUXOUT and ADCIN inputs driving the ADS8332, while operating the ADC at a reduced data rate. The OPA320 offers optimal settling time, DC precision and low noise at a relatively low power consumption (1.5 mA). In this case, the R1C1 is filter is designed to settle within ±1LSB in less than 1 µs after a full-scale input is applied. The ADC is operating at a reduced data rate of less than 250 kSPS in Manual Trigger Mode with Auto-NAP disabled (inactive) to allow a longer acquisition time.

Each multiplexer input is buffered with an ultralow power OPA333 to isolate the source impedance at the multiplexer inputs. A large capacitor Cx is placed at each INx input. The OPA320 has an estimated input capacitance of approximately 9 pF, and the capacitance associated with the MUXOUT pin is approximately 5 pF. The Cx capacitor is many times larger than the parasitic capacitance present at the MUXOUT pin to reduce the effect of charge injection due to the previously converted channel. The OPA333 consumes a maximum quiescent current of 25 µA per amplifier while providing low drift, excellent stability and DC performance at ultra low power consumption. To save power, this circuit is operated on a single 2.7-V supply. The OPA333 circuit is optimal for low-power, low-throughput applications measuring DC signals. When scanning through multiplexer channels ensure to limit the maximum sampling rate per channel to <10kSPS.

11 Power Supply Recommendations

During power on of the ADS833x, the digital interface supply voltage (VBD) should not exceed the analog supply voltage (VA). This condition is specified in the *Power-Supply Requirements* section of the Electrical Characteristics tables. If the analog and digital interface supplies for the converter are not generated by a single voltage source, TI recommends to power on the analog supply and wait for it to reach its final value before the digital interface supply is activated. Furthermore, the voltages applied to the analog input pins (IN_X, ADCIN) and digital input pins ($\overline{\text{RESET}}$, FS/$\overline{\text{CS}}$, SCLK, SDI, and $\overline{\text{CONVST}}$) should not exceed the voltages on VA and VBD, respectively, during the power-on sequence. This requirement prevents these input pins from powering the ADS833x through the ESD protection diodes and circuitry, and causing an increase in current consumption, until both supplies are fully powered (see the Electrical Characteristics and Figure 34 for further details).

Communication with the ADS833x, such as initiating a conversion with $\overline{\text{CONVST}}$ or writing to the Configuration register, should not occur for a minimum of 2 µs after the analog and digital interface supplies have finished the power-on sequence and reached the respective final values in the system. This time is required for the internal POR to activate and place the digital core of the device into the default mode of operation. This minimum delay time must also be adhered to whenever a reset condition occurs (see the *Reset Function* section for additional information).

12 Layout

12.1 Layout Guidelines

Figure 56 shows a board layout example for the ADS833x with the VQFN package. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As shown in Figure 56, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

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Layout Guidelines (continued)

The power sources to the device must be clean and well-bypassed. Use 10 μF, ceramic bypass capacitors in close proximity to the analog (VA) and digital (VBD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low impedance paths.

The REF+ reference input is bypassed with a 22 μF, X7S-grade, 0805-size, 10-V rated ceramic capacitors. Place the reference bypass capacitor as close as possible to the reference REF+ and REF- pins and connect the bypass capacitor using short, low-inductance connections. Avoid placing vias between the REF+ and REF- pins and the bypass capacitor. If the reference voltage originates from an op amp, make sure that the op amp can drive the bypass capacitor without oscillation. A small 0.2-Ω to 0.5-Ω resistors (R_{REF}) is used in series with the reference bypass capacitor to improve stability.

The fly-wheel RC filters are placed immediately next to the input pins. For applications measuring AC signals, COG (NPO) ceramic capacitors provide the best capacitance precision. Figure 56 shows input filter capacitors placed in close proximity to the INx analog input pins of the device.

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12.2 Layout Example

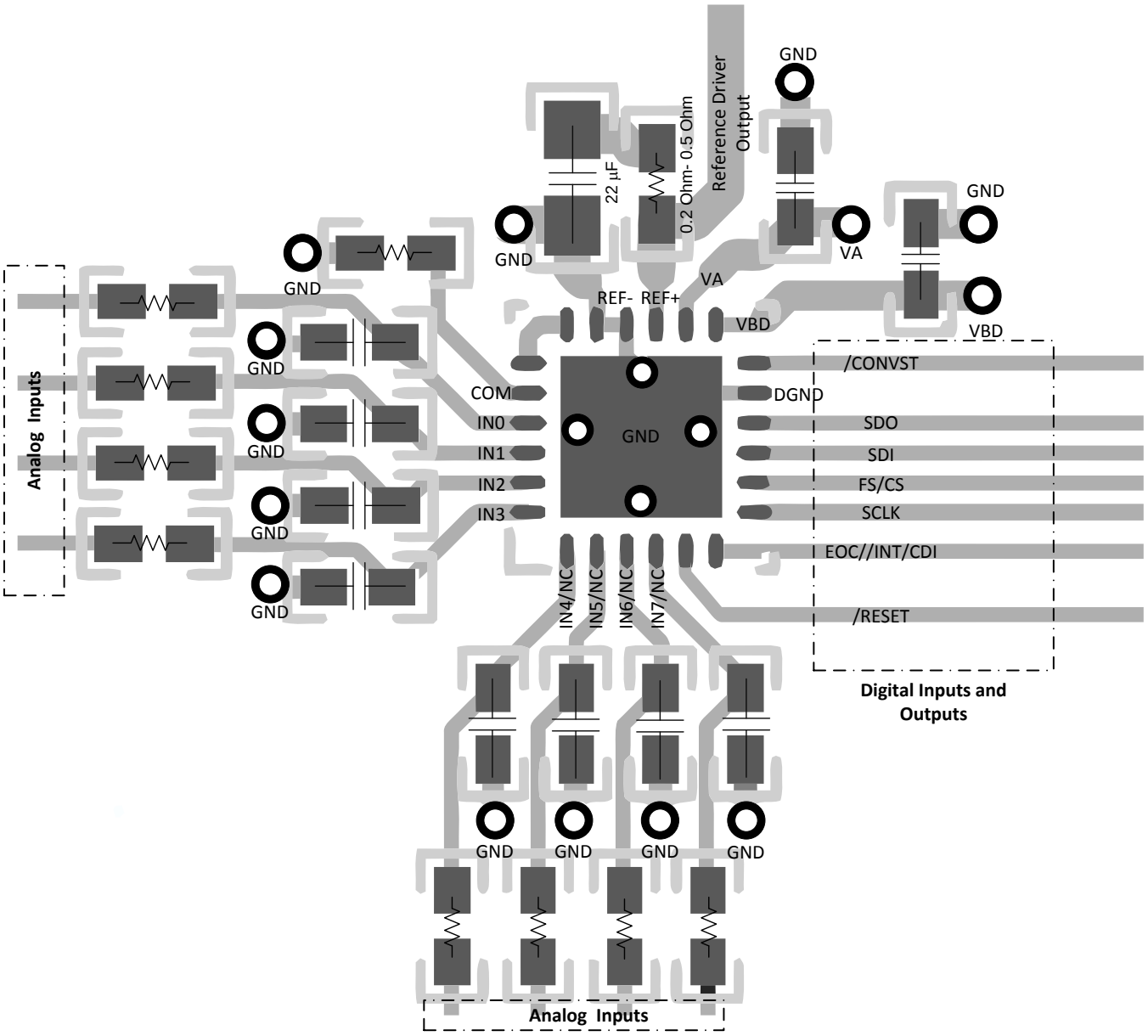

Figure 56. Layout Example for ADS833x

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *Determining Minimum Acquisition Times for SAR ADCs When a Step Function is Applied to the Input* (SBAA173)
- *50MHz, Low-Distortion, High CMRR, RRI/O, Single-Supply Operational Amplifier* (SBOS365)
- *1.1nV/√Hz Noise, Low Power, Precision Operational Amplifier in Small DFN-8 Package* (SBOS377)
- *Low-Noise, High-Precision, JFET-Input Operational Amplifier* (SBOS376)
- *100-MHz Low-Noise High-Speed Amplifiers* (SLOS224)
- *Low-Noise, Very Low Drift, Precision Voltage Reference* (SBOS410)
- *REF20xx Low-Drift, Low-Power, Dual-Output, VREF and VREF / 2 Voltage References* (SBOS600)
- *Precision, 20MHz, 0.9pA, Low-Noise, RRIO, CMOS Operational Amplifier With Shutdown* (SBOS513)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS8331	Click here	Click here	Click here	Click here	Click here
ADS8332	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

TMS320, E2E are trademarks of Texas Instruments.
SPI is a trademark of Motorola, Inc.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8331IBPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8331 B	Samples
ADS8331IBPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8331 B	Samples
ADS8331IBRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8331 B	Samples
ADS8331IBRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8331 B	Samples
ADS8331IPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8331	Samples
ADS8331IPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8331	Samples
ADS8331IRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8331	Samples
ADS8331IRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8331	Samples
ADS8332IBPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8332 B	Samples
ADS8332IBPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8332 B	Samples
ADS8332IBRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8332 B	Samples
ADS8332IBRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8332 B	Samples
ADS8332IPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8332	Samples
ADS8332IPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8332	Samples
ADS8332IRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8332	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8332IRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8332	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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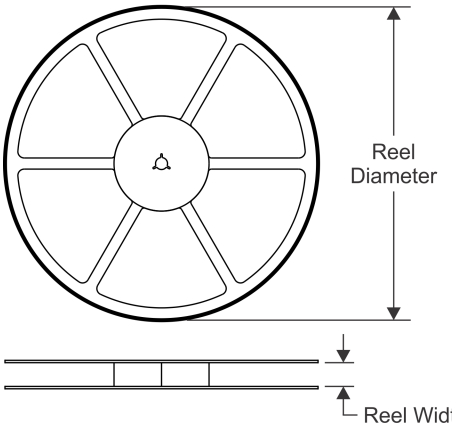
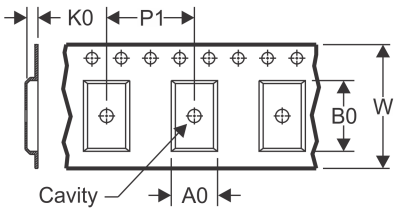
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

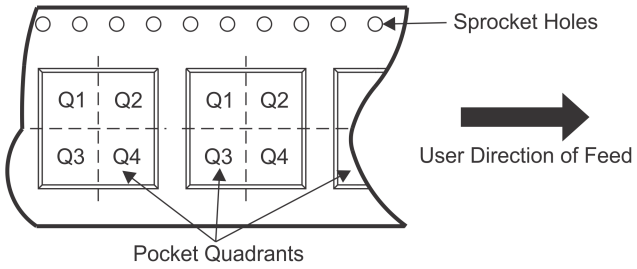


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

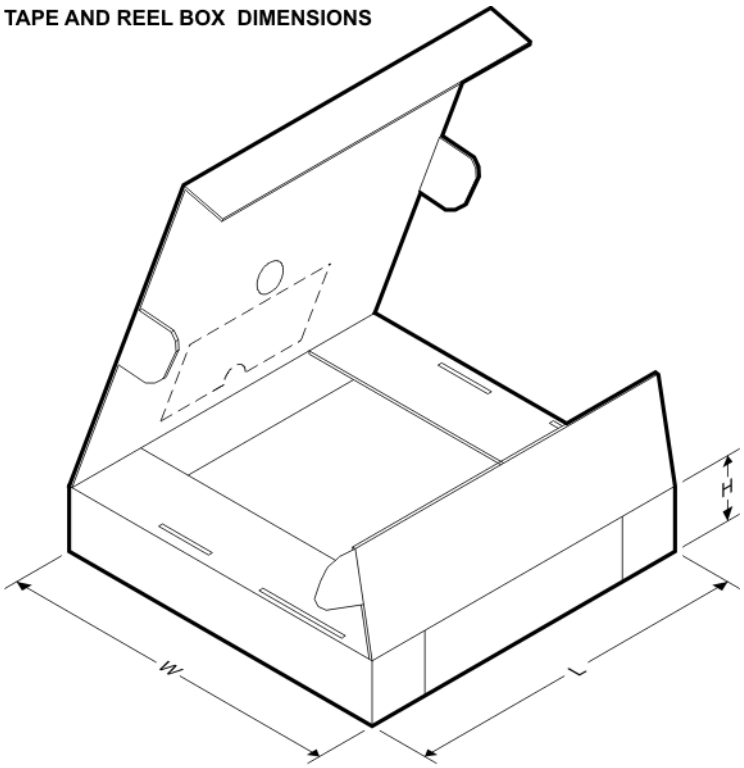
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8331IBPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS8331IBRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8331IBRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8331IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS8331IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8331IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8332IBPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS8332IBRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8332IBRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8332IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS8332IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8332IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



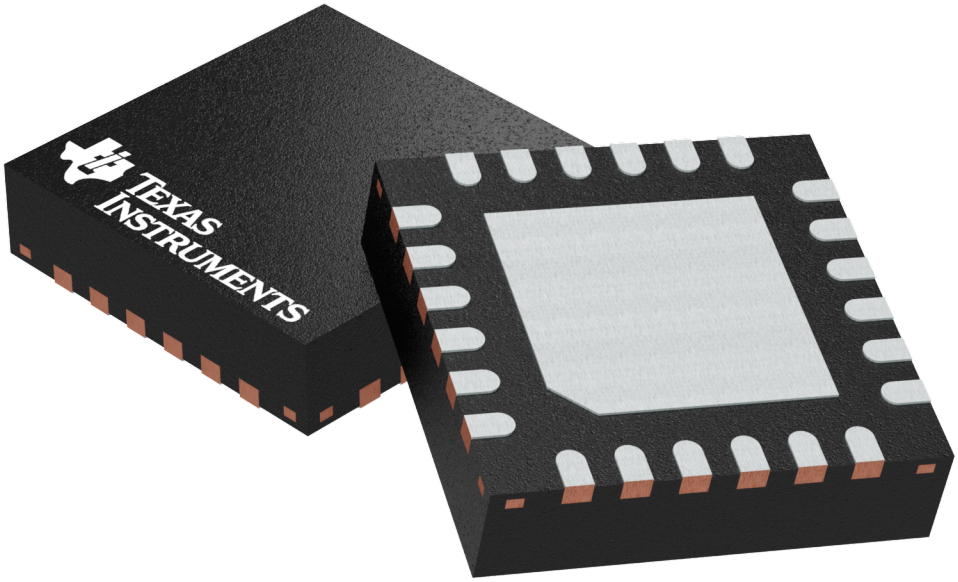
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8331IBPWR	TSSOP	PW	24	2000	367.0	367.0	38.0
ADS8331IBRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8331IBRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS8331IPWR	TSSOP	PW	24	2000	367.0	367.0	38.0
ADS8331IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8331IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS8332IBPWR	TSSOP	PW	24	2000	367.0	367.0	38.0
ADS8332IBRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8332IBRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS8332IPWR	TSSOP	PW	24	2000	367.0	367.0	38.0
ADS8332IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8332IRGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



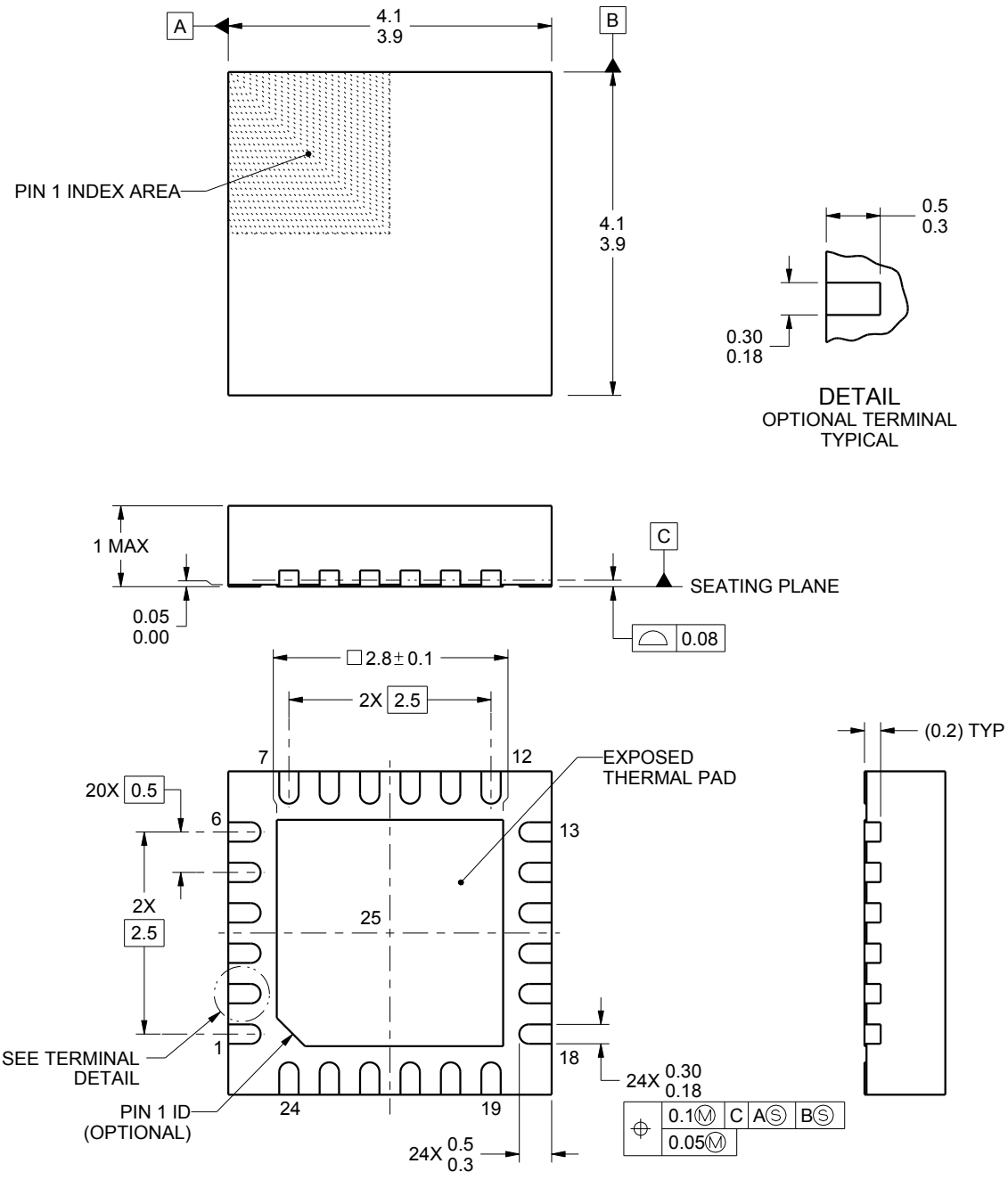
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGE0024F

VQFN - 1 mm max height

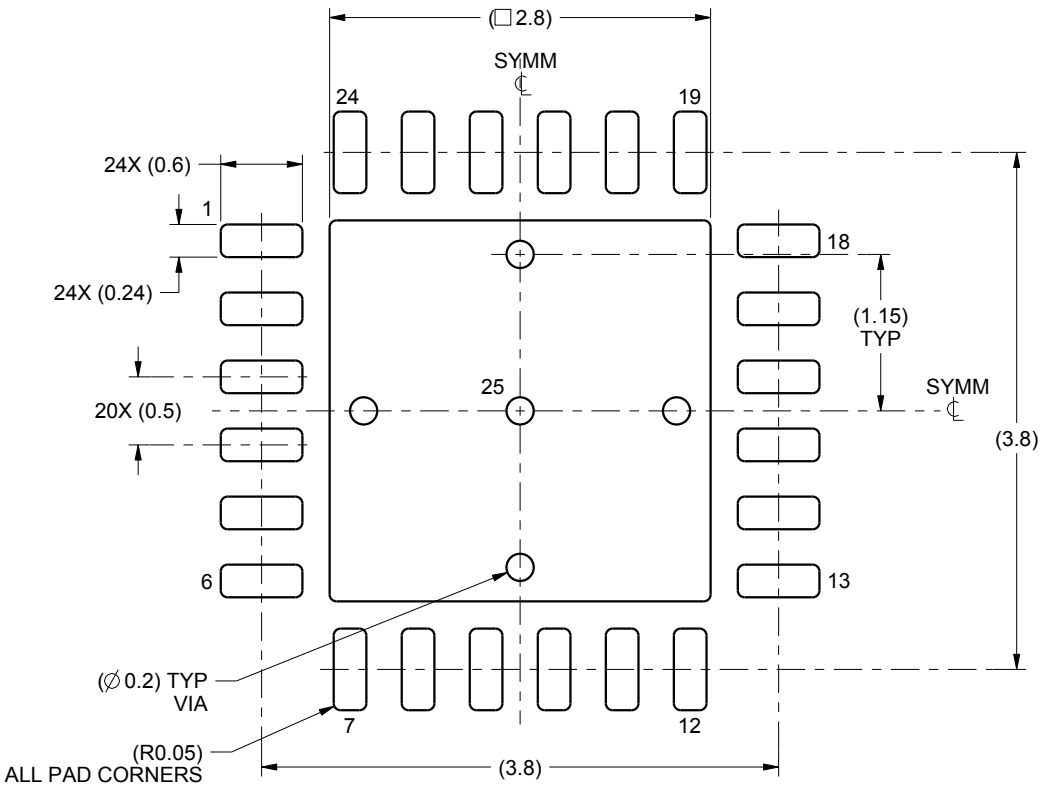
PLASTIC QUAD FLATPACK - NO LEAD



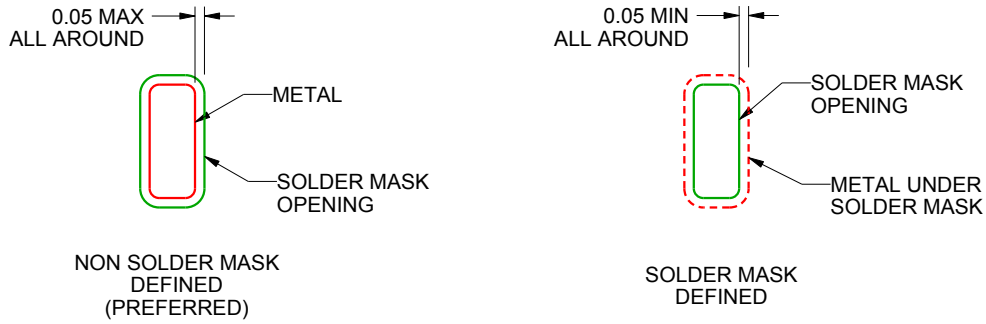
4222437/A 12/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
SCALE:18X

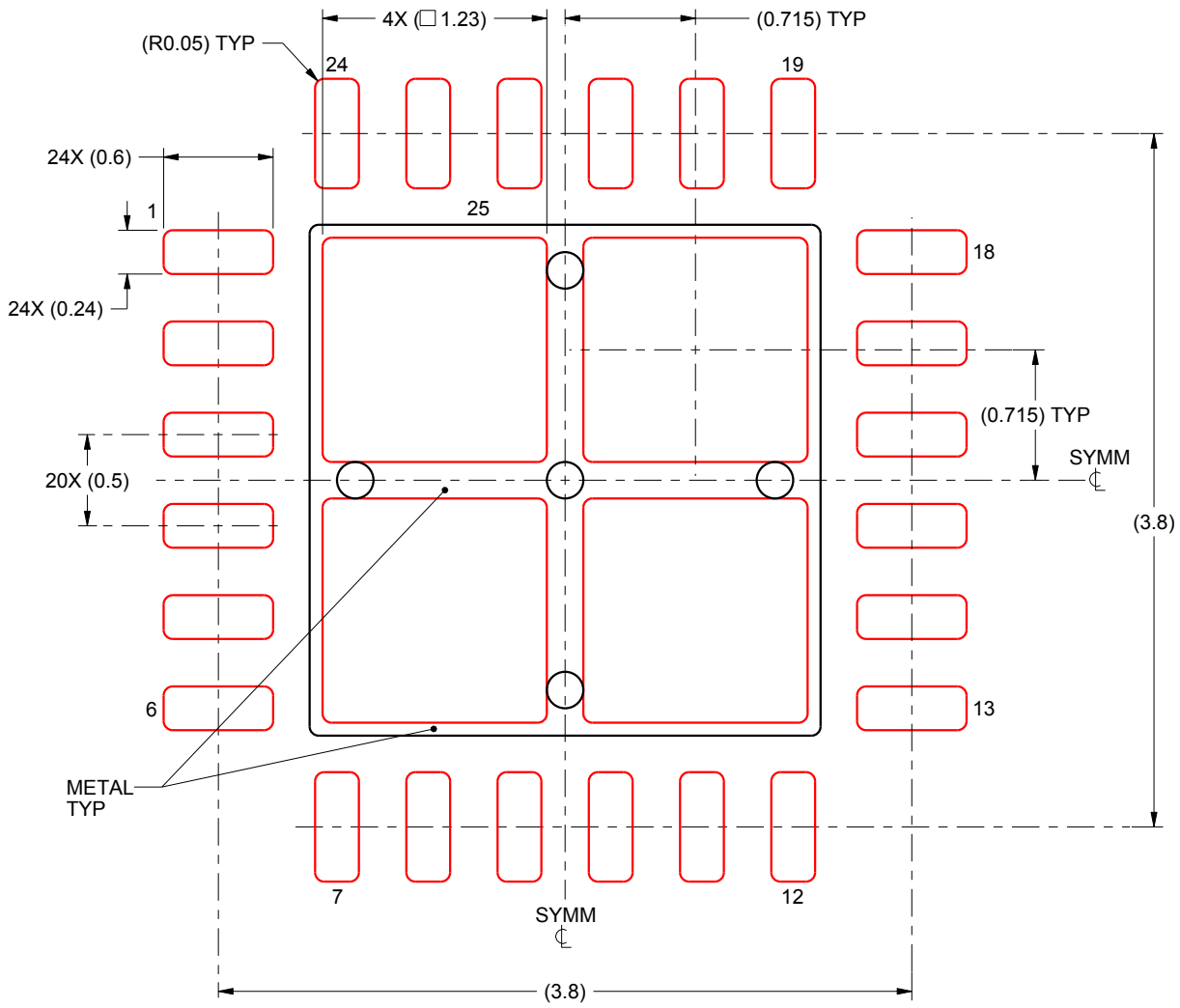


SOLDER MASK DETAILS

4222437/A 12/2015

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222437/A 12/2015

NOTES: (continued)

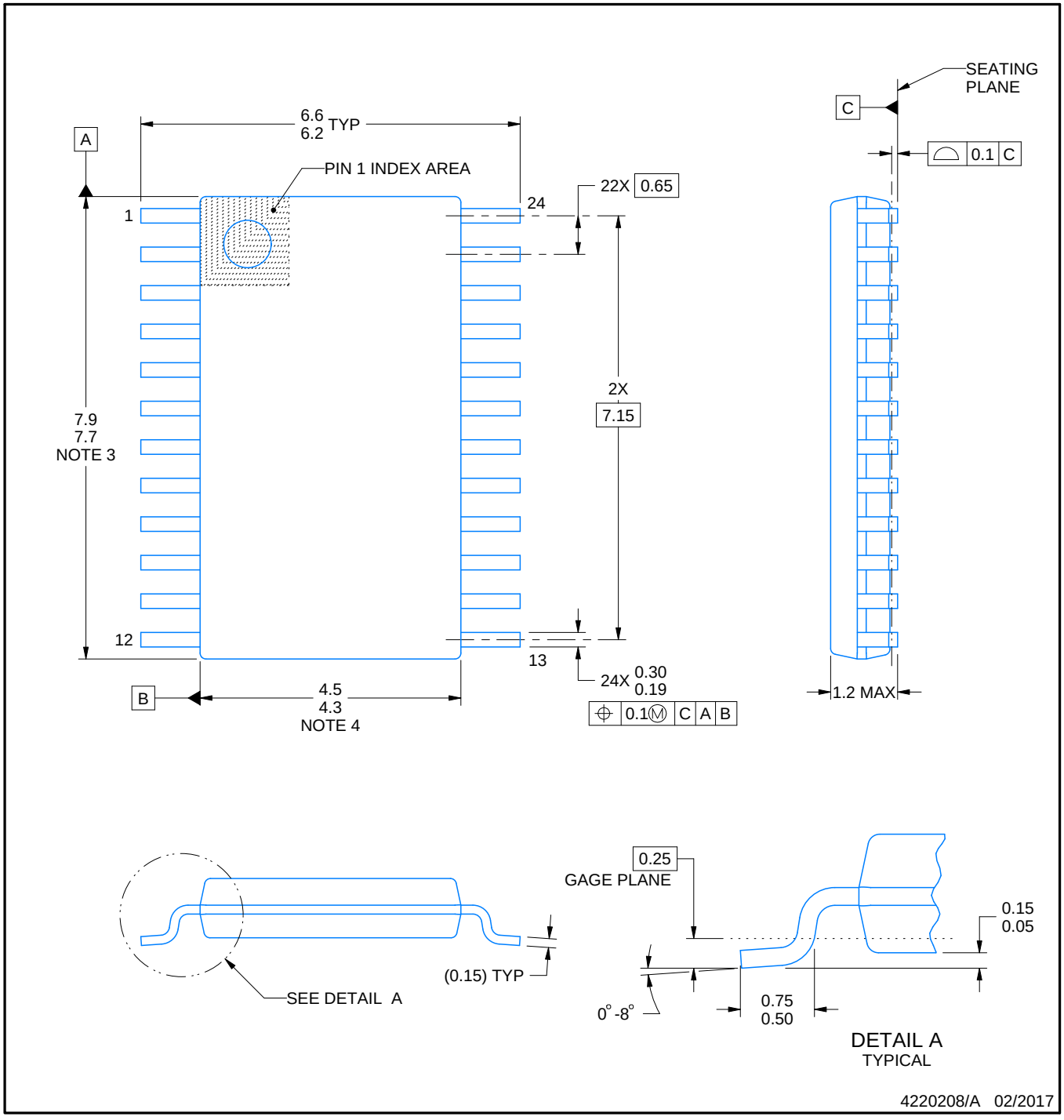
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0024A

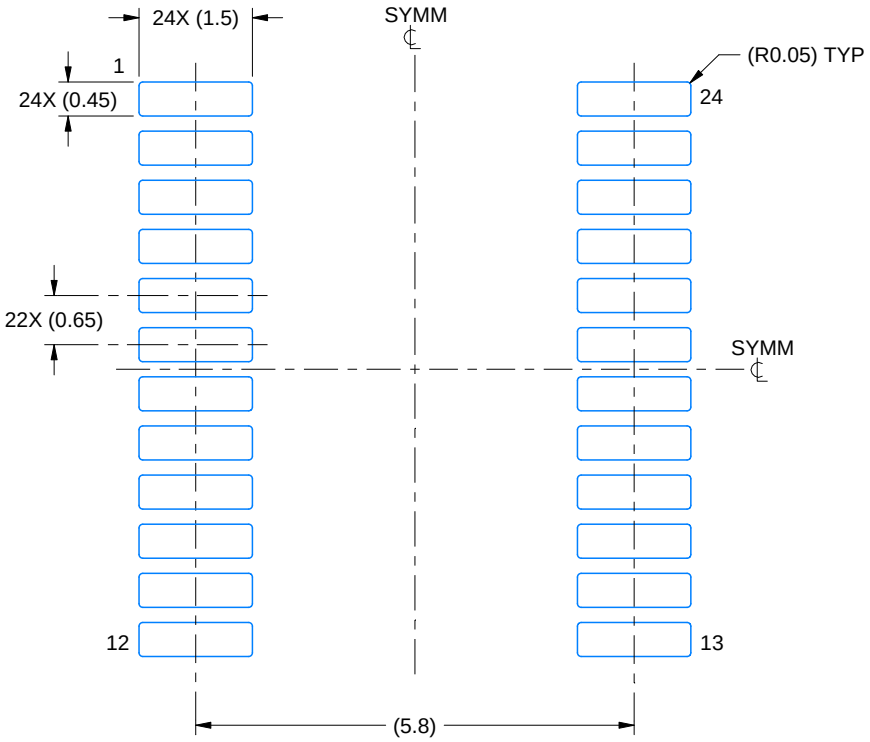
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

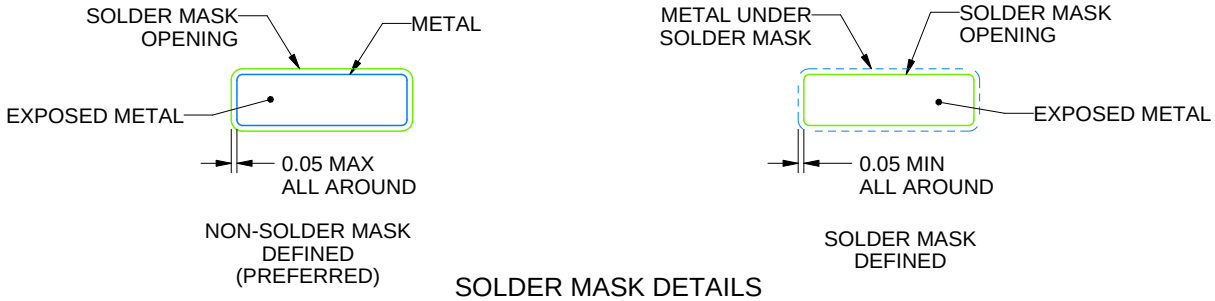


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

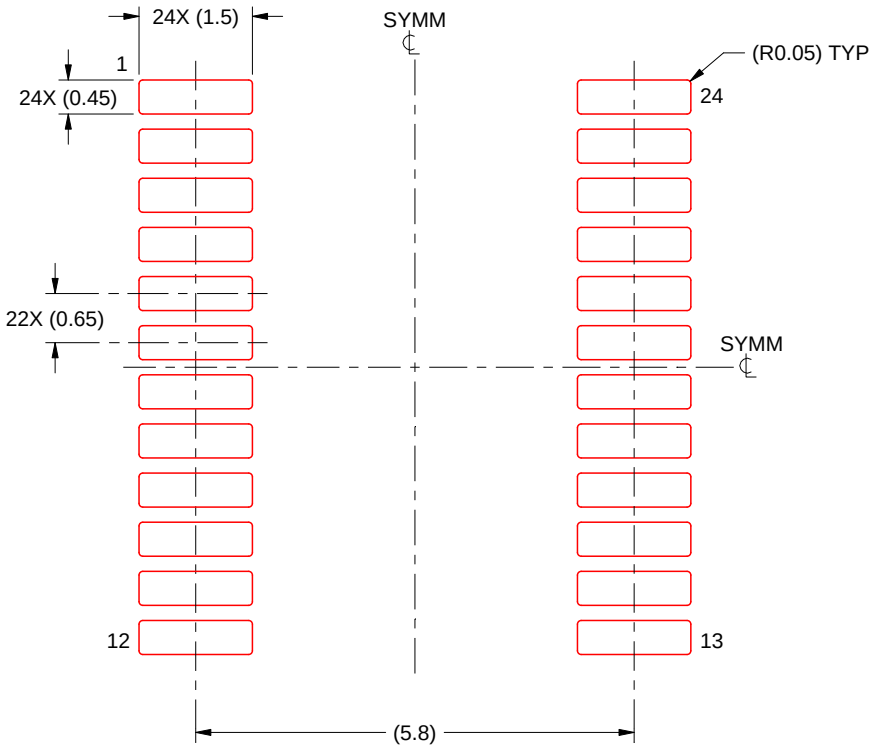


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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