

# H7N0603DL, H7N0603DS

Silicon N Channel MOS FET  
High speed power Switching

REJ03G0123-0100Z

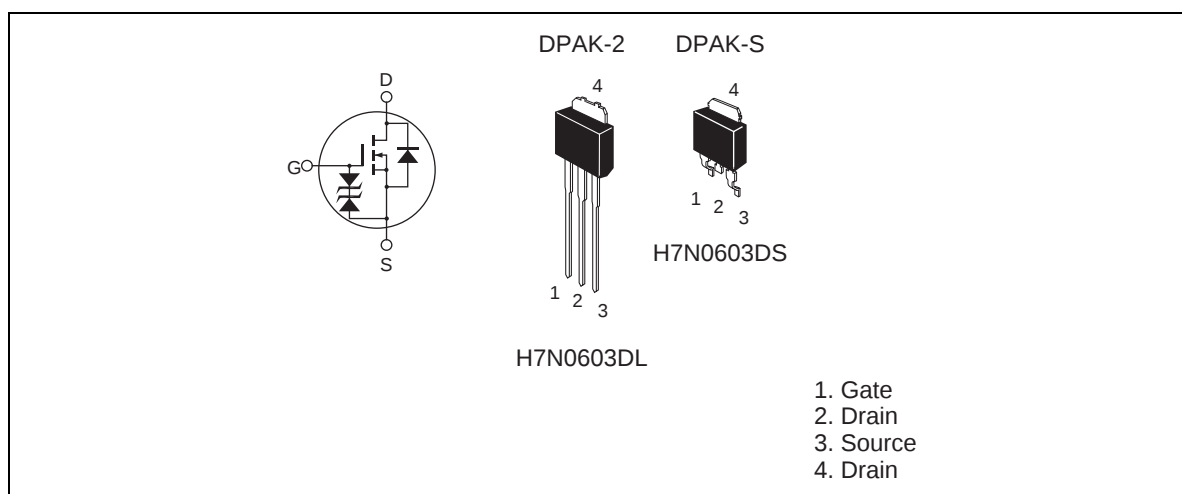
Rev.1.00

Oct.14.2003

## Features

- Low on - resistance  
 $R_{DS(on)} = 11\text{ m}\Omega$  typ.
- Low drive current
- Capable of 4.5 gate drive

## Outline



**Absolute Maximum Ratings**

(Ta = 25°C)

| Item                                   | Symbol                                  | Ratings     | Unit |
|----------------------------------------|-----------------------------------------|-------------|------|
| Drain to source voltage                | V <sub>DSS</sub>                        | 60          | V    |
| Gate to source voltage                 | V <sub>GSS</sub>                        | ±20         | V    |
| Drain current                          | I <sub>D</sub>                          | 30          | A    |
| Drain peak current                     | I <sub>D</sub> (pulse) <sup>Note1</sup> | 120         | A    |
| Body drain diode reverse drain current | I <sub>DR</sub>                         | 30          | A    |
| Avalanche current                      | I <sub>AP</sub> <sup>Note3</sup>        | 25          | A    |
| Avalanche energy                       | E <sub>AR</sub> <sup>Note3</sup>        | 53.6        | mJ   |
| Channel dissipation                    | P <sub>ch</sub> <sup>Note2</sup>        | 40          | W    |
| Channel temperature                    | T <sub>ch</sub>                         | 150         | °C   |
| Storage temperature                    | T <sub>stg</sub>                        | –55 to +150 | °C   |

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
2. Tc = 25°C  
3. Tch = 25°C, Rg ≥ 50Ω

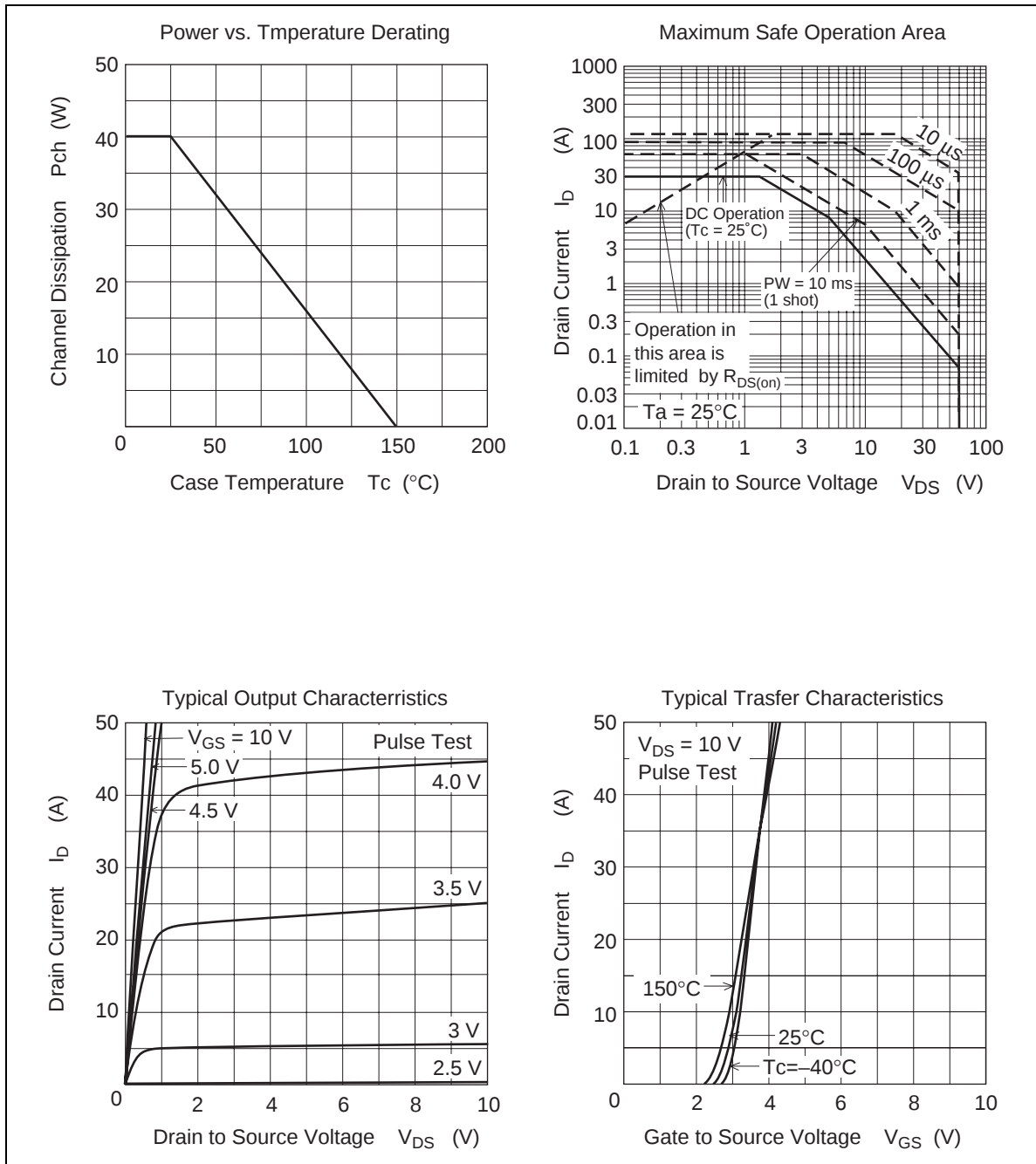
## Electrical Characteristics

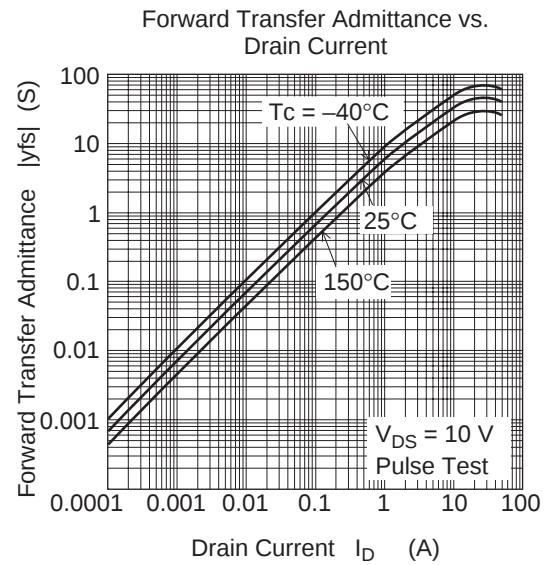
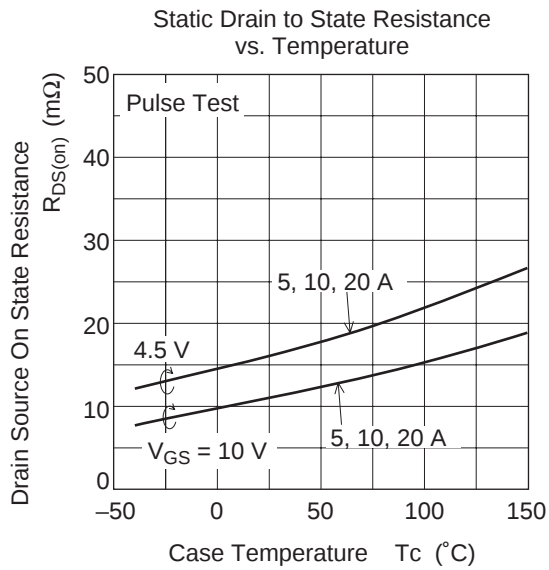
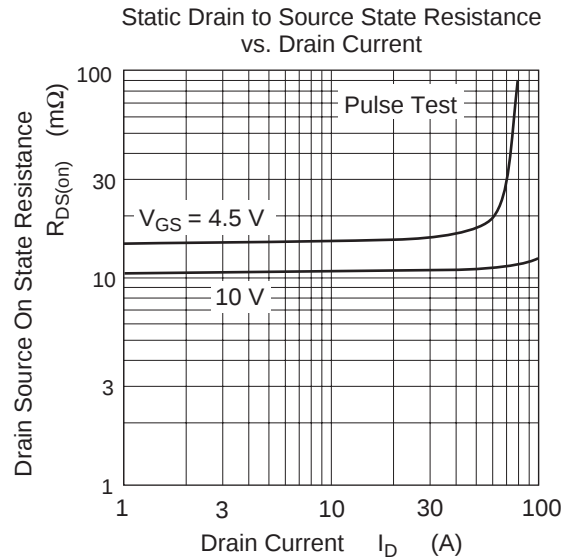
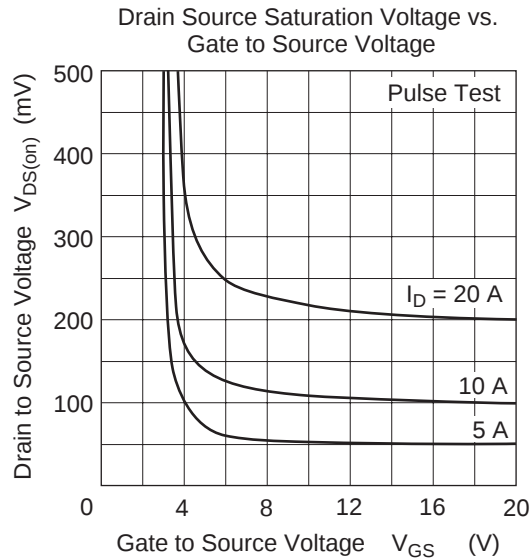
(Ta = 25°C)

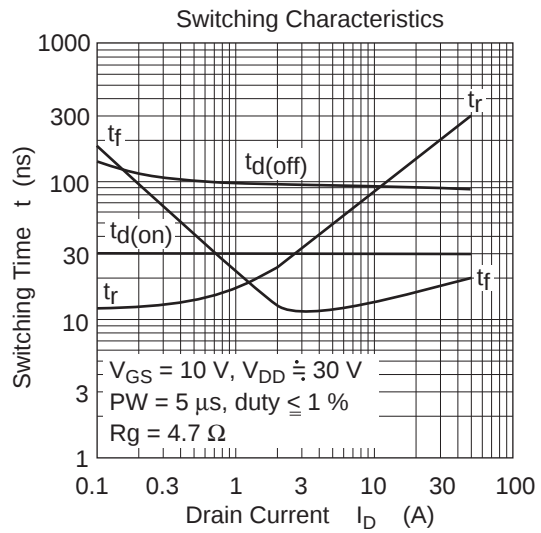
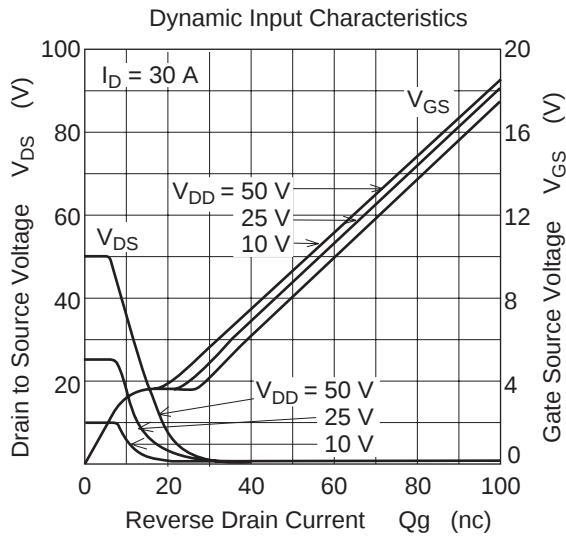
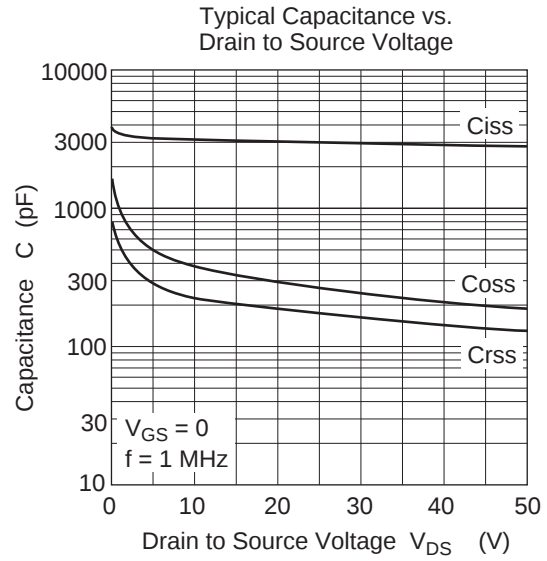
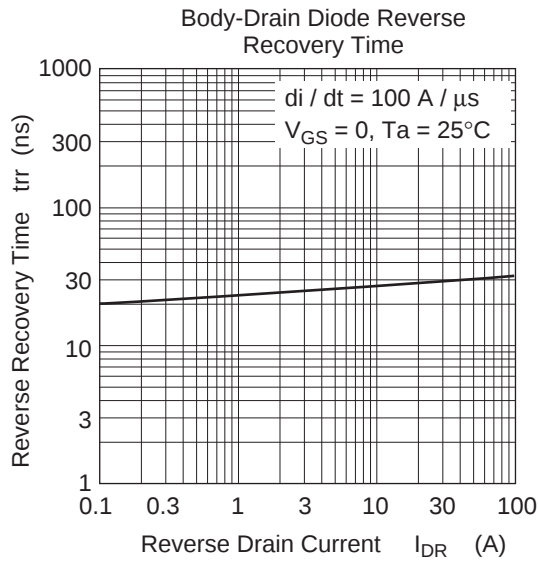
| Item                                       | Symbol        | Min      | Typ  | Max      | Unit          | Test condition                                                                  |
|--------------------------------------------|---------------|----------|------|----------|---------------|---------------------------------------------------------------------------------|
| Drain to source breakdown voltage          | $V_{(BR)DSS}$ | 60       | —    | —        | V             | $I_D = 10 \text{ mA}$ , $V_{GS} = 0$                                            |
| Gate to source breakdown voltage           | $V_{(BR)GSS}$ | $\pm 20$ | —    | —        | V             | $I_G = \pm 100 \text{ }\mu\text{A}$ , $V_{DS} = 0$                              |
| Gate to source leak current                | $I_{GSS}$     | —        | —    | $\pm 10$ | $\mu\text{A}$ | $V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$                                      |
| Zero gate voltage drain current            | $I_{DSS}$     | —        | —    | 10       | $\mu\text{A}$ | $V_{DS} = 60 \text{ V}$ , $V_{GS} = 0$                                          |
| Gate to source cutoff voltage              | $V_{GS(off)}$ | 1.5      | —    | 2.5      | V             | $I_D = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}$                                  |
| Static drain to source on state resistance | $R_{DS(on)}$  | —        | 11   | 15       | m $\Omega$    | $I_D = 15 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note1</sup>                 |
|                                            |               |          | 16   | 22       | m $\Omega$    | $I_D = 15 \text{ A}$ , $V_{GS} = 4.5 \text{ V}$ <sup>Note1</sup>                |
| Forward transfer capacitance               | $ y_{fs} $    | 24       | 40   | —        | S             | $I_D = 15 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note1</sup>                 |
| Input capacitance                          | $C_{iss}$     | —        | 3200 | —        | pF            | $V_{DS} = 10 \text{ V}$<br>$V_{GS} = 0$                                         |
| Output capacitance                         | $C_{oss}$     | —        | 385  | —        | pF            | $f = 1 \text{ MHz}$                                                             |
| Reverse transfer capacitance               | $C_{rss}$     | —        | 225  | —        | pF            |                                                                                 |
| Total gate charge                          | $Q_g$         | —        | 56   | —        | nC            | $V_{DD} = 25 \text{ V}$<br>$V_{GS} = 10 \text{ V}$                              |
| Gate to source charge                      | $Q_{gs}$      | —        | 11   | —        | nC            | $I_D = 30 \text{ A}$                                                            |
| Gate to drain charge                       | $Q_{gd}$      | —        | 12   | —        | nC            |                                                                                 |
| Turn-on delay time                         | $t_{d(on)}$   | —        | 30   | —        | ns            | $V_{GS} = 10 \text{ V}$ , $I_D = 15 \text{ A}$<br>$R_L = 2.0 \text{ }\Omega$    |
| Rise time                                  | $t_r$         | —        | 125  | —        | ns            | $R_g = 4.7 \text{ }\Omega$                                                      |
| Turn-off delay time                        | $t_{d(off)}$  | —        | 90   | —        | ns            |                                                                                 |
| fall time                                  | $t_f$         | —        | 17   | —        | ns            |                                                                                 |
| Body - drain diode forward voltage         | $V_{DF}$      | —        | 0.9  | —        | V             | $I_F = 30 \text{ A}$ , $V_{GS} = 0$ <sup>Note1</sup>                            |
| Body – drain diode reverse recovery time   | $t_{rr}$      | —        | 30   | —        | ns            | $I_F = 30 \text{ A}$ , $V_{GS} = 0$<br>$diF / dt = 100 \text{ A} / \mu\text{s}$ |

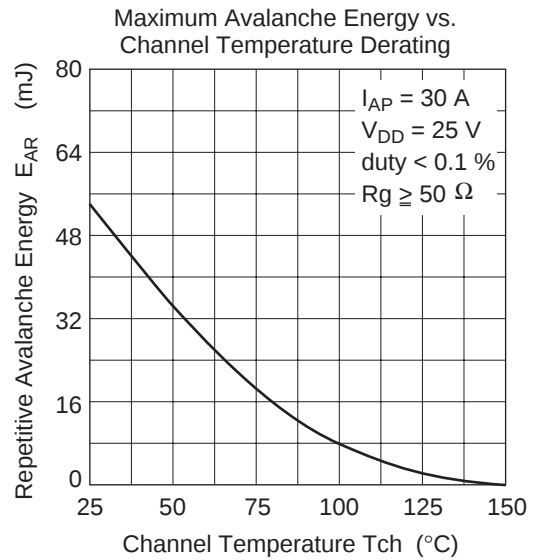
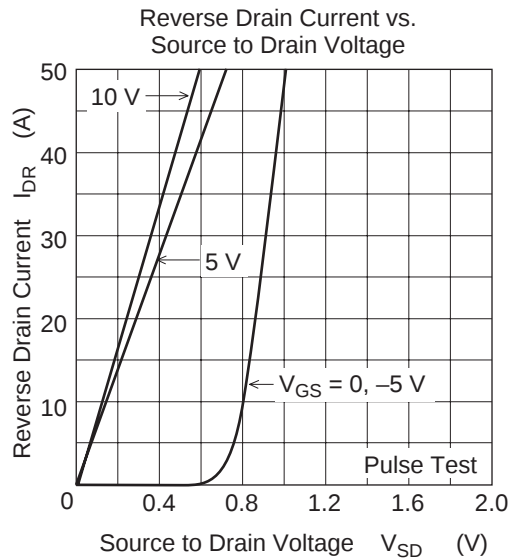
Notes: 1. Pulse Test

## Main Characteristics

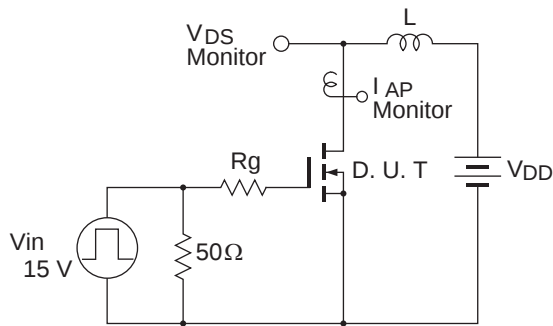






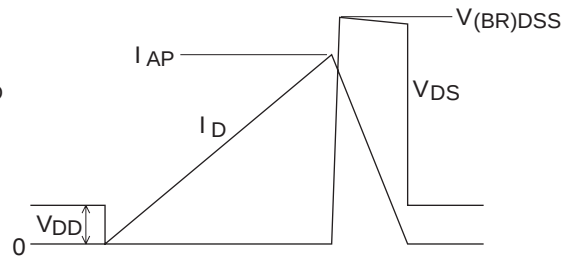


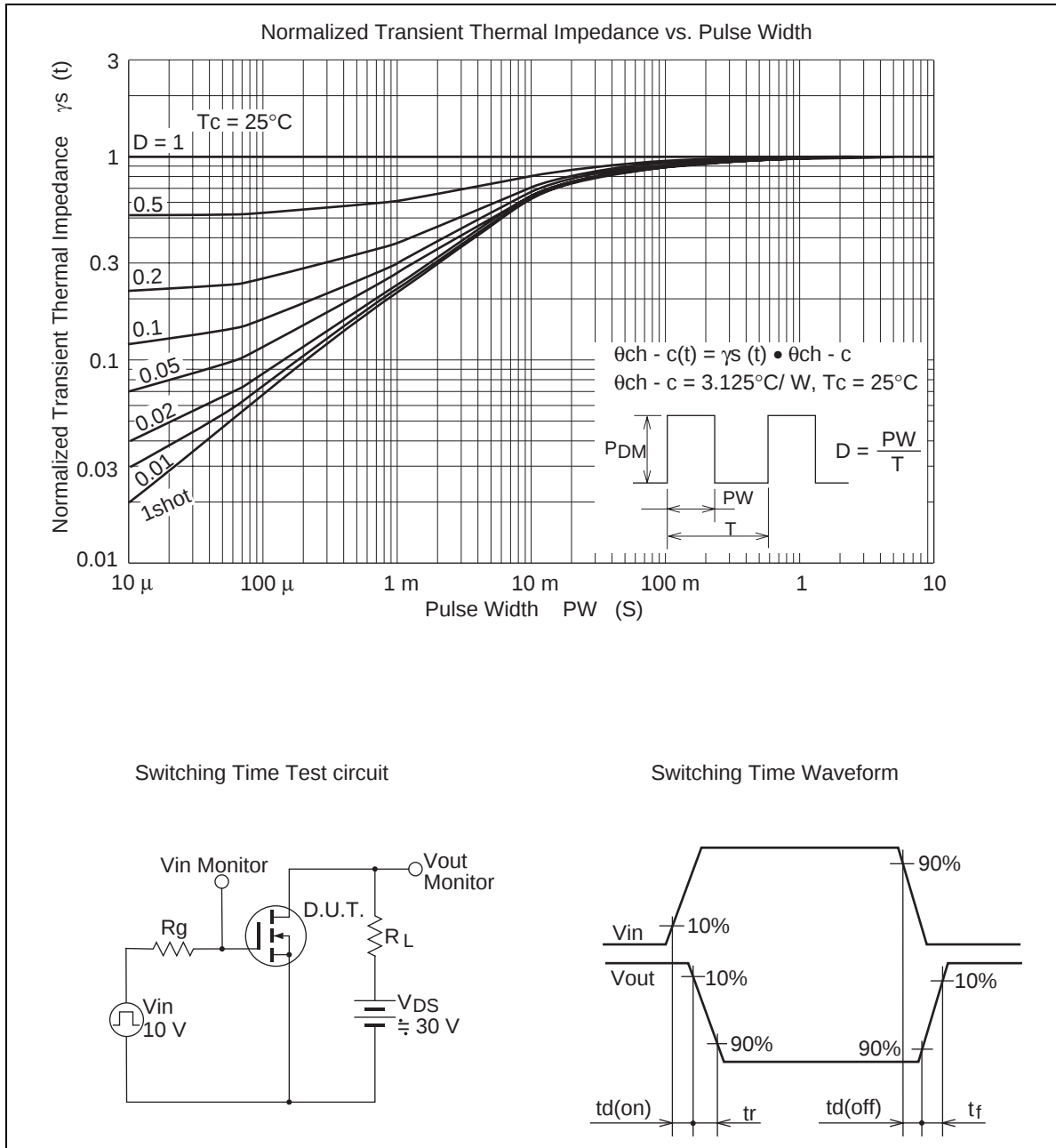
Avalanche Test Circuit



Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

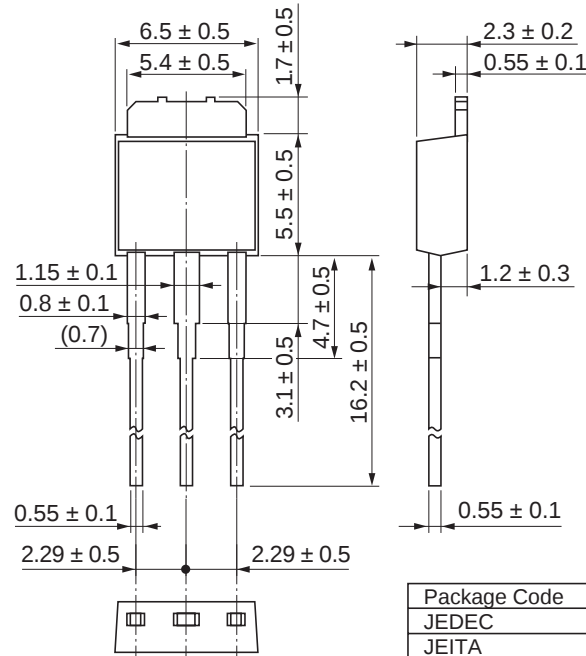




## Package Dimensions

• H7N0603DL

As of January, 2003  
Unit: mm

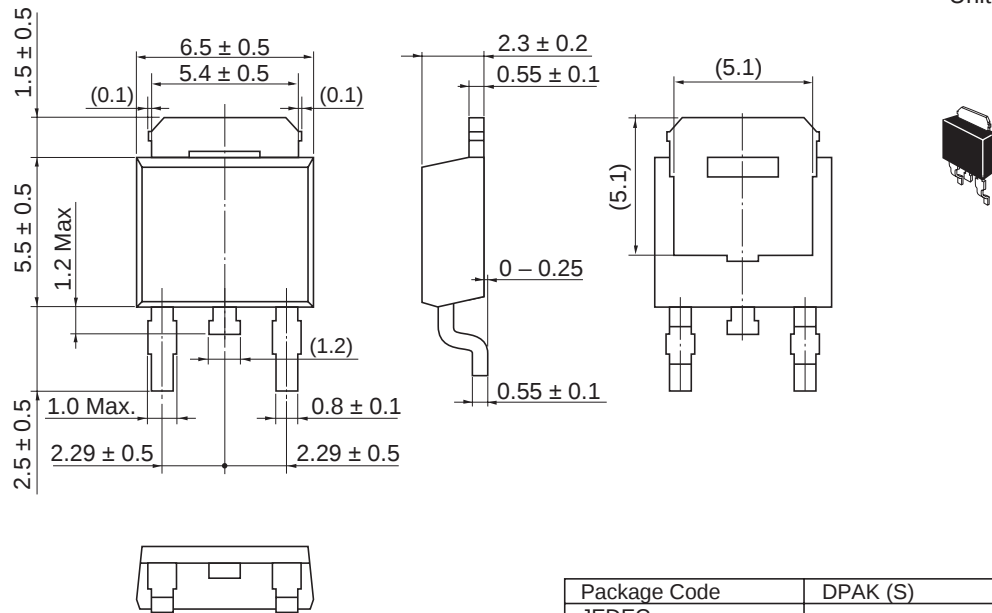


|                        |              |
|------------------------|--------------|
| Package Code           | DPAK (L)-(2) |
| JEDEC                  | —            |
| JEITA                  | —            |
| Mass (reference value) | 0.42 g       |

• H7N0603DS

As of January, 2003

Unit: mm



|                        |          |
|------------------------|----------|
| Package Code           | DPAK (S) |
| JEDEC                  | —        |
| JEITA                  | Conforms |
| Mass (reference value) | 0.28 g   |

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