18-Bit, 1Msps, ±10.24V True Bipolar, Pseudo-Differential Input ADC with 95dB SNR

FEATURES

- **1Msps Throughput Rate**
- **±5LSB INL (Max)**
- **Guaranteed 18-Bit No Missing Codes**
- **Pseudo-Differential Inputs**
- **True Bipolar Input Ranges ±6.25V, ±10.24V, ±12.5V**
- **95dB SNR (Typ) at f_{IN} = 2kHz**
- **–111dB THD (Typ) at f_{IN} = 2kHz**
- Guaranteed Operation to 125°C
- Single 5V Supply
- Low Drift (20ppm/°C Max) 2.048V Internal Reference
- Onboard Single-Shot Capable Reference Buffer
- No Pipeline Delay, No Cycle Latency
- 1.8V to 5V I/O Voltages
- SPI-Compatible Serial I/O with Daisy-Chain Mode
- Internal Conversion Clock
- Power Dissipation 50mW (Typ)
- 16-Lead MSOP Package

APPLICATIONS

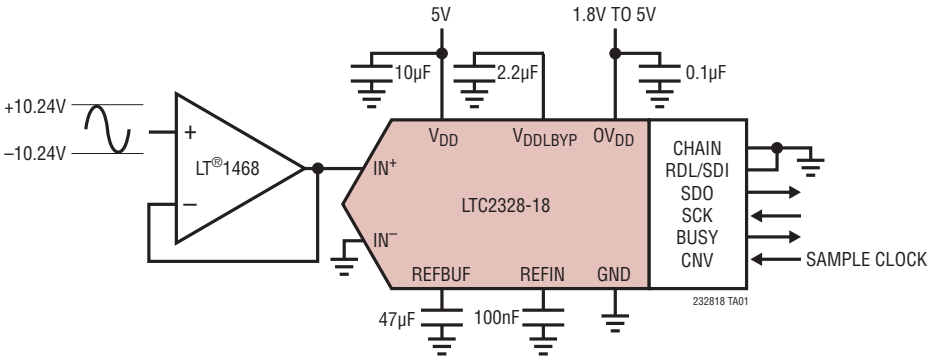
- Programmable Logic Controllers
- Industrial Process Control
- High Speed Data Acquisition
- Portable or Compact Instrumentation
- ATE

DESCRIPTION

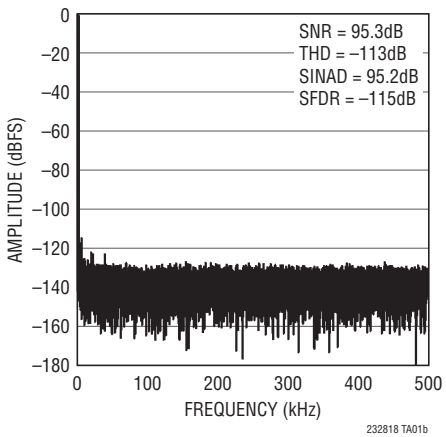
The LTC®2328-18 is a low noise, high speed 18-bit successive approximation register (SAR) ADC with pseudo-differential inputs. Operating from a single 5V supply, the LTC2328-18 has a ±10.24V true bipolar input range, making it ideal for high voltage applications which require a wide dynamic range. The LTC2328-18 achieves ±5LSB INL maximum, no missing codes at 18 bits with 95dB SNR.

The LTC2328-18 has an onboard single-shot capable reference buffer and low drift (20ppm/°C max) 2.048V temperature compensated reference. The LTC2328-18 also has a high speed SPI-compatible serial interface that supports 1.8V, 2.5V, 3.3V and 5V logic while also featuring a daisy-chain mode. The fast 1Msps throughput with no cycle latency makes the LTC2328-18 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2328-18 dissipates only 50mW and automatically naps between conversions, leading to reduced power dissipation that scales with the sampling rate. A sleep mode is also provided to reduce the power consumption of the LTC2328-18 to 300µW for further power savings during inactive periods.

TYPICAL APPLICATION



32k Point FFT f_S = 1Msps, f_{IN} = 2kHz

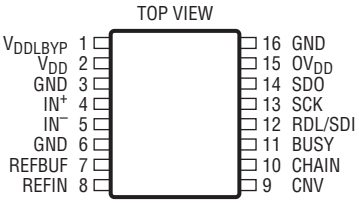


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Supply Voltage (OV_{DD}) 6V
Supply Bypass Voltage (V_{DDLBYP}) 3.2V
Analog Input Voltage
  IN^+, IN^- ..... –16.5V to 16.5V
  REFBUF 6V
  REFIN 2.8V
Digital Input Voltage
(Note 3) ..... (GND –0.3V) to (OV_{DD} + 0.3V)
Digital Output Voltage
(Note 3) ..... (GND –0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
  LTC2328C ..... 0°C to 70°C
  LTC2328I ..... –40°C to 85°C
  LTC2328H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



MS PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER INFORMATION

http://www.linear.com/product/LTC2328-18#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2328CMS-18#PBF	LTC2328CMS-18#TRPBF	232818	16-Lead Plastic MSOP	0°C to 70°C
LTC2328IMS-18#PBF	LTC2328IMS-18#TRPBF	232818	16-Lead Plastic MSOP	–40°C to 85°C
LTC2328HMS-18#PBF	LTC2328HMS-18#TRPBF	232818	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Absolute Input Range (IN^+)	(Note 5)	●	$-2.5 \cdot V_{REFBUF} - 0.5$		$2.5 \cdot V_{REFBUF} + 0.5$	V
V_{IN}^-	Absolute Input Range (IN^-)	(Note 5)	●	–0.5		0.5	V
$V_{IN}^+ - V_{IN}^-$	Input Differential Voltage Range	$V_{IN} = V_{IN}^+ - V_{IN}^-$	●	$-2.5 \cdot V_{REFBUF}$		$2.5 \cdot V_{REFBUF}$	V
I_{IN}	Analog Input Current		●	–7.8		4.8	mA
C_{IN}	Analog Input Capacitance				5		pF
R_{IN}	Analog Input Resistance				2.083		kΩ
CMRR	Input Common Mode Rejection Ratio	f_{IN} = 500kHz			66		dB

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	18			Bits
	No Missing Codes		●	18			Bits
	Transition Noise				1.6		LSB_{RMS}
INL	Integral Linearity Error	(Note 6)	●	–5	±1	5	LSB
DNL	Differential Linearity Error		●	–1	±0.1	1.25	LSB
BZE	Bipolar Zero-Scale Error	(Note 7)	●	–30	0	30	LSB
	Bipolar Zero-Scale Error Drift				0.01		LSB/°C
FSE	Bipolar Full-Scale Error	V_{REFBUF} = 4.096V (REFBUF Overdriven) (Notes 7, 9)	●	–125		125	LSB
		REFIN = 2.048V (Note 7)	●	–150		150	LSB
	Bipolar Full-Scale Error Drift				±0.5		ppm/°C

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS. (Notes 4, 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	±6.25V Range, f_{IN} = 2kHz, REFIN = 1.25V	●	87.6	91		dB
		±10.24V Range, f_{IN} = 2kHz, REFIN = 2.048V	●	91	95		dB
		±12.5V Range, f_{IN} = 2kHz, REFBUF = 5V	●	92	96.5		dB
SNR	Signal-to-Noise Ratio	±6.25V Range, f_{IN} = 2kHz, REFIN = 1.25V	●	88	91.5		dB
		±10.24V Range, f_{IN} = 2kHz, REFIN = 2.048V	●	92	95		dB
		±12.5V Range, f_{IN} = 2kHz, REFBUF = 5V	●	94	97		dB
THD	Total Harmonic Distortion	±6.25V Range, f_{IN} = 2kHz, REFIN = 1.25V	●		–108	–98	dB
		±10.24V Range, f_{IN} = 2kHz, REFIN = 2.048V	●		–111	–98	dB
		±12.5V Range, f_{IN} = 2kHz, REFBUF = 5V	●		–106	–96	dB
SFDR	Spurious Free Dynamic Range	±6.25V Range, f_{IN} = 2kHz, REFIN = 1.25V	●	98	110		dB
		±10.24V Range, f_{IN} = 2kHz, REFIN = 2.048V	●	98	113		dB
		±12.5V Range, f_{IN} = 2kHz, REFBUF = 5V	●	96	108		dB
	–3dB Input Linear Bandwidth				7		MHz
	Aperture Delay				500		ps
	Aperture Jitter				4		ps_{RMS}
	Transient Response	Full-Scale Step			0.5		µs

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFIN}	Internal Reference Output Voltage			2.043	2.048	2.053	V
	V_{REFIN} Temperature Coefficient	(Note 14)	●		2	20	ppm/°C
	REFIN Output Impedance				15		kΩ
	V_{REFIN} Line Regulation	V_{DD} = 4.75V to 5.25V			0.08		mV/V
	REFIN Input Voltage Range	(REFIN Overdriven) (Note 5)		1.25		2.4	V

REFERENCE BUFFER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFBUF}	Reference Buffer Output Voltage	V_{REFIN} = 2.048V	●	4.091	4.096	4.101	V
	REFBUF Input Voltage Range	(REFBUF Overdriven) (Notes 5, 9)	●	2.5		5	V
	REFBUF Output Impedance	V_{REFIN} = 0V			13		kΩ
I_{REFBUF}	REFBUF Load Current	V_{REFBUF} = 5V (REFBUF Overdriven) (Notes 9, 10) V_{REFBUF} = 5V, Nap Mode (REFBUF Overdriven) (Note 9)	●		0.89 0.39	1.2	mA mA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	0.8 • OV_{DD}			V
V_{IL}	Low Level Input Voltage		●			0.2 • OV_{DD}	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_O = –500µA	●	OV_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	4.75	5	5.25	V
OV_{DD}	Supply Voltage		●	1.71		5.25	V
I_{VDD}	Supply Current	1Msps Sample Rate (IN^+ = –10.24V, IN^- = 0V)	●		14.5	16	mA
		1Msps Sample Rate (IN^+ = IN^- = 0V)			10		mA
I_{OVDD}	Supply Current	1Msps Sample Rate (C_L = 20pF)			0.4		mA
I_{NAP}	Nap Mode Current	Conversion Done (I_{VDD} + I_{OVDD}, IN^+ = –10.24V, IN^- = 0V)	●		8.4	10	mA
I_{SLEEP}	Sleep Mode Current	Sleep Mode (I_{VDD} + I_{OVDD})	●		60	225	µA
P_D	Power Dissipation	1Msps Sample Rate (IN^+ = –10.24V, IN^- = 0V)	●		72.5	80	mW
		1Msps Sample Rate (IN^+ = IN^- = 0V)			50		mW
	Nap Mode	Conversion Done (I_{VDD} + I_{OVDD}, IN^+ = –10.24V, IN^- = 0V)	●		42	50	mW
	Sleep Mode	Sleep Mode (I_{VDD} + I_{OVDD})	●		0.3	1.1	mW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Maximum Sampling Frequency		●			1	Msps
t_{CONV}	Conversion Time		●	460		527	ns
t_{ACQ}	Acquisition Time	t_{ACQ} = t_{CYC} – t_{CONV} – t_{BUSYLH} (Note 11)	●	460			ns
t_{CYC}	Time Between Conversions		●	1			µs
t_{CNVH}	CNV High Time		●	20			ns
t_{BUSYLH}	CNV↑ to BUSY Delay	C_L = 20pF	●			13	ns
t_{CNVL}	Minimum Low Time for CNV	(Note 12)	●	20			ns
t_{QUIET}	SCK Quiet Time from CNV↑	(Note 11)	●	20			ns
t_{SCK}	SCK Period	(Notes 12, 13)	●	10			ns
t_{SCKH}	SCK High Time		●	4			ns
t_{SCKL}	SCK Low Time		●	4			ns
$t_{SSDISCK}$	SDI Setup Time From SCK↑	(Note 12)	●	4			ns
$t_{HSDISCK}$	SDI Hold Time From SCK↑	(Note 12)	●	1			ns
t_{SCKCH}	SCK Period in Chain Mode	t_{SCKCH} = $t_{SSDISCK}$ + t_{DSDO} (Note 12)	●	13.5			ns
t_{DSDO}	SDO Data Valid Delay from SCK↑	C_L = 20pF, OV_{DD} = 5.25V	●			7.5	ns
		C_L = 20pF, OV_{DD} = 2.5V	●			8	ns
		C_L = 20pF, OV_{DD} = 1.71V	●			9.5	ns
t_{HSDO}	SDO Data Remains Valid Delay from SCK↑	C_L = 20pF (Note 11)	●	1			ns
$t_{DSDOBUSYL}$	SDO Data Valid Delay from BUSY↓	C_L = 20pF (Note 11)	●			5	ns
t_{EN}	Bus Enable Time After RDL↓	(Note 12)	●			16	ns
t_{DIS}	Bus Relinquish Time After RDL↑	(Note 12)	●			13	ns
t_{WAKE}	REFBUF Wakeup Time	C_{REFBUF} = 47µF, C_{REFIN} = 100nF			200		ms

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground or above V_{DD} or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground or above V_{DD} or OV_{DD} without latch-up.

Note 4: V_{DD} = 5V, OV_{DD} = 2.5V, ±10.24V Range, REFIN = 2.048V, f_{SMPL} = 1MHz.

Note 5: Recommended operating conditions.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Bipolar zero error is the offset voltage measured from –0.5LSB when the output code flickers between 00 0000 0000 0000 0000 and 11 1111 1111 1111 1111. Full-scale bipolar error is the worst-case of –FS or +FS untrimmed deviation from ideal first and last code transitions and includes the effect of offset error.

Note 8: All specifications in dB are referred to a full-scale ±10.24V input with REFIN = 2.048V.

Note 9: When REFBUF is overdriven, the internal reference buffer must be turned off by setting REFIN = 0V.

Note 10: f_{SMPL} = 1MHz, I_{REFBUF} varies proportionally with sample rate.

Note 11: Guaranteed by design, not subject to test.

Note 12: Parameter tested and guaranteed at OV_{DD} = 1.71V, OV_{DD} = 2.5V and OV_{DD} = 5.25V.

Note 13: t_{SCK} of 10ns maximum allows a shift clock frequency up to 100MHz for rising edge capture.

Note 14: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

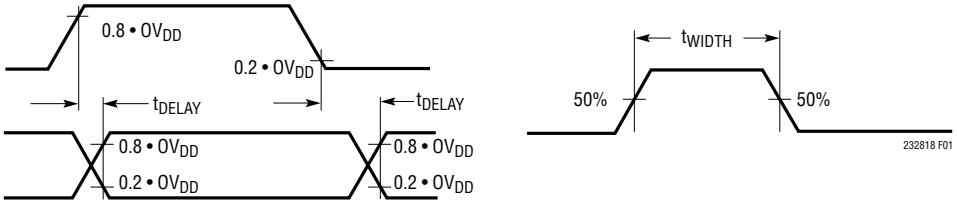
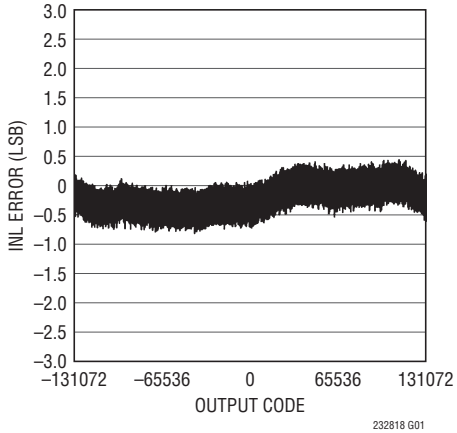


Figure 1. Voltage Levels for Timing Specifications

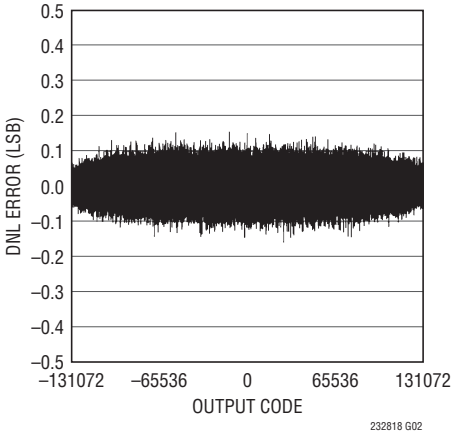
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, f_{SMPL} = 1Msps, unless otherwise noted.

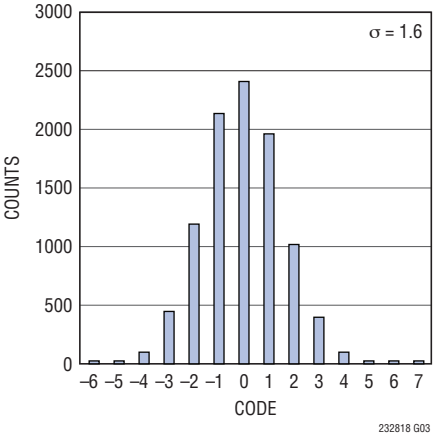
Integral Nonlinearity vs Output Code



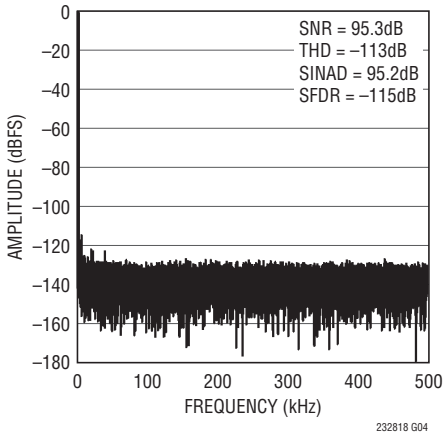
Differential Nonlinearity vs Output Code



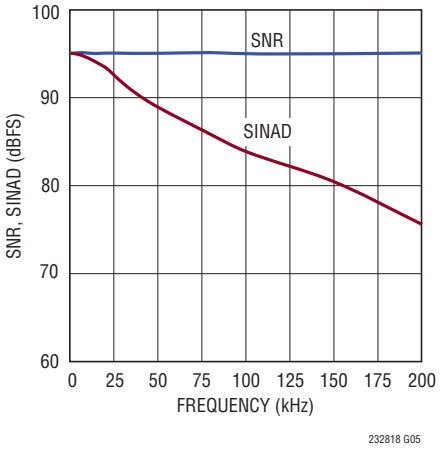
DC Histogram



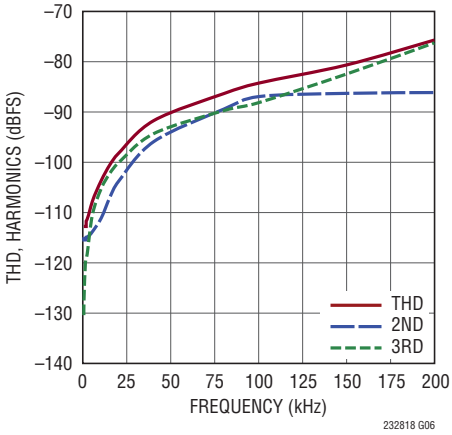
32k Point FFT f_S = 1Msps, f_{IN} = 2kHz



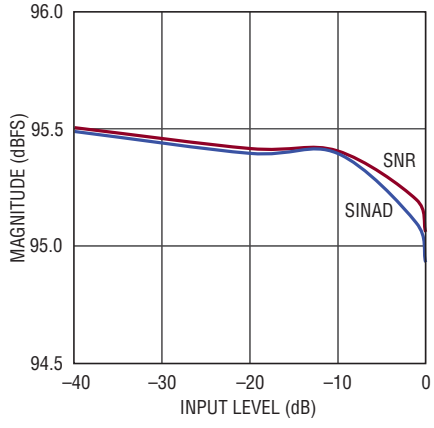
SNR, SINAD vs Input Frequency



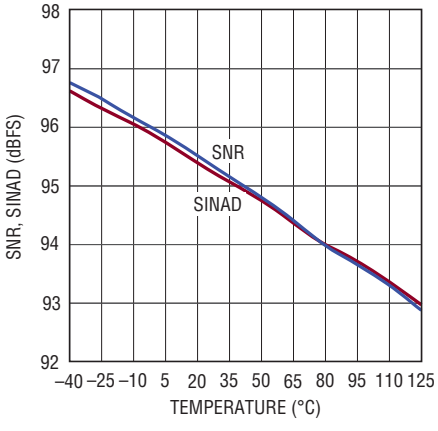
THD, Harmonics vs Input Frequency



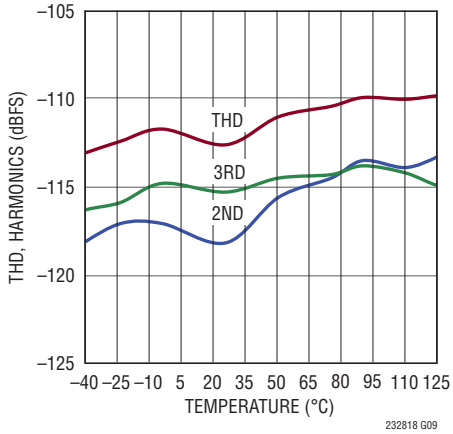
SNR, SINAD vs Input Level, f_{IN} = 2kHz



SNR, SINAD vs Temperature, f_{IN} = 2kHz



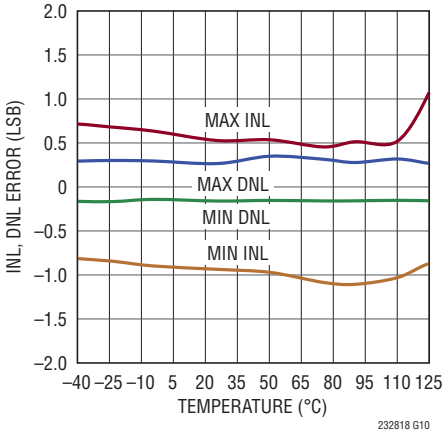
THD, Harmonics vs Temperature, f_{IN} = 2kHz



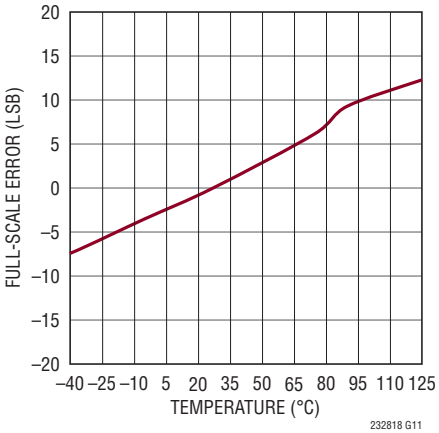
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, f_{SMPL} = 1Msps, unless otherwise noted.

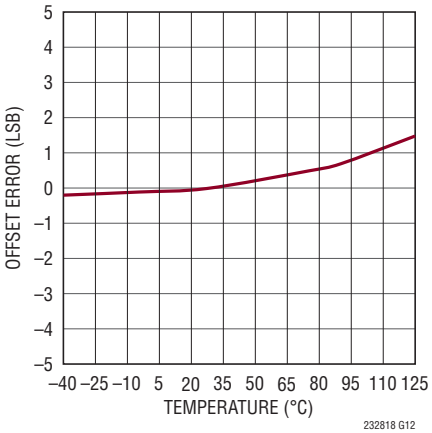
INL/DNL vs Temperature



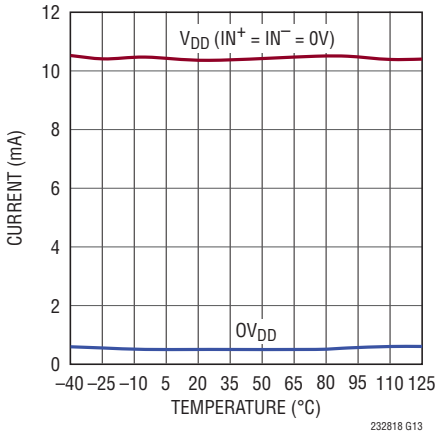
Full-Scale Error vs Temperature



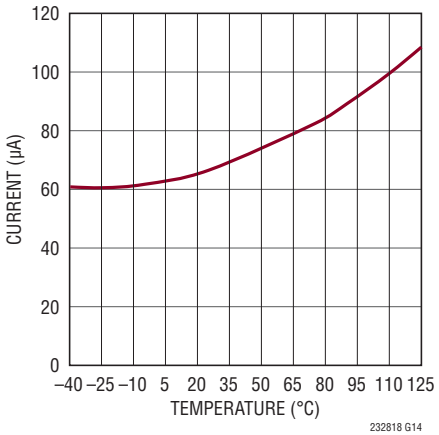
Offset Error vs Temperature



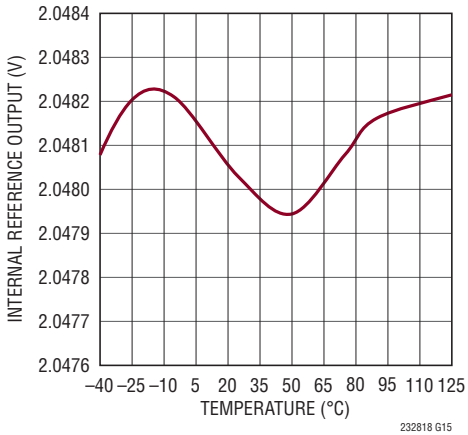
Supply Current vs Temperature



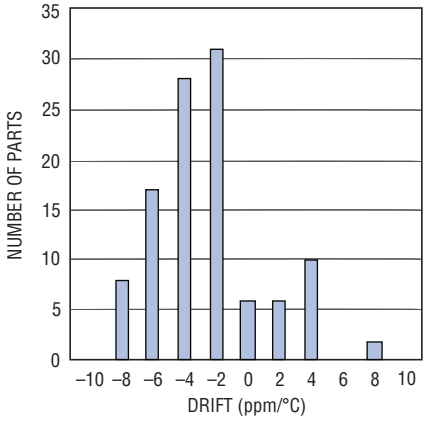
Sleep Current vs Temperature



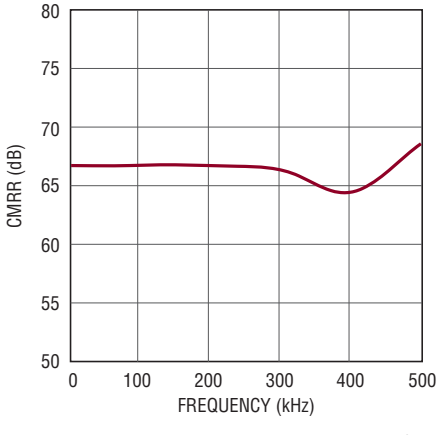
Internal Reference Output vs Temperature



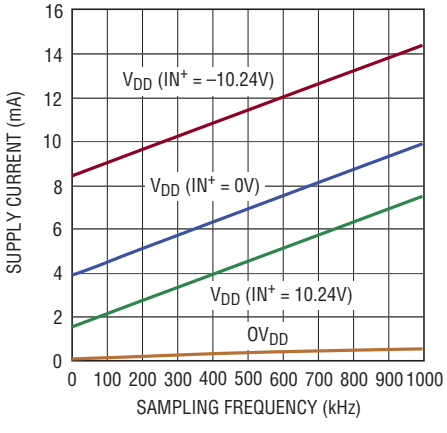
Internal Reference Output Temperature Coefficient Distribution



CMRR vs Input Frequency



Supply Current vs Sampling Rate



PIN FUNCTIONS

V_{DDLBYP} (Pin 1): 2.5V Supply Bypass Pin. The voltage on this pin is generated via an onboard regulator off of V_{DD}. This pin must be bypassed with a 2.2µF ceramic capacitor to GND.

V_{DD} (Pin 2): 5V Power Supply. The range of V_{DD} is 4.75V to 5.25V. Bypass V_{DD} to GND with a 10µF ceramic capacitor.

GND (Pins 3, 6 and 16): Ground.

IN^+ (Pin 4): Analog Input. IN^+ operates differential with respect to IN^- with an IN^+-IN^- range of $–2.5 • V_{REFBUF}$ to $2.5 • V_{REFBUF}$.

IN^- (Pin 5): Analog Ground Sense. IN^- has an input range of ±500mV with respect to GND and must be tied to the ground plane or a remote sense.

REFBUF (Pin 7): Reference Buffer Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 47µF ceramic capacitor. The internal buffer driving this pin may be disabled by grounding its input at REFIN. Once the buffer is disabled, an external reference may overdrive this pin in the range of 2.5V to 5V. A resistive load greater than 500kΩ can be placed on the reference buffer output.

REFIN (Pin 8): Reference Output/Reference Buffer Input. An onboard bandgap reference nominally outputs 2.048V at this pin. Bypass this pin with a 100nF ceramic capacitor to GND to limit the reference output noise. If more accuracy is desired, this pin may be overdriven by an external reference in the range of 1.25V to 2.4V.

CNV (Pin 9): Convert Input. A rising edge on this input powers up the part and initiates a new conversion. Logic levels are determined by OV_{DD}.

CHAIN (Pin 10): Chain Mode Selector Pin. When low, the LTC2328-18 operates in normal mode and the RDL/SDI input pin functions to enable or disable SDO. When high, the LTC2328-18 operates in chain mode and the RDL/SDI pin functions as SDI, the daisy-chain serial data input. Logic levels are determined by OV_{DD}.

BUSY (Pin 11): BUSY Indicator. Goes high at the start of a new conversion and returns low when the conversion has finished. Logic levels are determined by OV_{DD}.

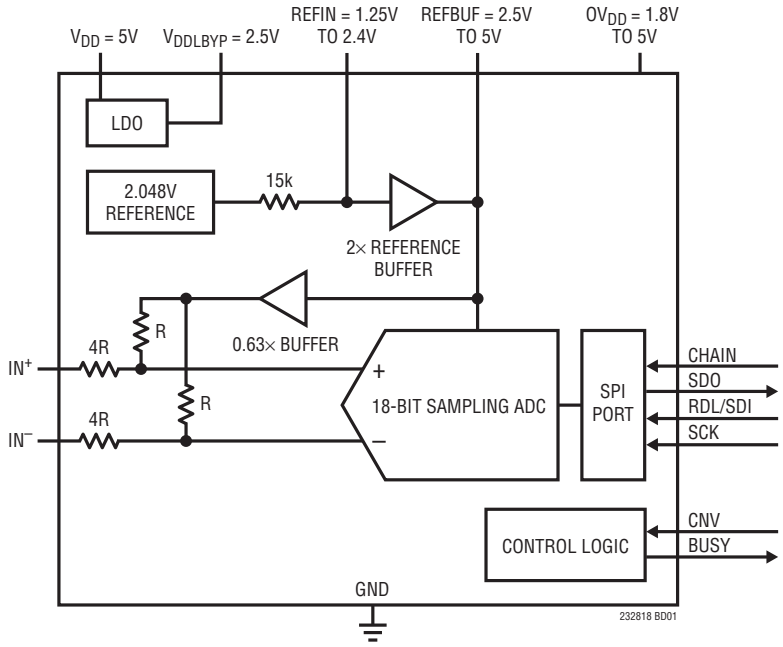
RDL/SDI (Pin 12): When CHAIN is low, the part is in normal mode and the pin is treated as a bus enabling input. When CHAIN is high, the part is in chain mode and the pin is treated as a serial data input pin where data from another ADC in the daisy chain is input. Logic levels are determined by OV_{DD}.

SCK (Pin 13): Serial Data Clock Input. When SDO is enabled, the conversion result or daisy-chain data from another ADC is shifted out on the rising edges of this clock MSB first. Logic levels are determined by OV_{DD}.

SDO (Pin 14): Serial Data Output. The conversion result or daisy-chain data is output on this pin on each rising edge of SCK MSB first. The output data is in 2's complement format. Logic levels are determined by OV_{DD}.

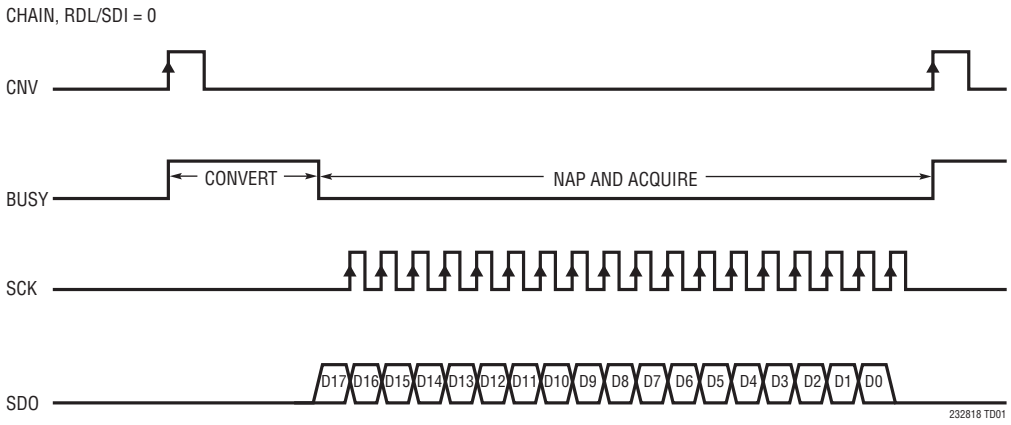
OV_{DD} (Pin 15): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 5.25V. This supply is nominally set to the same supply as the host interface (1.8V, 2.5V, 3.3V, or 5V). Bypass OV_{DD} to GND with a 0.1µF capacitor.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM

Conversion Timing Using the Serial Interface



APPLICATIONS INFORMATION

OVERVIEW

The LTC2328-18 is a low noise, high speed 18-bit successive approximation register (SAR) ADC with pseudo-differential inputs. Operating from a single 5V supply, the LTC2328-18 has a ±10.24V true bipolar input range, making it ideal for high voltage applications which require a wide dynamic range. The LTC2328-18 achieves ±5LSB INL maximum, no missing codes at 18-bits and 95dB SNR.

The LTC2328-18 has an onboard single-shot capable reference buffer and low drift (20ppm/°C max) 2.048V temperature-compensated reference. The LTC2328-18 also has a high speed SPI-compatible serial interface that supports 1.8V, 2.5V, 3.3V and 5V logic while also featuring a daisy-chain mode. The fast 1Msps throughput with no cycle latency makes the LTC2328-18 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2328-18 dissipates only 50mW and automatically naps between conversions, leading to reduced power dissipation that scales with the sampling rate. A sleep mode is also provided to reduce the power consumption of the LTC2328-18 to 300µW for further power savings during inactive periods.

CONVERTER OPERATION

The LTC2328-18 operates in two phases. During the acquisition phase, the charge redistribution capacitor D/A converter (CDAC) is connected to the outputs of the resistor divider networks that pins IN^+ and IN^- drive to sample an attenuated and level-shifted version of the pseudo-differential analog input voltage as shown in Figure 3. A rising edge on the CNV pin initiates a conversion. During the conversion phase, the 18-bit CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g. $V_{REFBUF}/2$, $V_{REFBUF}/4$ … $V_{REFBUF}/262144$) using the differential comparator. At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then prepares the 18-bit digital output code for serial transfer.

TRANSFER FUNCTION

The LTC2328-18 digitizes the full-scale voltage of ±2.5 • REFBUF into 2^{18} levels, resulting in an LSB size of 78µV with REFBUF = 4.096V. The ideal transfer function is shown in Figure 2. The output data is in 2's complement format.

ANALOG INPUT

The analog inputs of the LTC2328-18 are pseudo-differential in order to reduce any unwanted signal that is common to both inputs. The analog inputs can be modeled by the equivalent circuit shown in Figure 3. The back-to-back diodes at the inputs form clamps that provide ESD protection. Each input drives a resistor divider network that has

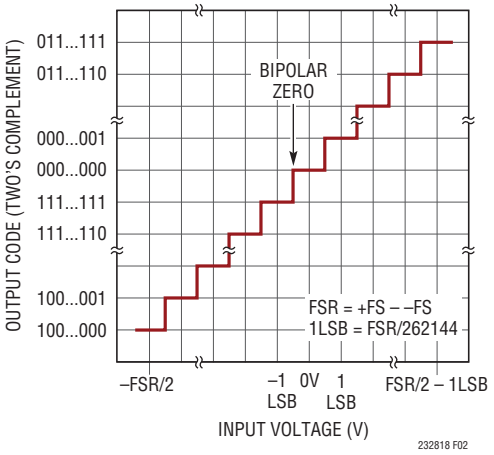


Figure 2. LTC2328-18 Transfer Function

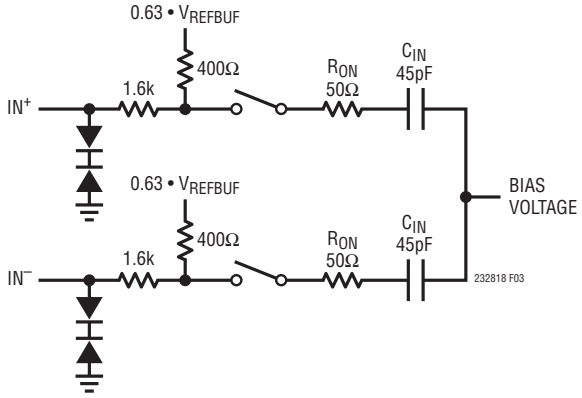


Figure 3. The Equivalent Circuit for the Differential Analog Input of the LTC2328-18

APPLICATIONS INFORMATION

a total impedance of 2kΩ. The resistor divider network attenuates and level shifts the ±2.5 • REFBUF true bipolar signal swing of each input to the 0-REFBUF input signal swing of the ADC core. In the acquisition phase, 45pF (C_{IN}) from the sampling CDAC in series with approximately 50Ω (R_{ON}) from the on-resistance of the sampling switch is connected to the output of the resistor divider network. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC core and resistor divider network. The IN^+ input of the ADC core draws a current spike while charging the C_{IN} capacitor during acquisition.

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance input of the LTC2328-18 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC. Minimizing settling time is important even for DC inputs, because the ADC input draws a current spike when entering acquisition.

For best performance, a buffer amplifier should be used to drive the analog input of the LTC2328-18. The amplifier provides low output impedance to minimize gain error and allows for fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC input which draws a small current spike during acquisition.

Input Filtering

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with a low bandwidth filter to minimize noise. The simple 1-pole RC lowpass filter shown in Figure 4 is sufficient for many applications.

The input resistor divider network, sampling switch on-resistance (R_{ON}) and the sample capacitor (C_{IN}) form a second lowpass filter that limits the input bandwidth to the ADC core to 7MHz. A buffer amplifier with a low noise density must be selected to minimize the degradation of the SNR over this bandwidth.

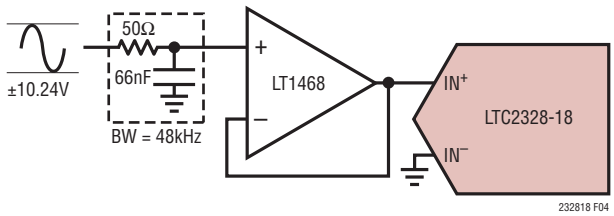


Figure 4. Input Signal Chain

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Pseudo-Differential Bipolar Inputs

For most applications, we recommend the low power LT1468 ADC driver to drive the LTC2328-18. With a low noise density of 5nV/$\sqrt{Hz}$ and a low supply current of 3mA, the LT1468 is flexible and may be configured to convert signals of various amplitudes to the ±10.24V input range of the LTC2328-18.

To achieve the full distortion performance of the LTC2328-18, a low distortion single-ended signal source driven through the LT1468 configured as a unity-gain buffer as shown in Figure 4 can be used to get the full data sheet THD specification of –111dB.

ADC REFERENCE

There are three ways of providing the ADC reference. The first is to use both the internal reference and reference buffer. The second is to externally overdrive the internal reference and use the internal reference buffer. The third is to disable the internal reference buffer and overdrive the REFBUF pin from an external source. The following tables give examples of these cases and the resulting bipolar input ranges.

APPLICATIONS INFORMATION

Table 1. Internal Reference with Internal Buffer

REFIN	REFBUF	BIPOLAR INPUT RANGE
2.048V	4.096V	±10.24V

Table 2. External Reference with Internal Buffer

REFIN (OVERDRIVE)	REFBUF	BIPOLAR INPUT RANGE
1.25V (Min)	2.5V	±6.25V
2.048V	4.096V	±10.24V
2.4V (Max)	4.8V	±12V

Table 3. External Reference Unbuffered

REFIN	REFBUF (OVERDRIVE)	BIPOLAR INPUT RANGE
0V	2.5V (Min)	±6.25V
0V	5V (Max)	±12.5V

Internal Reference with Internal Buffer

The LTC2328-18 has an on-chip, low noise, low drift (20ppm/°C max), temperature compensated bandgap reference that is factory trimmed to 2.048V. It is internally connected to a reference buffer as shown in Figure 5a and is available at REFIN (Pin 8). REFIN should be bypassed to GND with a 100nF ceramic capacitor to minimize noise. The reference buffer gains the REFIN voltage by 2 to 4.096V at REFBUF (Pin 7). So the input range is ±10.24V, as shown in Table 1. Bypass REFBUF to GND with at least a 47µF ceramic capacitor (X7R, 10V, 1210 size) to compensate the reference buffer and minimize noise.

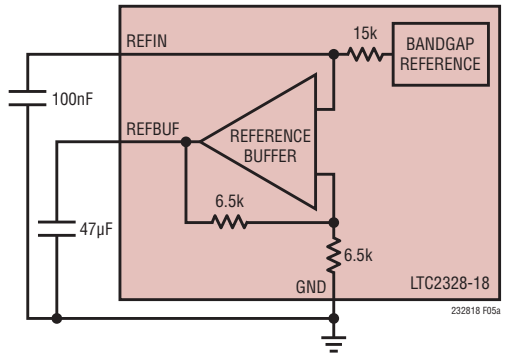


Figure 5a. LTC2328-18 Internal Reference Circuit

External Reference with Internal Buffer

If more accuracy and/or lower drift is desired, REFIN can be easily overdriven by an external reference since a 15k resistor is in series with the reference as shown in Figure 5b. REFIN can be overdriven in the range from 1.25V to 2.4V. The resulting voltage at REFBUF will be 2 • REFIN. So the input range is ±5 • REFIN, as shown in Table 2. Linear Technology offers a portfolio of high performance references designed to meet the needs of many applications. With its small size, low power, and high accuracy, the LTC6655-2.048 is well suited for use with the LTC2328-18 when overdriving the internal reference. The LTC6655-2.048 offers 0.025% (max) initial accuracy and 2ppm/°C (max) temperature coefficient for high precision applications. The LTC6655-2.048 is fully specified over the H-grade temperature range and complements the extended temperature range of the LTC2328-18 up to 125°C. Bypassing the LTC6655-2.048 with a 2.7µF to 100µF ceramic capacitor close to the REFIN pin is recommended.

External Reference Unbuffered

The internal reference buffer can also be overdriven from 2.5V to 5V with an external reference at REFBUF as shown in Figure 5c. So the input ranges are ±6.25V to ±12.5V, respectively, as shown in Table 3. To do so, REFIN must be grounded to disable the reference buffer. A 13k resistor loads the REFBUF pin when the reference buffer is disabled. To maximize the input signal swing and corresponding SNR, the LTC6655-5 is recommended when overdriving REFBUF. The LTC6655-5 offers the same small size, accuracy, drift and extended temperature range as the LTC6655-2.048. By using this 5V reference, an SNR of 97dB can be achieved. Bypassing the LTC6655-5 with a 47µF ceramic capacitor (X5R, 0805 size) close to the REFBUF pin is recommended.

The REFBUF pin of the LTC2328-18 draws a charge (Q_{CONV}) from the external bypass capacitor during each conversion cycle. If the internal reference buffer is overdriven, the external reference must provide all of this charge with a DC current equivalent to $I_{REFBUF} = Q_{CONV}/t_{CYC}$. Thus, the DC current draw of REFBUF depends on the sampling

APPLICATIONS INFORMATION

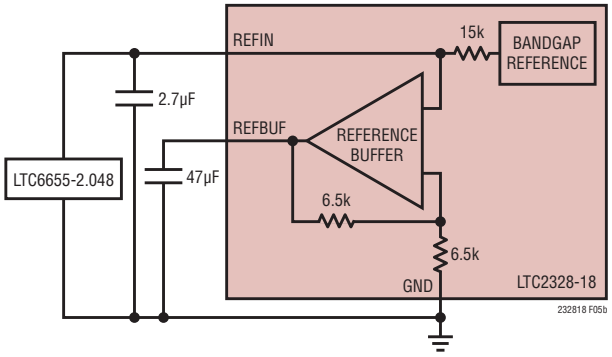


Figure 5b. Using the LTC6655-2.048 as an External Reference

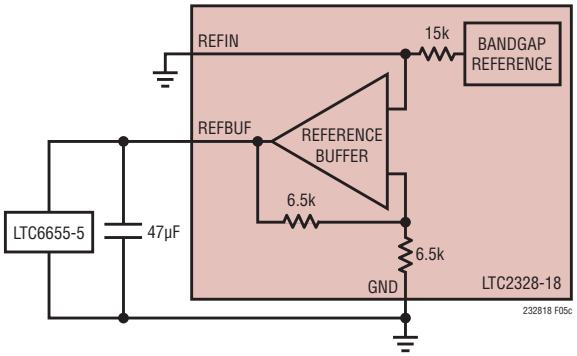


Figure 5c. Overdriving REFBUF Using the LTC6655-5

rate and output code. In applications where a burst of samples is taken after idling for long periods, as shown in Figure 6, I_{REFBUF} quickly goes from approximately 390µA to a maximum of 1.2mA for REFBUF = 5V at 1Msps. This step in DC current draw triggers a transient response in the external reference that must be considered since any deviation in the voltage at REFBUF will affect the accuracy of the output code. If an external reference is used to overdrive REFBUF, the fast settling LTC6655-5 reference is recommended.

Internal Reference Buffer Transient Response

For optimum transient performance, the internal reference buffer should be used. The internal reference buffer uses a proprietary design that results in an output voltage change at REFBUF of less than 1LSB when responding to a sudden burst of conversions. This makes the internal reference buffer of the LTC2328-18 truly single-shot capable since the first sample taken after idling will yield the same result as a sample taken after the transient response of the internal reference buffer has settled. Figure 7 shows the transient responses of the LTC2328-18 with the internal reference buffer and with the internal reference buffer overdriven by the LTC6655-5, both with a bypass capacitance of 47µF.

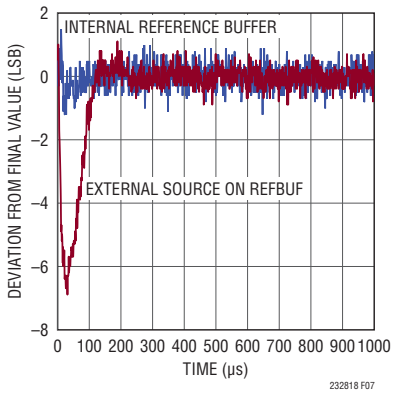


Figure 7. Transient Response of the LTC2328-18

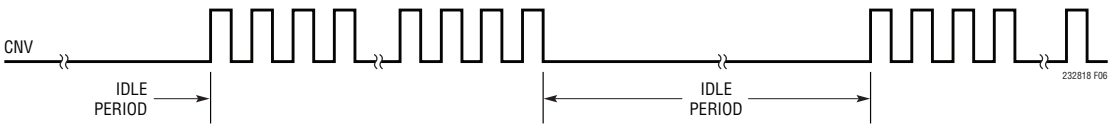


Figure 6. CNV Waveform Showing Burst Sampling

APPLICATIONS INFORMATION

DYNAMIC PERFORMANCE

Fast Fourier Transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2328-18 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 8 shows that the LTC2328-18 achieves a typical SINAD of 95dB at a 1MHz sampling rate with a 2kHz input.

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 8 shows that the LTC2328-18 achieves a typical SNR of 95dB at a 1MHz sampling rate with a 2kHz input.

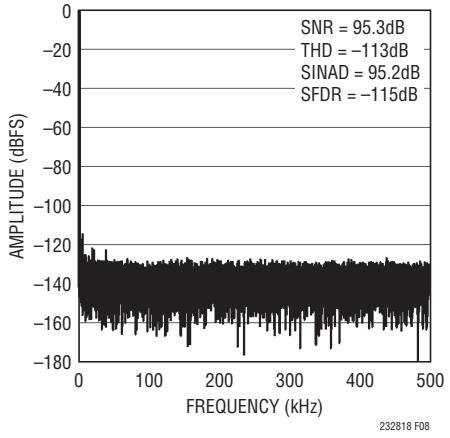


Figure 8. 32k Point FFT of the LTC2328-18

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots + V_N{}^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through V_N are the amplitudes of the second through Nth harmonics.

POWER CONSIDERATIONS

The LTC2328-18 provides two power supply pins: the 5V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2328-18 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

Power Supply Sequencing

The LTC2328-18 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2328-18 has a power-on reset (POR) circuit that will reset the LTC2328-18 at initial power-up or whenever the power supply voltage drops below 2V. Once the supply voltage reenters the nominal supply voltage range, the POR will re-initialize the ADC. No conversions should be initiated until 200µs after a POR event to ensure the re-initialization period has ended. Any conversions initiated before this time will produce invalid results.

TIMING AND CONTROL

CNV Timing

The LTC2328-18 conversion is controlled by CNV. A rising edge on CNV will start a conversion and power up the LTC2328-18. Once a conversion has been initiated,

APPLICATIONS INFORMATION

it cannot be restarted until the conversion is complete. For optimum performance, CNV should be driven by a clean low jitter signal. Converter status is indicated by the BUSY output which remains high while the conversion is in progress. To ensure that no errors occur in the digitized results, any additional transitions on CNV should occur within 40ns from the start of the conversion or after the conversion has been completed. Once the conversion has completed, the LTC2328-18 powers down and begins acquiring the input signal.

Internal Conversion Clock

The LTC2328-18 has an internal clock that is trimmed to achieve a maximum conversion time of 527ns. With a minimum acquisition time of 460ns, throughput performance of 1Msps is guaranteed without any external adjustments.

Auto Nap Mode

The LTC2328-18 automatically enters nap mode after a conversion has been completed and completely powers up once a new conversion is initiated on the rising edge of CNV. During nap mode, only the ADC core powers down and all other circuits remain active. During nap, data from the last conversion can be clocked out. The auto nap mode feature will reduce the power dissipation of the LTC2328-18 as the sampling frequency is reduced. Since full power is consumed only during a conversion, the ADC core of the LTC2328-18 remains powered down for a larger fraction of the conversion cycle (t_{CYC}) at lower sample rates, thereby reducing the average power dissipation which scales with the sampling rate as shown in Figure 9.

Sleep Mode

The auto nap mode feature provides limited power savings since only the ADC core powers down. To obtain greater power savings, the LTC2328-18 provides a sleep mode. During sleep mode, the entire part is powered down except for a small standby current resulting in a power dissipation of 300µW. To enter sleep mode, toggle CNV twice with no intervening rising edge on SCK. The part will enter sleep mode on the falling edge of BUSY from the last conversion initiated. Once in sleep mode, a rising edge on SCK will wake the part up. Upon emerging from sleep mode, wait t_{WAKE} ms before initiating a conversion to allow the reference and reference buffer to wake up and charge the bypass capacitors at REFIN and REFBUF. (Refer to the Timing Diagrams section for more detailed timing information about sleep mode.)

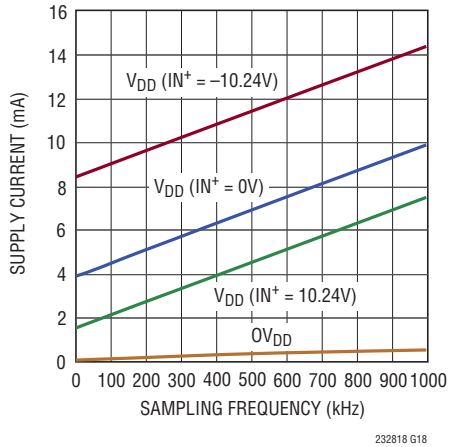


Figure 9. Power Supply Current of the LTC2328-18 Versus Sampling Rate

DIGITAL INTERFACE

The LTC2328-18 has a serial digital interface. The flexible OV_{DD} supply allows the LTC2328-18 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

The serial output data is clocked out on the SDO pin when an external clock is applied to the SCK pin if SDO is enabled. Clocking out the data after the conversion will yield the best performance. With a shift clock frequency of at least 40MHz, a 1Msps throughput is still achieved. The serial output data changes state on the rising edge of SCK and can be captured on the falling edge or next rising edge of SCK. D17 remains valid till the first rising edge of SCK.

The serial interface on the LTC2328-18 is simple and straightforward to use. The following sections describe the operation of the LTC2328-18. Several modes are provided depending on whether a single or multiple ADCs share the SPI bus or are daisy-chained.

APPLICATIONS INFORMATION

Normal Mode, Single Device

When CHAIN = 0, the LTC2328-18 operates in normal mode. In normal mode, RDL/SDI enables or disables the serial data output pin SDO. If RDL/SDI is high, SDO is in high impedance. If RDL/SDI is low, SDO is driven. Figure 10 shows a single LTC2328-18 operated in normal mode with CHAIN and RDL/SDI tied to ground. With RDL/SDI grounded, SDO is enabled and the MSB(D17) of the new conversion data is available at the falling edge of BUSY. This is the simplest way to operate the LTC2328-18.

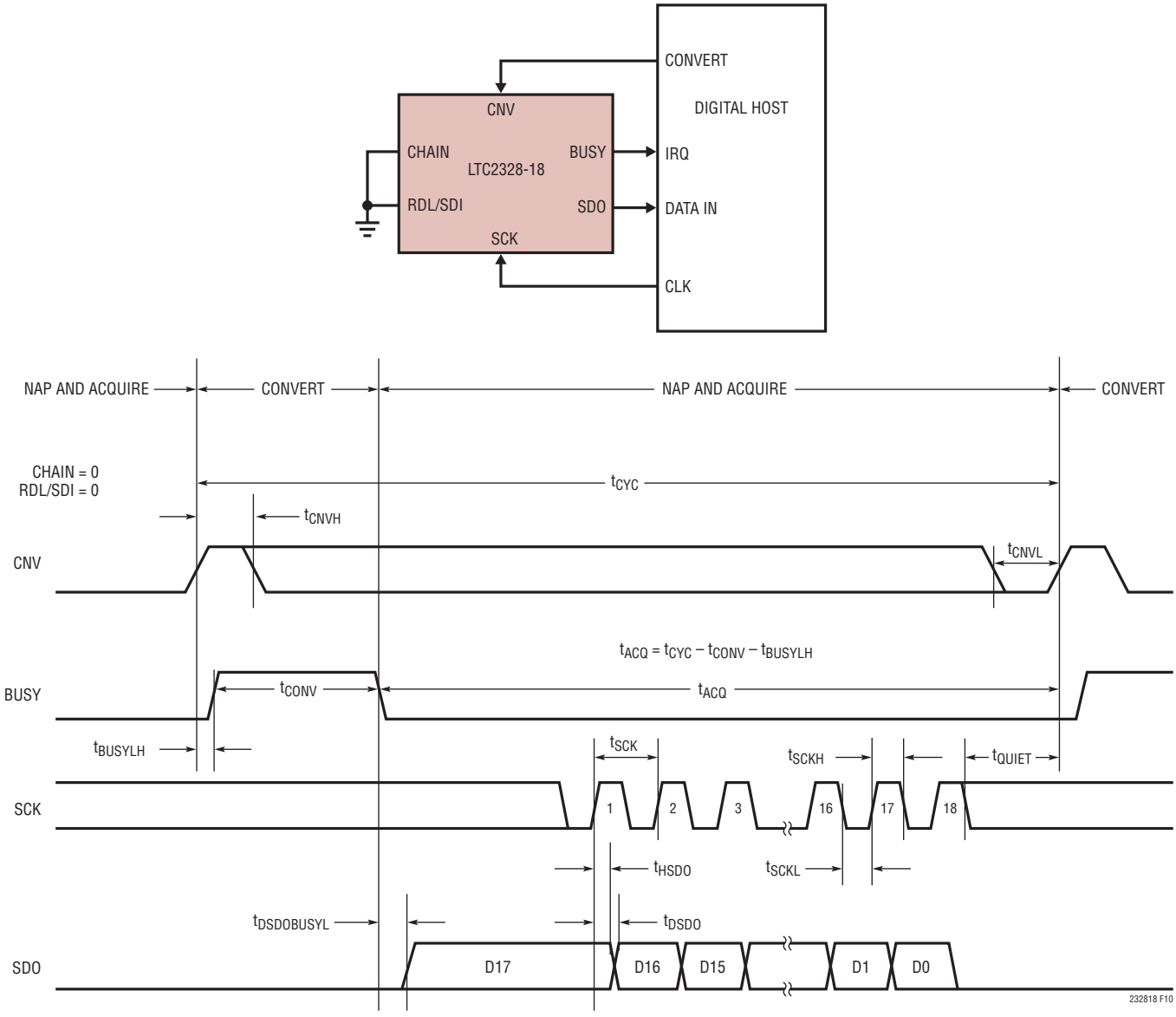


Figure 10. Using a Single LTC2328-18 in Normal Mode

APPLICATIONS INFORMATION

Normal Mode, Multiple Devices

Figure 11 shows multiple LTC2328-18 devices operating in normal mode (CHAIN = 0) sharing CNV, SCK and SDO. By sharing CNV, SCK and SDO, the number of required signals to operate multiple ADCs in parallel is reduced. Since SDO is shared, the RDL/SDI input of each ADC must be used to allow only one LTC2328-18 to drive SDO at a time in order to avoid bus conflicts. As shown in Figure 11, the RDL/SDI inputs idle high and are individually brought low to read data out of each device between conversions. When RDL/SDI is brought low, the MSB of the selected device is output onto SDO.

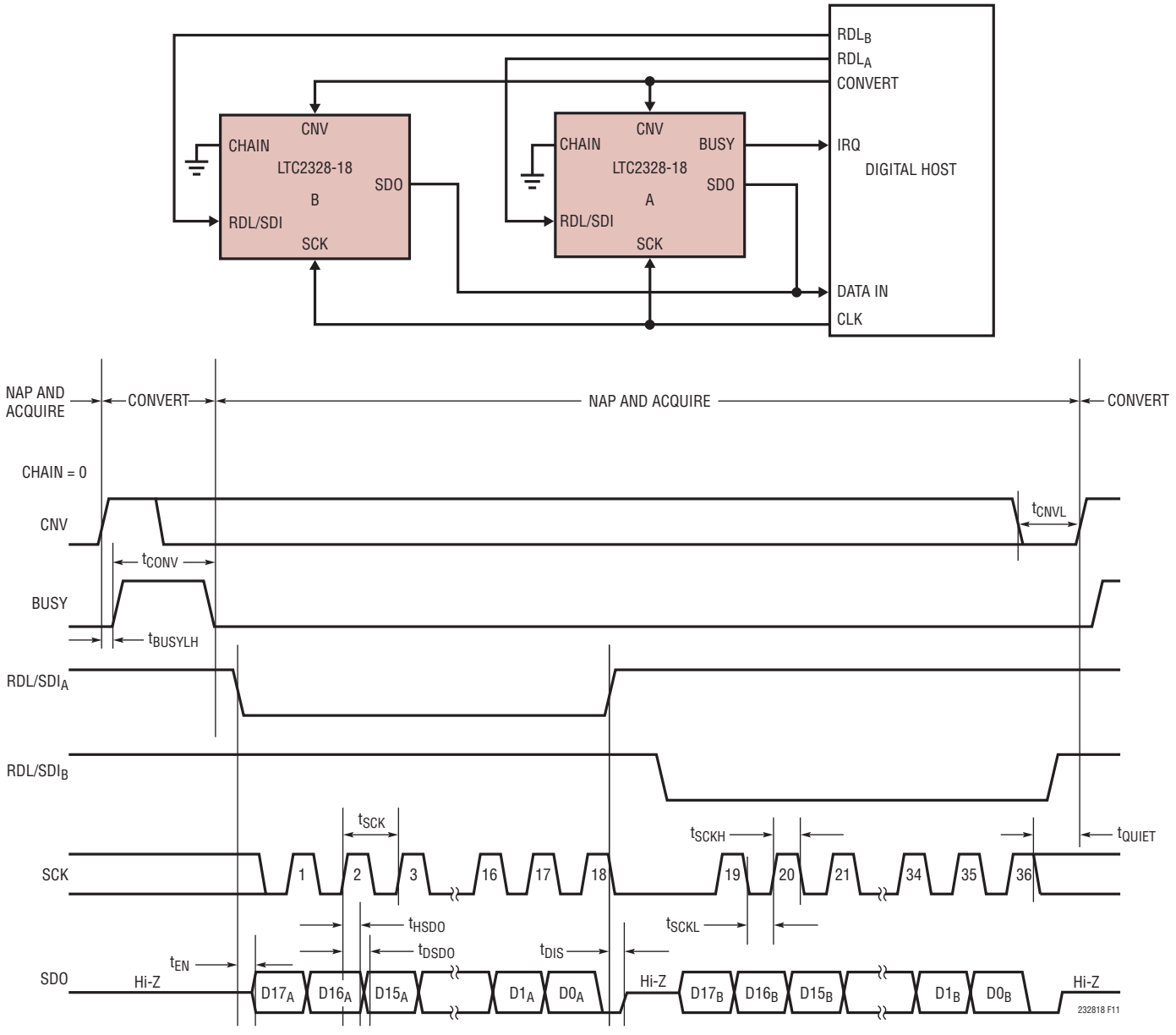


Figure 11. Normal Mode with Multiple Devices Sharing CNV, SCK, and SDO

APPLICATIONS INFORMATION

Chain Mode, Multiple Devices

When CHAIN = OV_{DD}, the LTC2328-18 operates in chain mode. In chain mode, SDO is always enabled and RDL/SDI serves as the serial data input pin (SDI) where daisy-chain data output from another ADC can be input. This is useful for applications where hardware constraints may limit the number of lines needed to interface to a large number of converters. Figure 12 shows an example with two daisy-chained devices. The MSB of converter A will appear at SDO of converter B after 18 SCK cycles. The MSB of converter A is clocked in at the SDI/RDL pin of converter B on the rising edge of the first SCK.

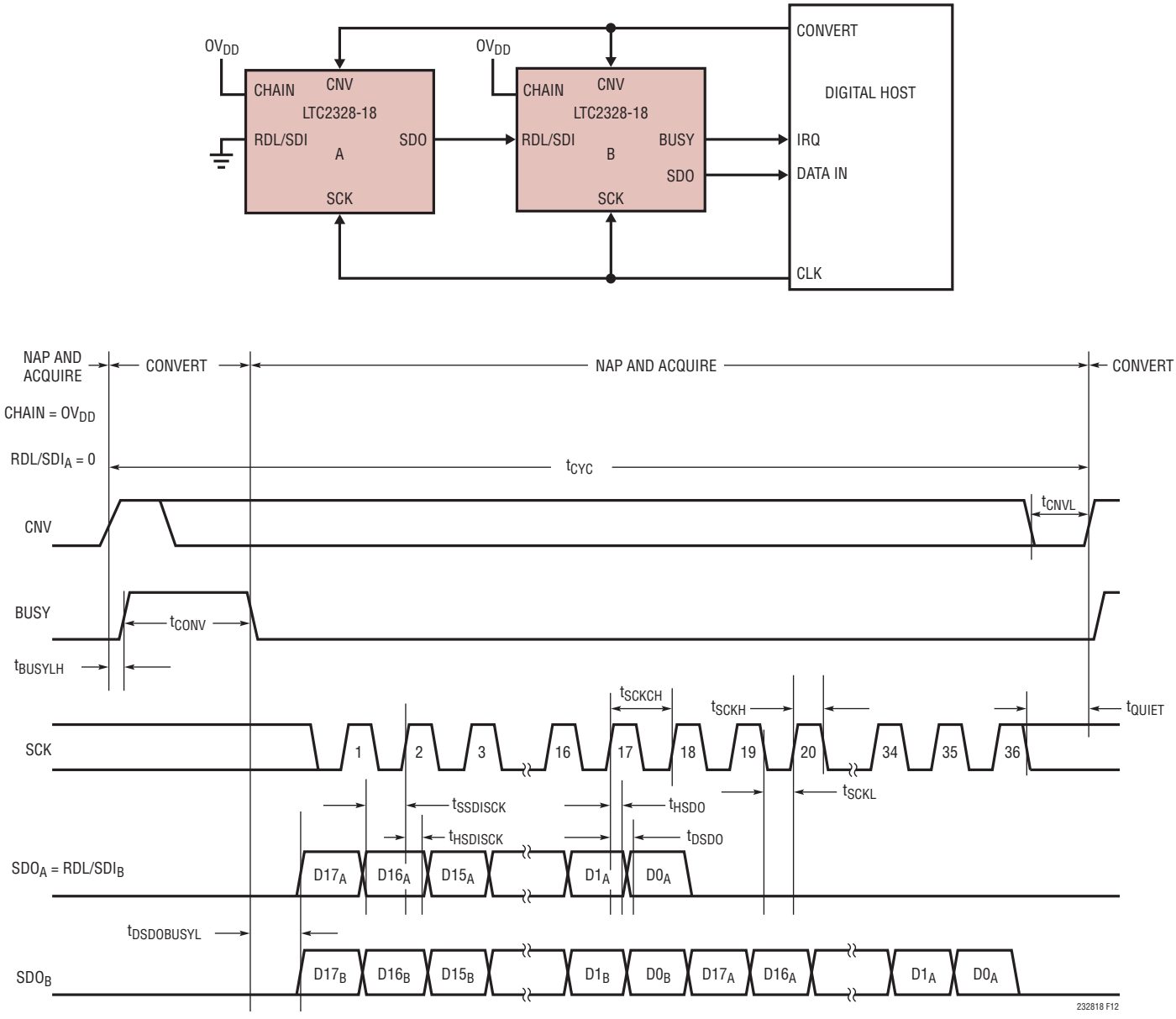


Figure 12. Chain Mode Timing Diagram

APPLICATIONS INFORMATION

Sleep Mode

To enter sleep mode, toggle CNV twice with no intervening rising edge on SCK as shown in Figure 13. The part will enter sleep mode on the falling edge of BUSY from the last conversion initiated. Once in sleep mode, a rising edge on SCK will wake the part up. Upon emerging from sleep mode, wait t_{WAKE} ms before initiating a conversion to allow the reference and reference buffer to wake up and charge the bypass capacitors at REFIN and REFBUF.

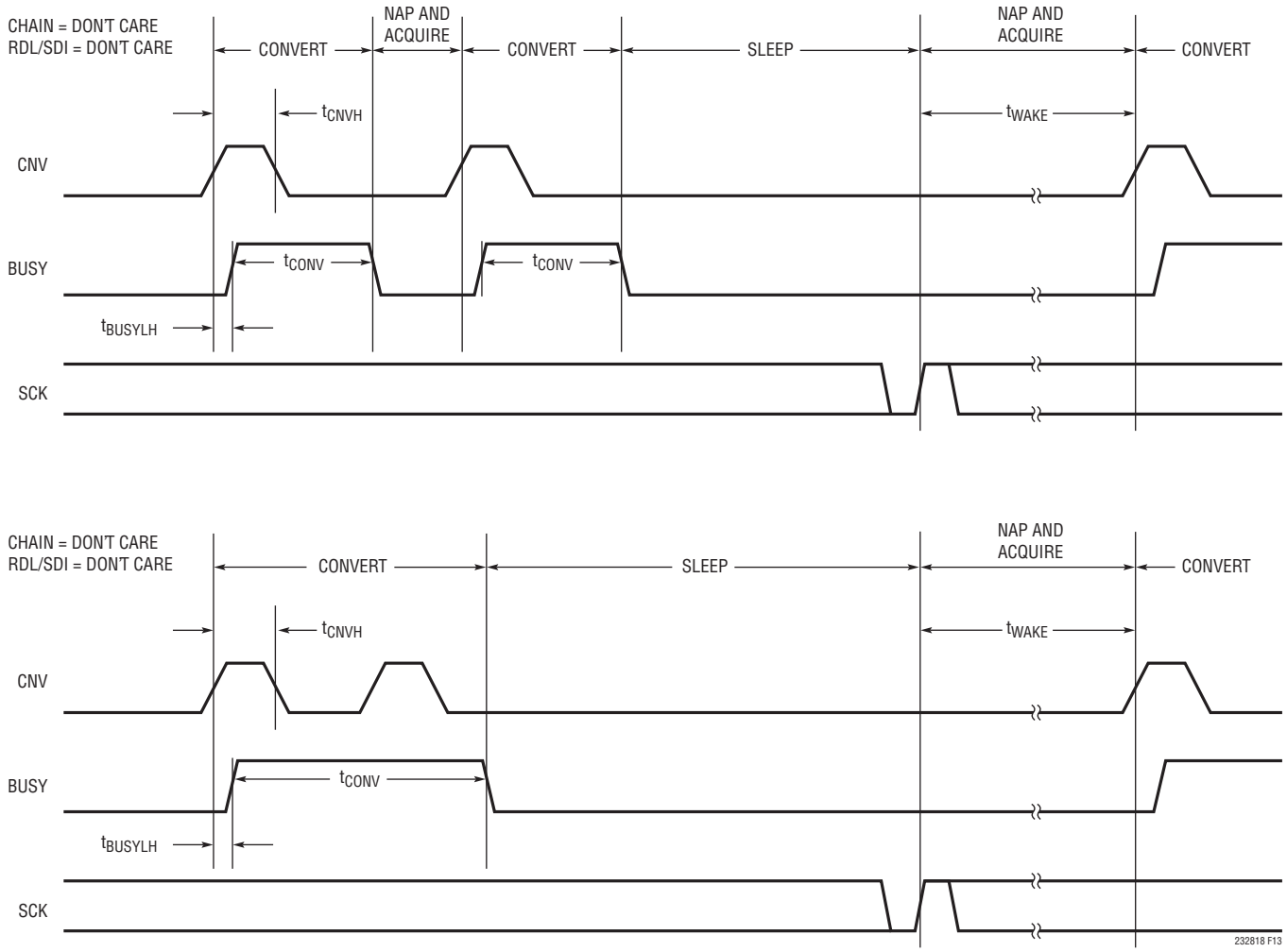


Figure 13. Sleep Mode Timing Diagram

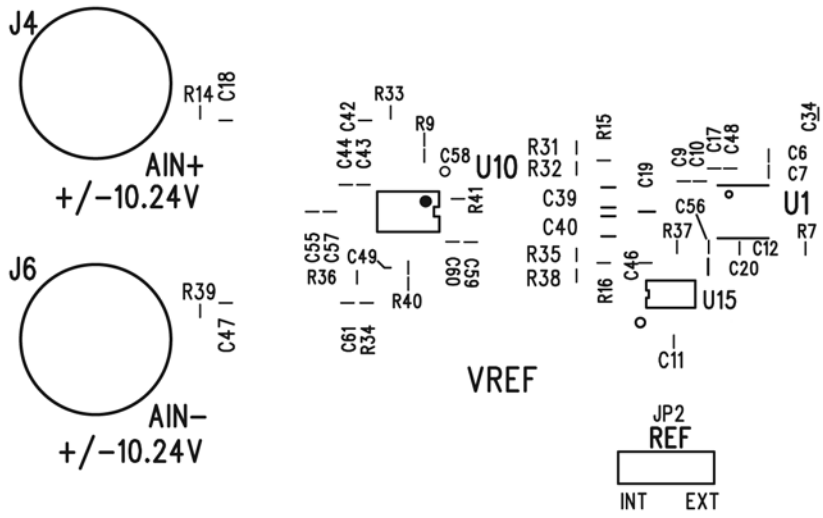
BOARD LAYOUT

To obtain the best performance from the LTC2328-18 a printed circuit board (PCB) is recommended. Layout for the PCB should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals alongside analog signals or underneath the ADC.

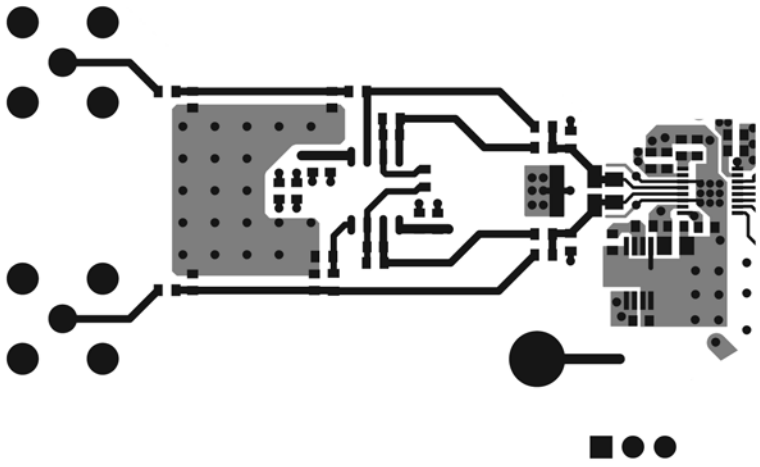
Recommended Layout

The following is an example of a recommended PCB layout. A single solid ground plane is used. Bypass capacitors to the supplies are placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. The analog input traces are screened by ground. For more details and information refer to DC1908, the evaluation kit for the LTC2328-18.

Partial Top Silkscreen

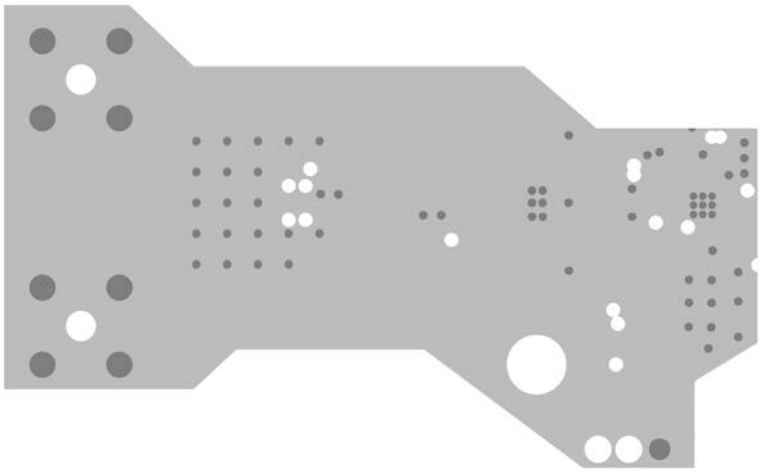


Partial Layer 1 Component Side

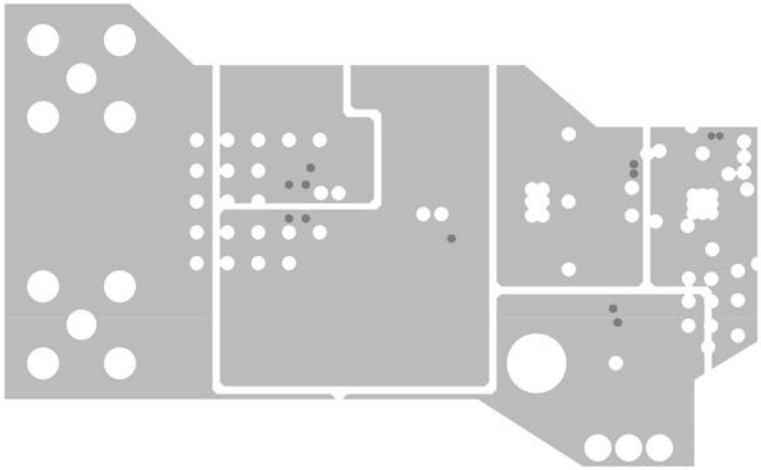


BOARD LAYOUT

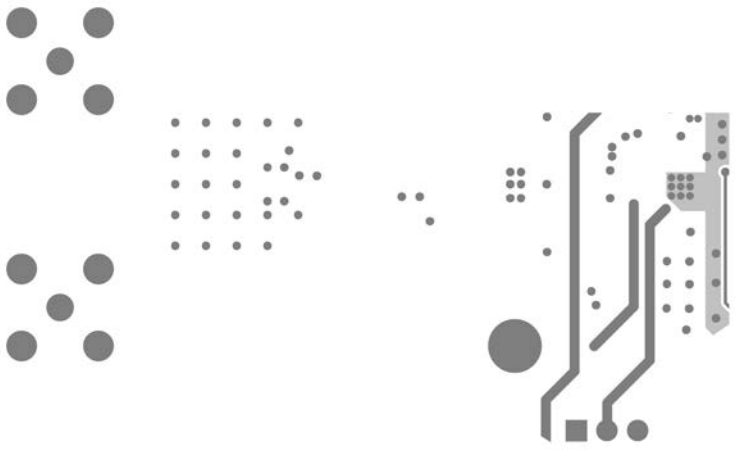
Partial Layer 2 Ground Plane



Partial Layer 3 Power Plane

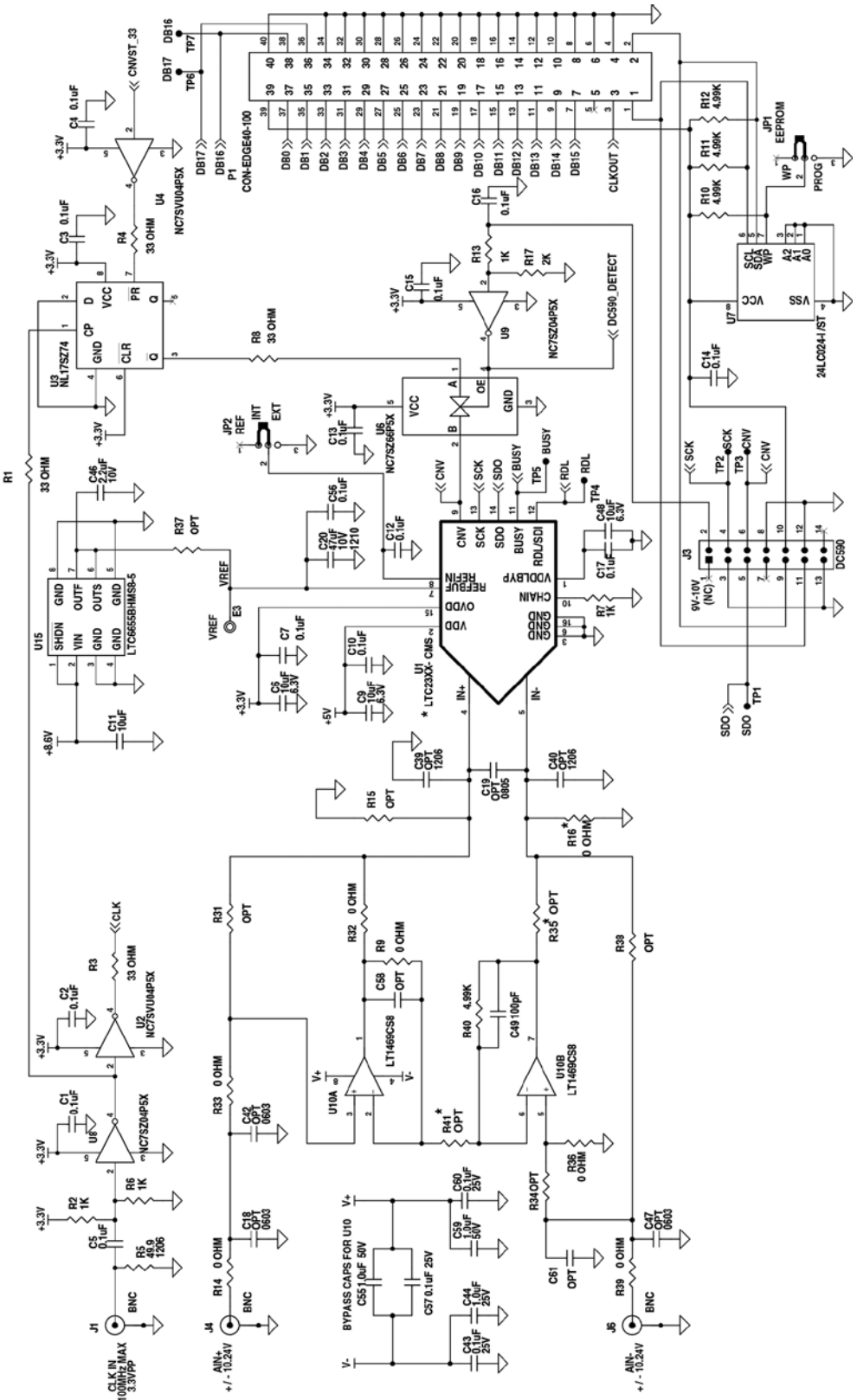


Partial Layer 4 Bottom Layer



BOARD LAYOUT

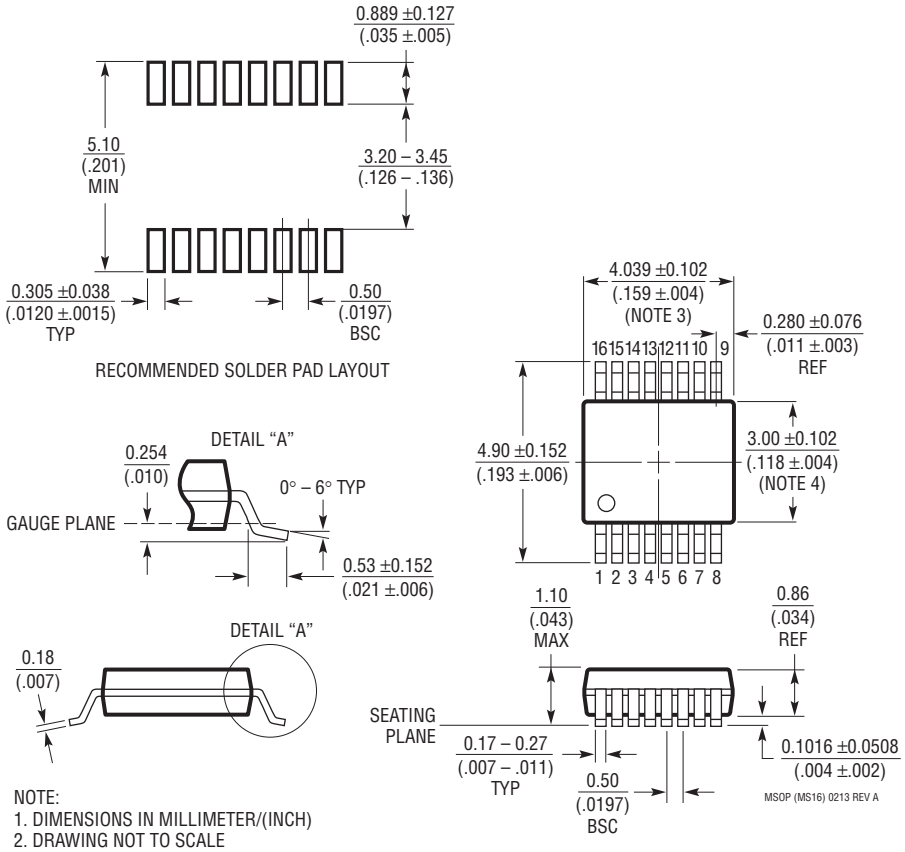
Partial Schematic of Demo Board



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2328-18#packaging for the most recent package drawings.

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev A)



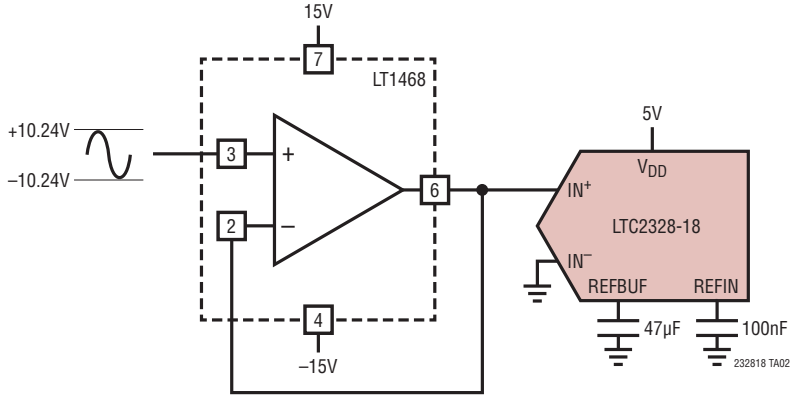
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/14	Updated minimum values for SINAD/SNR for ±6.25V range	3
		Updated Figure 9	16
B	08/16	Updated graphs G01, G02 and G03	7

TYPICAL APPLICATION

LT1468 Configured to Buffer a ±10.24V Single-Ended Signal Into the LTC2328-18



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2338-18/LTC2337-18/ LTC2336-18	18-Bit, 1Msps/500ksps/250ksps Serial, Low Power ADC	5V Supply, ±10.24V True Bipolar, Differential Input, 100dB SNR, Pin-Compatible Family in MSOP-16 Package
LTC2378-20/LTC2377-20/ LTC2376-20	20-Bit, 1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 0.5ppm INL, ±5V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4mm × 3 mm DFN-16 Packages
LTC2379-18/LTC2378-18/ LTC2377-18/LTC2376-18	18-Bit, 1.6Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 101.2dB SNR, ±5V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2380-16/LTC2378-16/ LTC2377-16/LTC2376-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 96.2dB SNR, ±5V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2369-18/LTC2368-18/ LTC2367-18/LTC2364-18	18-Bit, 1.6Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Pseudo-Differential Unipolar Input, 96.5dB SNR, 0V to 5V Input Range, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2370-16/LTC2368-16/ LTC2367-16/LTC2364-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Pseudo-Differential Unipolar Input, 94dB SNR, 0V to 5V Input Range, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2389-18/LTC2389-16	18-Bit/16-Bit, 2.5Msps Parallel/Serial ADC	5V Supply, Pin-Configurable Input Range, 99.8dB/96dB SNR, Parallel or Serial I/O 7mm × 7mm LQFP-48 and QFN-48 Packages
LTC1609	16-Bit, 200ksps Serial ADC	±10V, Configurable Unipolar/Bipolar Input, Single 5V Supply, SSOP-28 and SO-20 Packages
DACs		
LTC2756/LTC2757	18-Bit, Single Serial/Parallel I_{OUT} SoftSpan™ DAC	±1LSB INL/DNL, Software-Selectable Ranges, SSOP-28/7mm × 7mm LQFP-48 Package
LTC2641	16-Bit/14-Bit/12-Bit Single Serial V_{OUT} DAC	±1LSB INL /DNL, MSOP-8 Package, 0V to 5V Output
LTC2630	12-Bit/10-Bit/8-Bit Single V_{OUT} DACs	±1LSB INL (12 Bits), Internal Reference, SC70 6-Pin Package
References		
LTC6655	Precision Low Drift Low Noise Buffered Reference	5V/2.5V/2.048V/1.2V, 2ppm/°C, 0.25ppm Peak-to-Peak Noise, MSOP-8 Package
LTC6652	Precision Low Drift Low Noise Buffered Reference	5V/2.5V/2.048V/1.2V, 5ppm/°C, 2.1ppm Peak-to-Peak Noise, MSOP-8 Package
Amplifiers		
LT1468/LT1469	Single/Dual 90MHz, 22V/µs, 16-Bit Accurate Op Amp	Low Input Offset: 75µV/125µV

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