

# TPS1101, TPS1101Y SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS079C – DECEMBER 1993 – REVISED AUGUST 1995

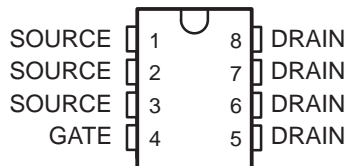
- Low  $r_{DS(on)}$  . . . 0.09  $\Omega$  Typ at  $V_{GS} = -10$  V
- 3 V Compatible
- Requires No External  $V_{CC}$
- TTL and CMOS Compatible Inputs
- $V_{GS(th)} = -1.5$  V Max
- Available in Ultrathin TSSOP Package (PW)
- ESD Protection Up to 2 kV per MIL-STD-883C, Method 3015

## description

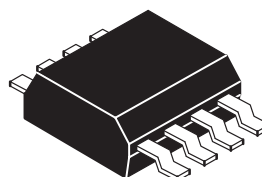
The TPS1101 is a single, low- $r_{DS(on)}$ , P-channel, enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of the Texas Instruments LinBiCMOS™ process. With a maximum  $V_{GS(th)}$  of  $-1.5$  V and an  $I_{DSS}$  of only 0.5  $\mu$ A, the TPS1101 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low  $r_{DS(on)}$  and excellent ac characteristics (rise time 5.5 ns typical) of the TPS1101 make it the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin thin shrink small-outline package or TSSOP (PW) version fits in height-restricted places where other P-channel MOSFETs cannot. The size advantage is especially important where board height restrictions do not allow for an small-outline integrated circuit (SOIC) package. Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other P-channel MOSFETs in SOIC packages.

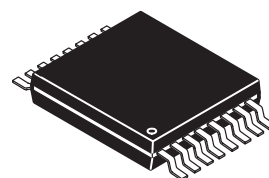
D PACKAGE  
(TOP VIEW)



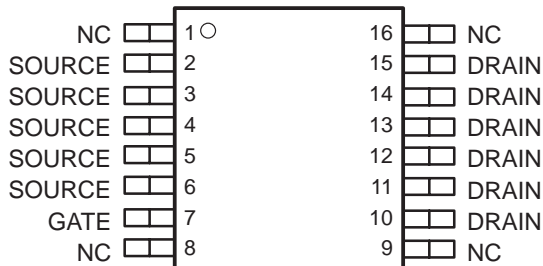
D PACKAGE



PW PACKAGE



PW PACKAGE  
(TOP VIEW)



NC – No internal connection

## AVAILABLE OPTIONS

$T_J$	PACKAGED DEVICES†		CHIP FORM (Y)
	SMALL OUTLINE (D)	TSSOP (PW)	
$-40^{\circ}\text{C}$ to $150^{\circ}\text{C}$	TPS1101D	TPS1101PWLE	TPS1101Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1101DR). The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1101PWLE). The chip form is tested at  $25^{\circ}\text{C}$ .



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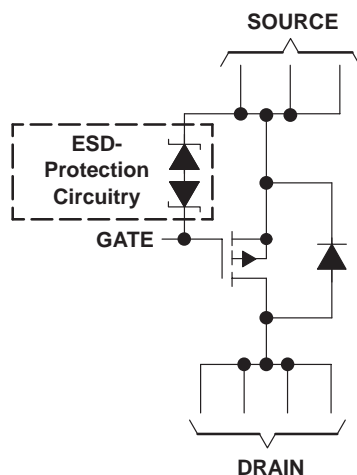
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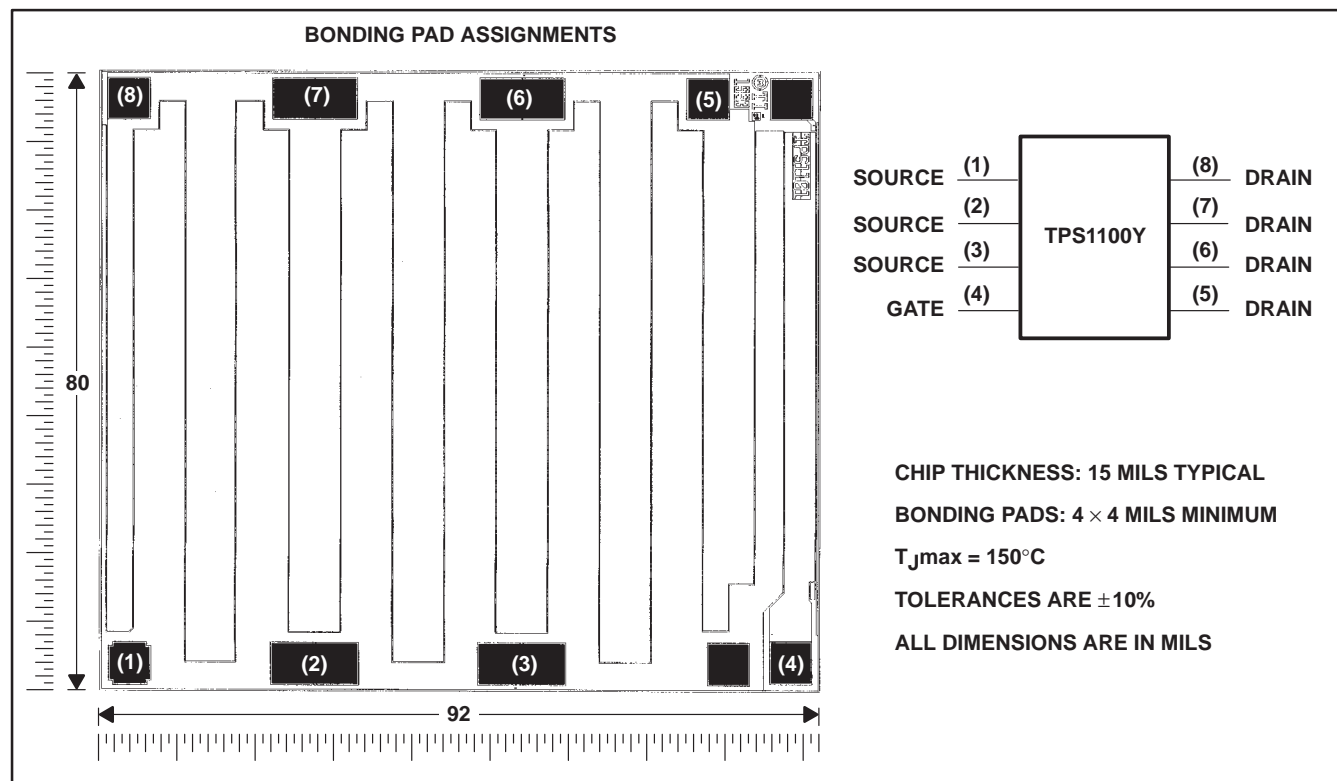
## schematic



NOTE A: For all applications, all source terminals should be connected and all drain terminals should be connected.

## TPS1101Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1101. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



# TPS1101, TPS1101Y

## SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

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**absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>**

					UNIT
Drain-to-source voltage, $V_{DS}$				– 15	V
Gate-to-source voltage, $V_{GS}$				2 or – 15	V
Continuous drain current ( $T_J = 150^{\circ}\text{C}$ ), $I_D^{\ddagger}$	$V_{GS} = -2.7\text{ V}$	D package	$T_A = 25^{\circ}\text{C}$	$\pm 0.62$	A
			$T_A = 125^{\circ}\text{C}$	$\pm 0.39$	
		PW package	$T_A = 25^{\circ}\text{C}$	$\pm 0.61$	
			$T_A = 125^{\circ}\text{C}$	$\pm 0.38$	
	$V_{GS} = -3\text{ V}$	D package	$T_A = 25^{\circ}\text{C}$	$\pm 0.88$	
			$T_A = 125^{\circ}\text{C}$	$\pm 0.47$	
		PW package	$T_A = 25^{\circ}\text{C}$	$\pm 0.86$	
			$T_A = 125^{\circ}\text{C}$	$\pm 0.45$	
	$V_{GS} = -4.5\text{ V}$	D package	$T_A = 25^{\circ}\text{C}$	$\pm 1.52$	
			$T_A = 125^{\circ}\text{C}$	$\pm 0.71$	
		PW package	$T_A = 25^{\circ}\text{C}$	$\pm 1.44$	
			$T_A = 125^{\circ}\text{C}$	$\pm 0.67$	
	$V_{GS} = -10\text{ V}$	D package	$T_A = 25^{\circ}\text{C}$	$\pm 2.30$	
			$T_A = 125^{\circ}\text{C}$	$\pm 1.04$	
		PW package	$T_A = 25^{\circ}\text{C}$	$\pm 2.18$	
			$T_A = 125^{\circ}\text{C}$	$\pm 0.98$	
Pulsed drain current, $I_D^{\ddagger}$			$T_A = 25^{\circ}\text{C}$	$\pm 10$	A
Continuous source current (diode conduction), $I_S$			$T_A = 25^{\circ}\text{C}$	– 1.1	A
Storage temperature range, $T_{Stg}$				–55 to 150	$^{\circ}\text{C}$
Operating junction temperature range, $T_J$				–40 to 150	$^{\circ}\text{C}$
Operating free-air temperature range, $T_A$				–40 to 125	$^{\circ}\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	$^{\circ}\text{C}$

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>‡</sup> Maximum values are calculated using a derating factor based on  $R_{\theta JA} = 158^\circ\text{C/W}$  for the D package and  $R_{\theta JA} = 176^\circ\text{C/W}$  for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR <sup>‡</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	791 mW	6.33 mW/ $^\circ\text{C}$	506 mW	411 mW	158 mW
PW	710 mW	5.68 mW/ $^\circ\text{C}$	454 mW	369 mW	142 mW

<sup>‡</sup> Maximum values are calculated using a derating factor based on  $R_{\theta JA} = 158^\circ\text{C/W}$  for the D package and  $R_{\theta JA} = 176^\circ\text{C/W}$  for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

# TPS1101, TPS1101Y

## SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

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### electrical characteristics at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

#### static

PARAMETER		TEST CONDITIONS		TPS1101			TPS1101Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = −250 μA		−1	−1.25	−1.5	−1.25			V
V <sub>SD</sub>	Source-to-drain voltage (diode-forward voltage) <sup>†</sup>	I <sub>S</sub> = −1 A, V <sub>GS</sub> = 0 V		−1.04			−1.04			V
I <sub>GSS</sub>	Reverse gate current, drain short circuited to source	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = −12 V		±100						nA
I <sub>DSS</sub>	Zero-gate-voltage drain current	V <sub>DS</sub> = −12 V, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C	−0.5						μA
			T <sub>J</sub> = 125°C	−10						
r <sub>DS(on)</sub>	Static drain-to-source on-state resistance <sup>†</sup>	V <sub>GS</sub> = −10 V	I <sub>D</sub> = −2.5 A	90			90			mΩ
		V <sub>GS</sub> = −4.5 V	I <sub>D</sub> = −1.5 A	134 190			134			
		V <sub>GS</sub> = −3 V	I <sub>D</sub> = −0.5 A	198 310			198			
		V <sub>GS</sub> = −2.7 V		232 400			232			
g <sub>fs</sub>	Forward transconductance <sup>†</sup>	V <sub>DS</sub> = −10 V, I <sub>D</sub> = −2 A		4.3			4.3			S

<sup>†</sup> Pulse test: pulse duration  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$

#### dynamic

PARAMETER	TEST CONDITIONS	TPS1101, TPS1101Y			UNIT
		MIN	TYP	MAX	
$Q_g$ Total gate charge	$V_{DS} = -10\ \text{V}$ , $V_{GS} = -10\ \text{V}$ , $I_D = -1\ \text{A}$		11.25		nC
$Q_{gs}$ Gate-to-source charge			1.5		
$Q_{gd}$ Gate-to-drain charge			2.6		
$t_{d(on)}$ Turn-on delay time	$V_{DD} = -10\ \text{V}$ , $R_L = 10\ \Omega$ , $I_D = -1\ \text{A}$ , $R_G = 6\ \Omega$ , See Figures 1 and 2		6.5		ns
$t_{d(off)}$ Turn-off delay time			19		ns
$t_r$ Rise time			5.5		ns
$t_f$ Fall time			13		
$t_{rr(SD)}$ Source-to-drain reverse recovery time	$I_F = 5.3\ \text{A}$ , $di/dt = 100\ \text{A}/\mu\text{s}$		16		

PARAMETER MEASUREMENT INFORMATION

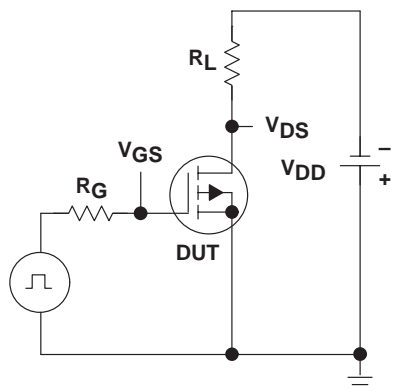


Figure 1. Switching-Time Test Circuit

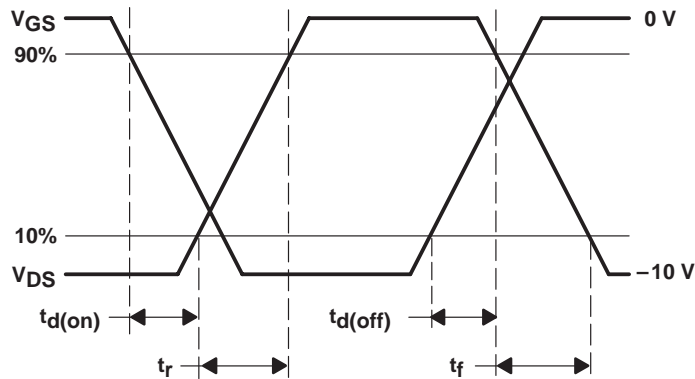


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

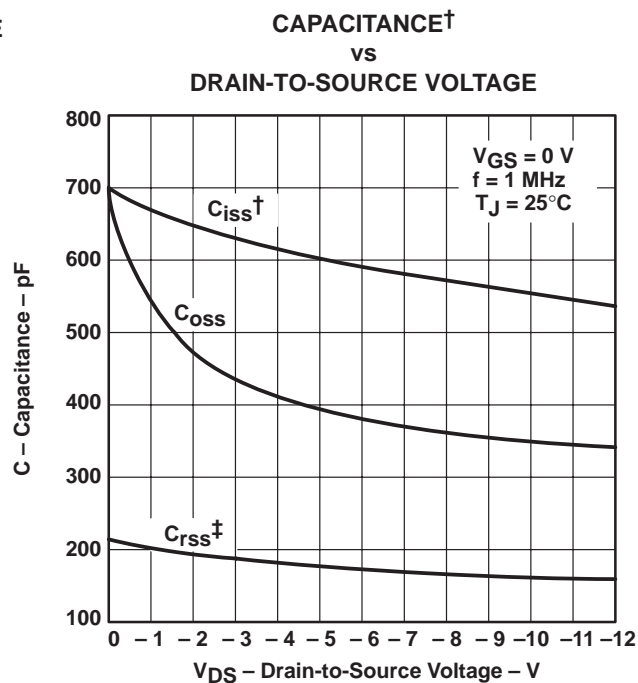
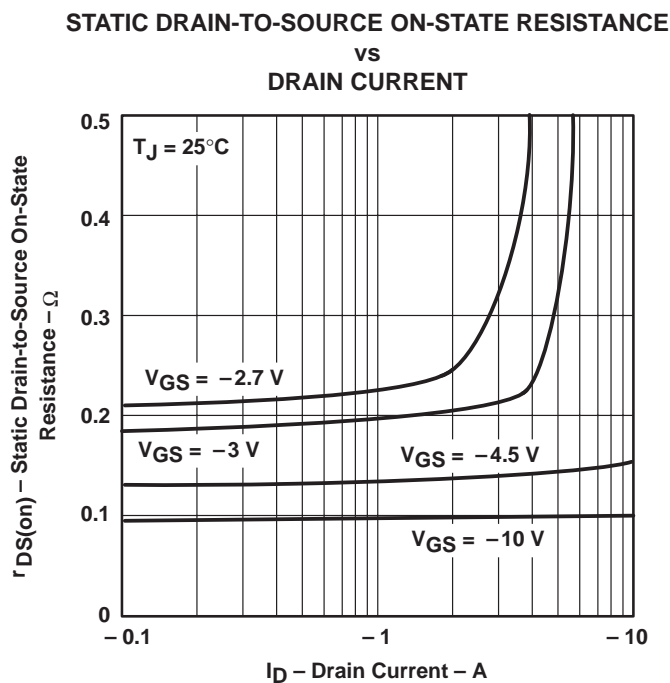
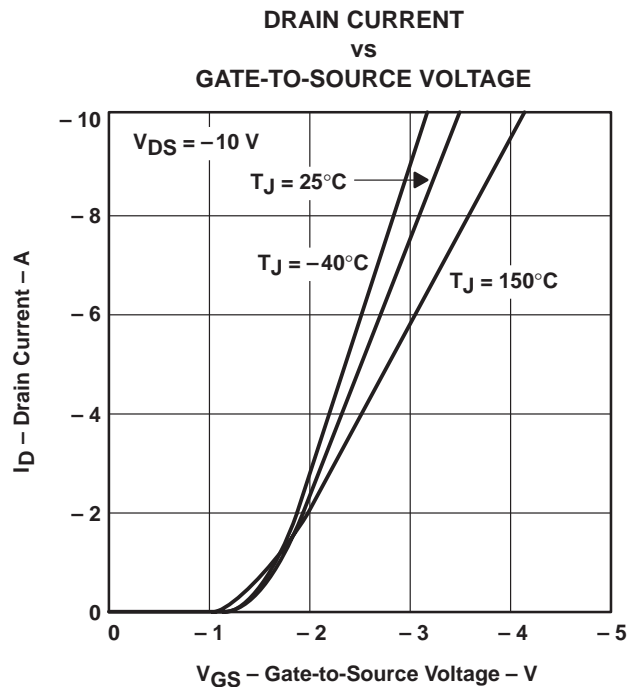
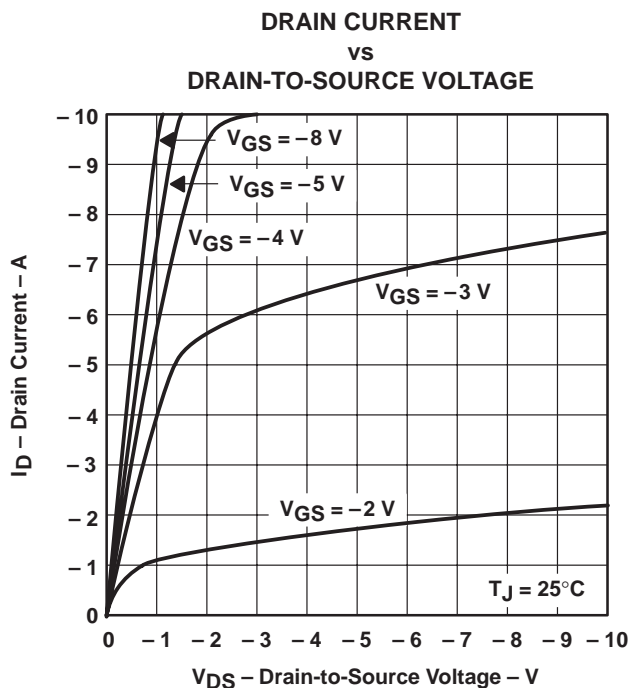
Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

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## TYPICAL CHARACTERISTICS



$$† C_{iss} = C_{gs} + C_{gd}, C_{ds(short)}$$

$$‡ C_{rss} = C_{gd}, C_{oss} = C_{ds} + \frac{C_{gs} C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$$

**Figure 6**

TYPICAL CHARACTERISTICS

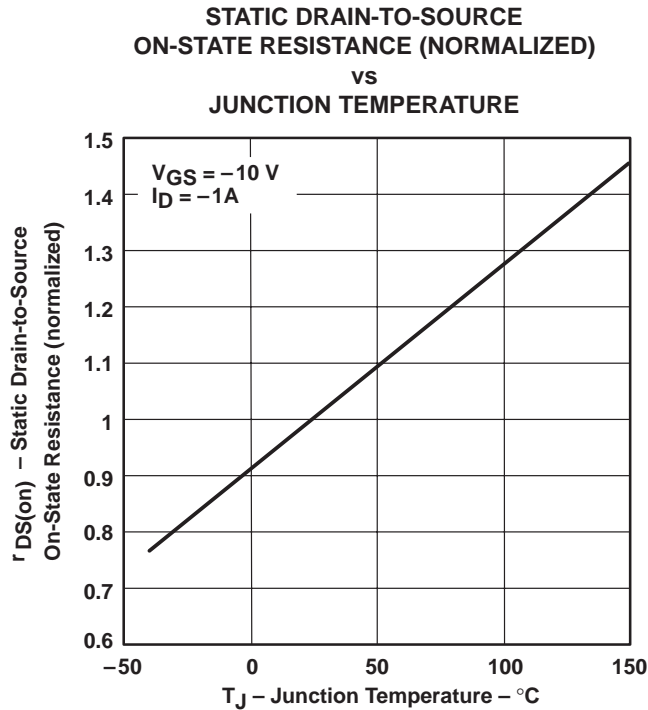


Figure 7

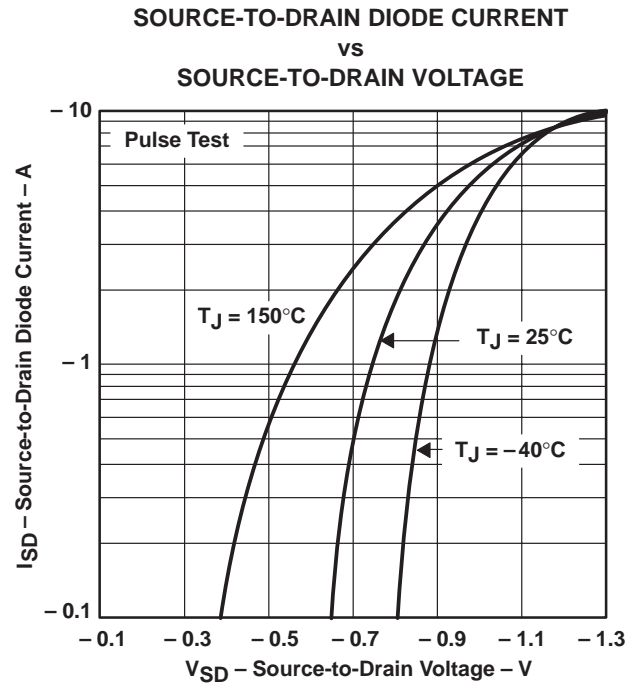


Figure 8

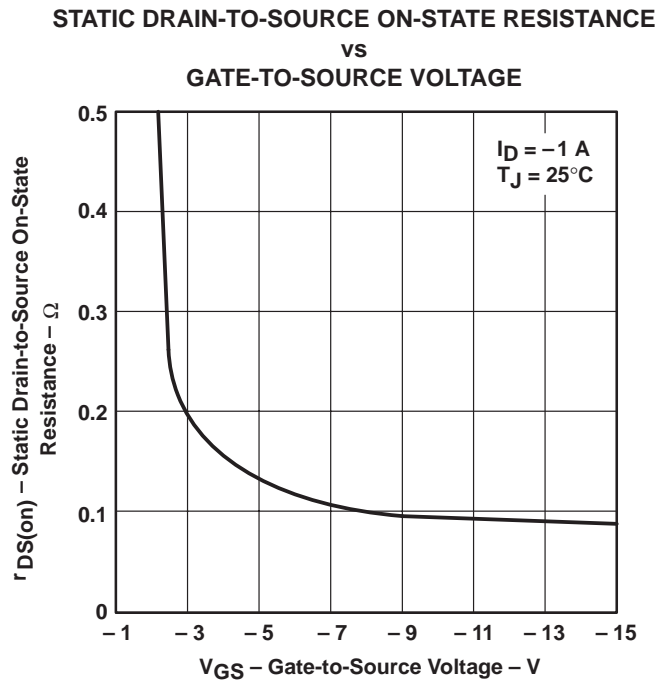


Figure 9

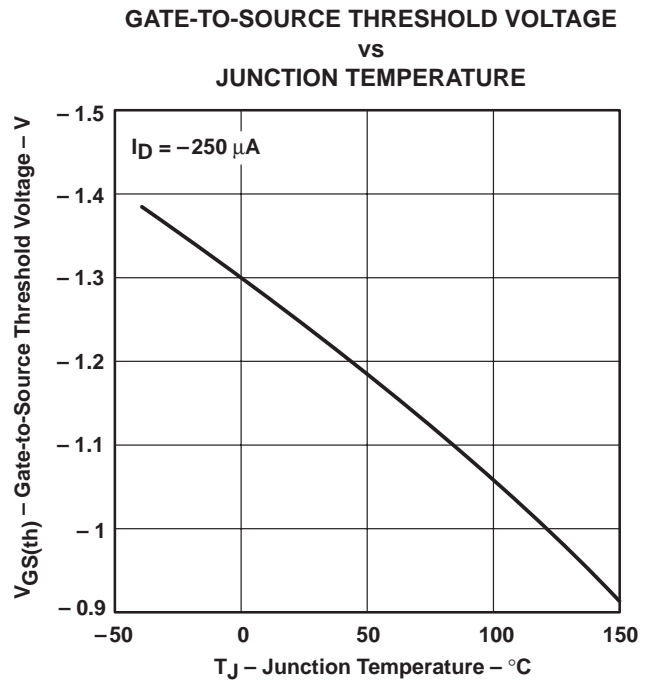


Figure 10

TPS1101, TPS1101Y  
SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

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TYPICAL CHARACTERISTICS

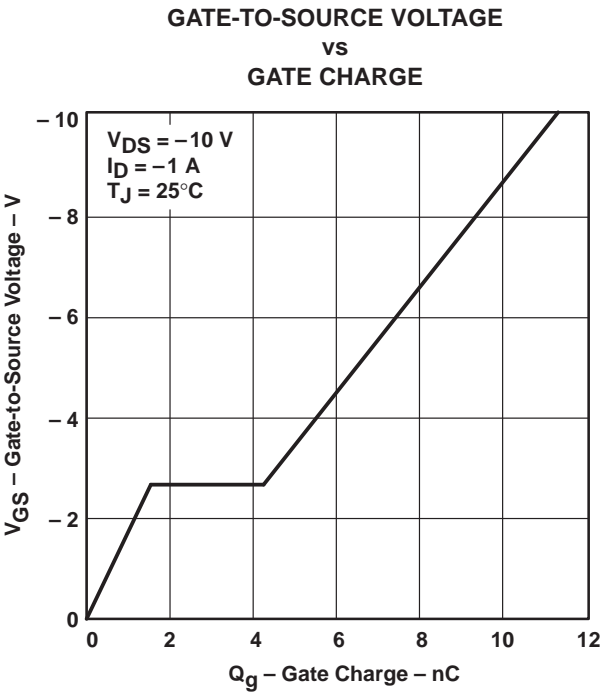
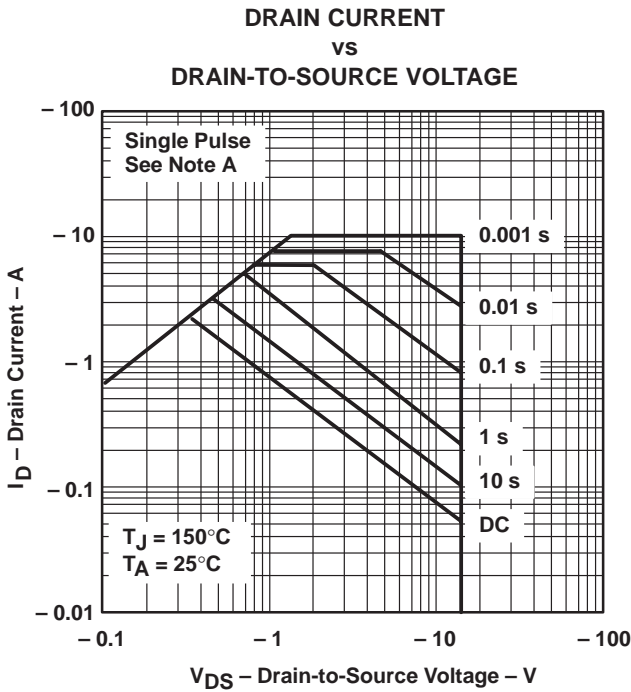


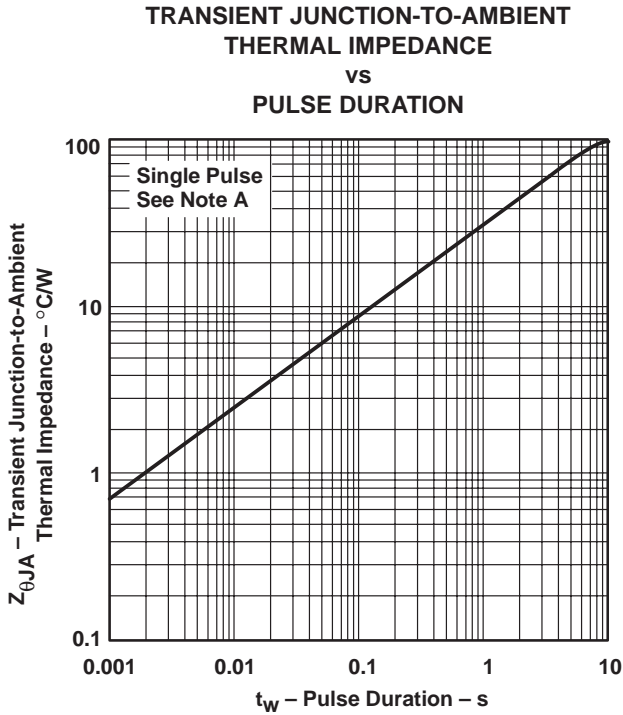
Figure 11



# THERMAL INFORMATION



NOTE A: Values are for the D package and are FR4-board-mounted only.



NOTE A: Values are for the D package and are FR4-board-mounted only.

# APPLICATION INFORMATION

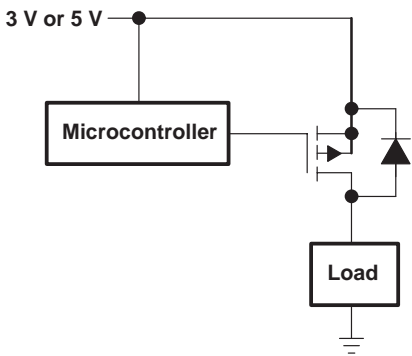


Figure 14. Notebook Load Management

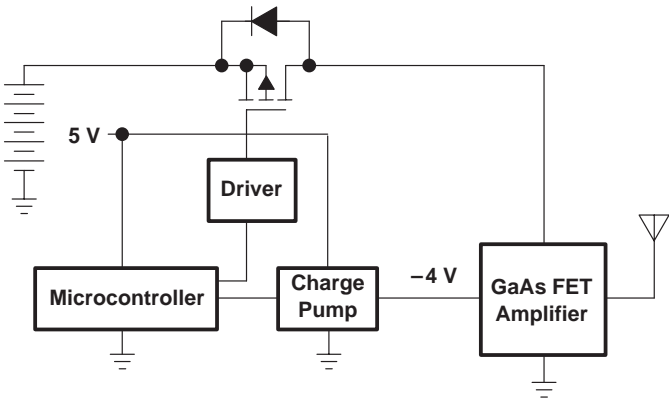


Figure 15. Cellular Phone Output Drive

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS1101D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1101	<a href="#">Samples</a>
TPS1101DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1101	<a href="#">Samples</a>
TPS1101DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1101	<a href="#">Samples</a>
TPS1101DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1101	<a href="#">Samples</a>
TPS1101PWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI			
TPS1101PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PS1101	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1101DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS1101PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1101DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS1101PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

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Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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