Siliconix incorporated

DG506A/507A
16-Channel and Dual 8-Channel CMOS Analog Multiplexers

FEATURES

- TTL & CMOS Direct Control Over Military Temperature Range
- Low Power (30 mW typ.)
- Break-Before-Make Switching
- ESD Protection > ±2500 V
- 44 V Power Supply Rating

BENEFITS

- Easily Interfaced
- Reduced Power Consumption
- Reduced System Crosstalk
- Environmentally Rugged

APPLICATIONS

- Communication Systems
- Multiplexing Reference Signals
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing

DESCRIPTION

DG506A/507A are 16- and dual 8-channel analog multiplexers, respectively, designed for selecting 1 of 16 (or 8) analog input signals and connecting it to a common output or, conversely, routing an analog signal to 1 of 16 (or 8) output loads. Break-before-make switching action protects against momentary shorting of the input signals.

The DG506A, a 16-channel single-ended analog multiplexer, is designed to connect 1 of 16 inputs to a common output as determined by a 4-bit binary address (A_0, A_1, A_2, A_3). DG507A, a dual 8-channel analog multiplexer, is designed to connect 1 of 8 dual inputs to a common dual output as determined by its 3 bit binary address (A_0, A_1, A_2) logic.

A channel in the ON state conducts current equally well in both directions (bi-directional switches). In the OFF state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches OFF. All control inputs, address (A_X) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

DG506A/507A are designed in the Siliconix PLUS-40 process, which includes improved ESD protection up to 2500 V for ruggedness. An epitaxial layer prevents latch up.

Both DG506A and DG507A are available in dual-in-line ceramic and plastic packages, and are specified for operation over the military, A suffix (–55 to 125°C), industrial, D suffix (–40 to 85°C), and commercial, C suffix (0 to 70°C), temperature ranges.

For applications requiring address data latching, the DG528/DG529 is recommended. For wideband/video routing and multiplexing applications, the DG536 is recommended.

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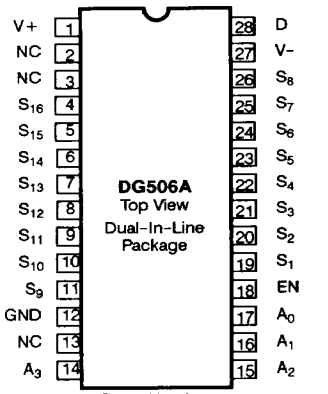
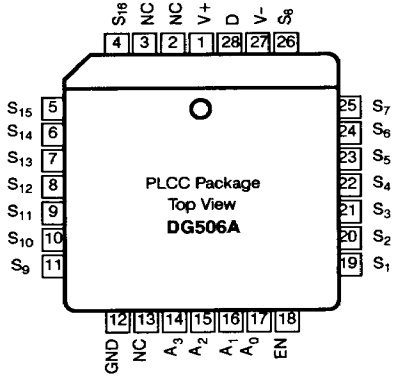
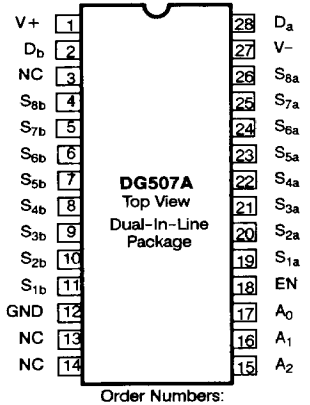
PIN CONFIGURATION



Order Numbers:
Side Braze: DG506ABR, DG506AAK/883
CerDIP: DG506AAK, DG506AAK/883
DG506ABK, DG506ACK
Plastic: DG506ACJ

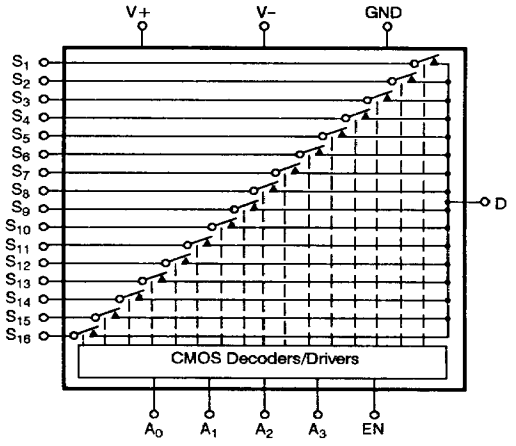


Order Number:
DG506ADN

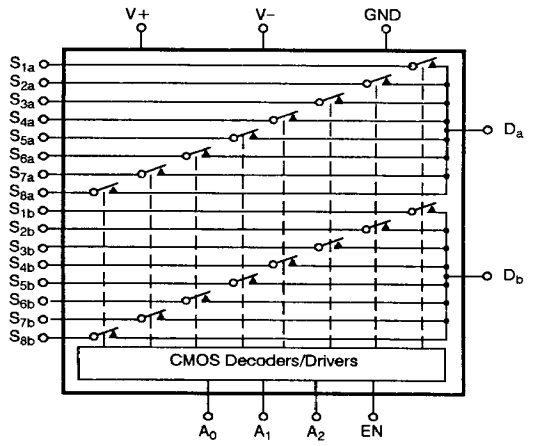


Order Numbers:
Side Braze: DG507ABR, DG507AAK/883
CerDIP: DG507AAK, DG507AAK/883
DG507ABK, DG507ACK
Plastic: DG507ACJ

FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLES



DG506A
16-Channel Single Ended Multiplexer



DG507A
Differential 8-Channel Multiplexer

A_3	A_2	A_1	A_0	EN	ON Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

A_2	A_1	A_0	EN	ON Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} \leq 0.8$ V, Logic "1" = $V_{AH} \geq 2.4$ V

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[h], V_S, V_D ..... (V-) -2 V to (V+) +2 V or
..... 20 mA, whichever occurs first
Current (Any Terminal, Except S or D) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak CURRENT, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA
Storage Temperature (A & B Suffix) ..... -65 to 150°C
(C Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C
(C Suffix) ..... 0 to 70°C

Power Dissipation (Package)*
28-Pin Ceramic DIP** ..... 1200 mW
28-Pin Plastic DIP*** ..... 625 mW

*All leads soldered or welded to PC board.
**Derate 16 mW/°C above 75°C.
***Derate 8.3 mW/°C above 75°C.

SPECIFICATIONS[a]

PARAMETER		SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V		TEMP[j]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B, C SUFFIX MIN[b]	B, C SUFFIX MAX[b]	UNIT
ANALOG SWITCH											
Analog Signal Range[c]		V_{ANALOG}			Full		-15	15	-15	15	V
Drain-Source ON-Resistance[e]		$r_{DS(ON)}$	$V_D = \pm 10$ V, $V_{AL} = 0.8$ V $I_S = -200$ µA, $V_{AH} = 2.4$ V		Room Full			400 500		450 550	Ω
$r_{DS(ON)}$ Matching[f]		$\Delta r_{DS(ON)}$	-10 V < V_S < 10 V		Room	6					%
Source OFF Leakage Current		$I_{S(OFF)}$	V_{EN} = 0 V	$V_S = \pm 10$ V $V_D = \mp 10$ V	Room Hot		-1 -50	1 50	-5 -50	5 50	µA
Drain OFF Leakage Current	DG506A	$I_{D(OFF)}$	V_{EN} = 0 V	$V_D = \pm 10$ V $V_S = \mp 10$ V	Room Hot		-10 -300	10 300	-20 -300	20 300	µA
	DG507A	$I_{D(OFF)}$	V_{EN} = 0 V	$V_D = \pm 10$ V $V_S = \mp 10$ V	Room Hot		-5 -200	5 200	-10 -200	10 200	µA
Drain ON[e, g] Leakage Current	DG506A	$I_{D(ON)}$	$V_S = V_D = \pm 10$ V $V_{AL} = 0.8$ V $V_{AH} = 2.4$ V		Room Hot		-10 -300	10 300	-20 -300	20 300	µA
	DG507A	$I_{D(ON)}$	$V_S = V_D = \pm 10$ V $V_{AL} = 0.8$ V $V_{AH} = 2.4$ V		Room Hot		-5 -200	5 200	-10 -200	10 200	µA
DIGITAL CONTROL											
Logic Input Current Input Voltage High		I_{AH}	V_A = 2.4 V		Room Hot		-10 -30		-10 -30		µA
		I_{AH}	V_A = 15 V		Room Hot			10 30		10 30	µA
Logic Input Current Input Voltage Low		I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Room Hot		-10 -30		-10 -30		µA
DYNAMIC CHARACTERISTICS											
Transition Time		t_{TRANS}	See Figure 1		Room	0.6		1			µs
Break-Before-Make Time		t_{OPEN}	See Figure 3		Room	0.2					ns
Enable Turn-ON Time		$t_{ON(EN)}$	See Figure 2		Room	1					µs
Enable Turn-OFF Time		$t_{OFF(ON)}$	See Figure 2		Room	0.4					µs
Charge Injection		Q			Room	20					pC
OFF Isolation[l]			V_{EN} = 0 V, R_L = 1 kΩ C_L = 15 pF, V_S = 7 V_{RMS} f = 500 kHz		Room	68					dB
Source OFF Capacitance		$C_{S(OFF)}$	V_{EN} = 0 V f = 140 kHz	V_S = 0 V	Room	6					pF
Drain OFF Capacitance	DG506A	$C_{D(OFF)}$	V_{EN} = 0 V f = 140 kHz	V_D = 0 V	Room	45					pF
	DG507A	$C_{D(OFF)}$	V_{EN} = 0 V f = 140 kHz	V_D = 0 V	Room	23					pF
POWER SUPPLIES											
Positive Supply Current		I+	V_{EN} = 0 V, V_A = 0 V		Room	1.3		2.4		2.4	mA
Negative Supply Current		I-	V_{EN} = 0 V, V_A = 0 V		Room	-0.7	-1.5		-1.5		mA

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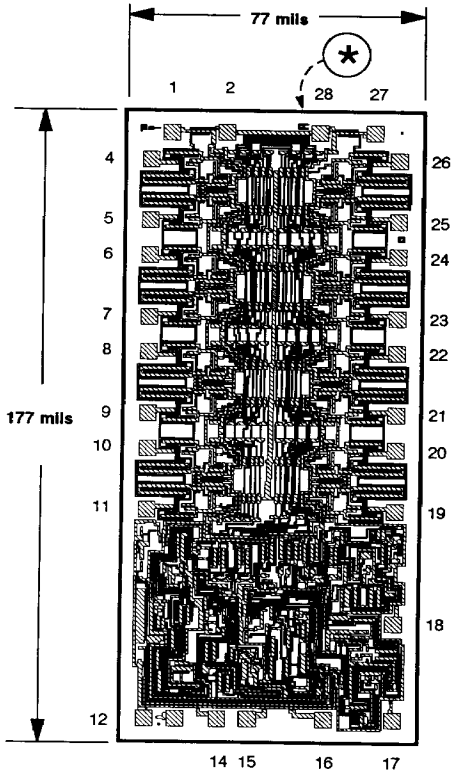
SPECIFICATIONS[a] (Cont'd)

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Sequence each switch ON.
f. $\Delta r_{DS(ON)} = \left(\frac{r_{DS(ON)}MAX - r_{DS(ON)}MIN}{r_{DS(ON)}AVE} \right)$
g. $I_{D(ON)}$ is leakage from driver into "ON" switch.
h. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
i. OFF isolation = 20 log $\frac{V_D}{V_S}$, V_S = input to "OFF" switch, V_D = output due to V_S.
j. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY



Pad No.	Function DG506A
1	V+ (Substrate)
2	NC
3	NC
4	S_{16}
5	S_{15}
6	S_{14}
7	S_{13}
8	S_{12}
9	S_{11}
10	S_{10}
11	S_9
12	GND
13	NC
14	A_3
15	A_2
16	A_1
17	A_0
18	EN
19	S_1
20	S_2
21	S_3
22	S_4
23	S_5
24	S_6
25	S_7
26	S_8
27	V-
28	D

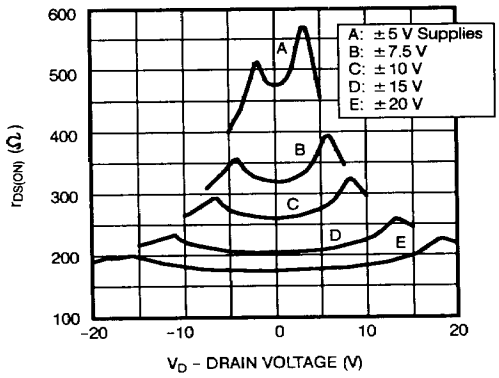
Pad No.	Function DG507A
1	V+ (Substrate)
2	D_b
3	NC
4	S_{8b}
5	S_{7b}
6	S_{6b}
7	S_{5b}
8	S_{4b}
9	S_{3b}
10	S_{2b}
11	S_{1b}
12	GND
13	NC
14	NC
15	A_2
16	A_1
17	A_0
18	EN
19	S_{1a}
20	S_{2a}
21	S_{3a}
22	S_{4a}
23	S_{5a}
24	S_{6a}
25	S_{7a}
26	S_{8a}
27	V-
28	D_a

ICMHA-I ***A = DG506A**
5 Capacitors
152 p-channel enhancement MOSFETs
8 Resistors
169 n-channel enhancement MOSFETs

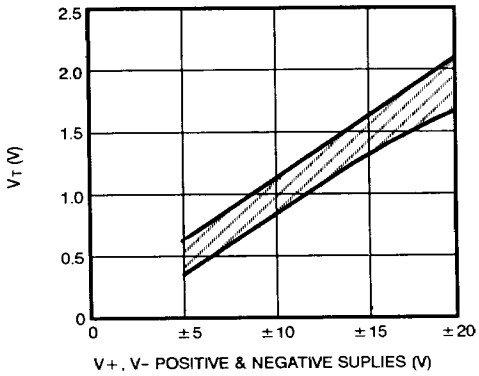
ICMHB-I ***B = DG507A**
4 Capacitors
141 p-channel enhancement MOSFETs
7 Resistors
160 n-channel enhancement MOSFETs

TYPICAL CHARACTERISTICS

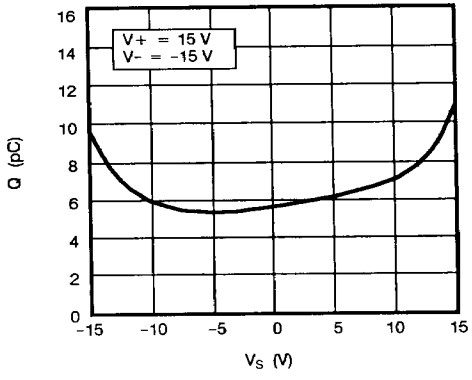
$r_{DS(ON)}$ vs. V_D and Power Supply



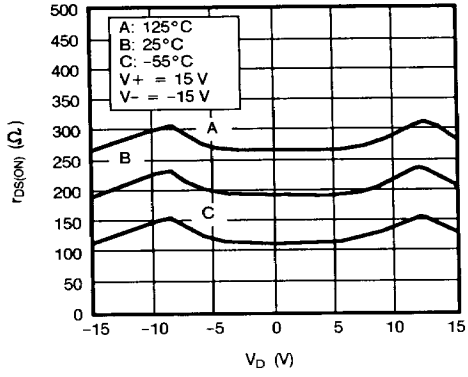
Input Switching Threshold vs. V+ and V- Supply Voltages



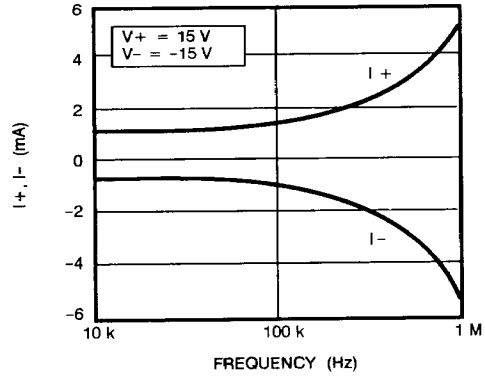
Charge Injection vs. Analog Voltage (V_S)



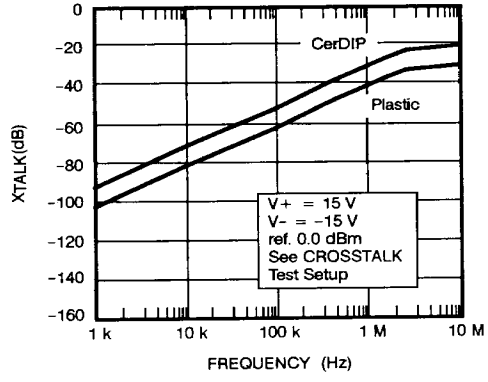
$r_{DS(ON)}$ vs. V_D and Temperature



Supply Current vs. Switching Frequency



Crosstalk vs. Frequency



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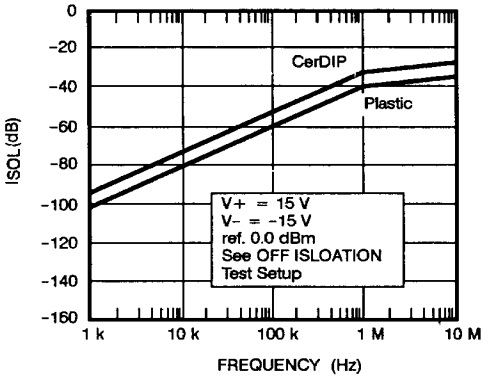
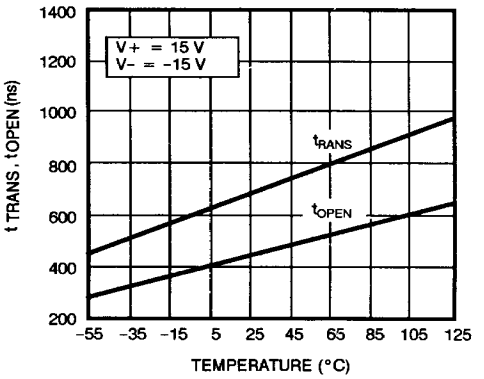
TYPICAL CHARACTERISTICS (Cont'd)

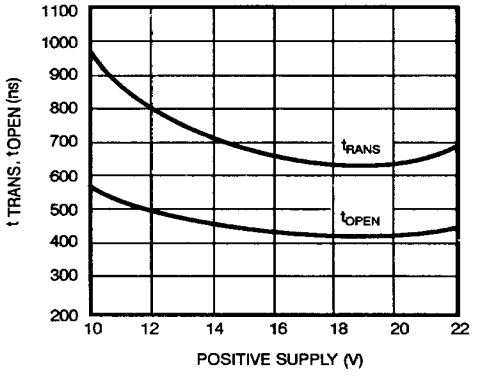
Off Isolation vs. Frequency



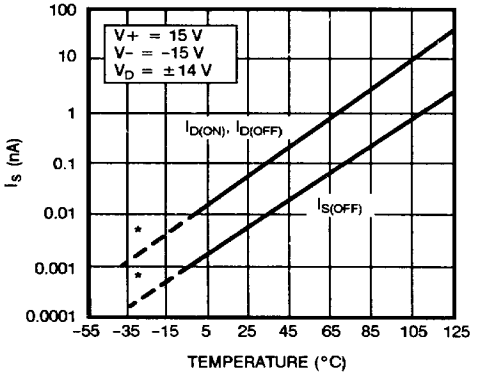
Switching Time vs. Temperature



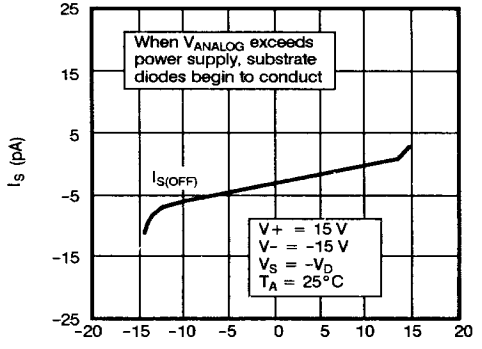
Switching Time vs. Positive Supply Voltage



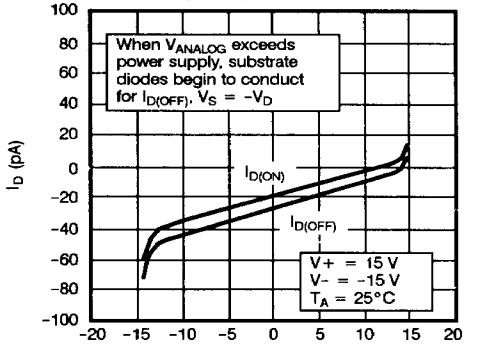
Leakages vs. Temperature



$I_{S(OFF)}$ vs. Analog Voltage



$I_{D(ON)}$, $I_{D(OFF)}$ vs. Analog Voltage



* Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

TEST CIRCUITS

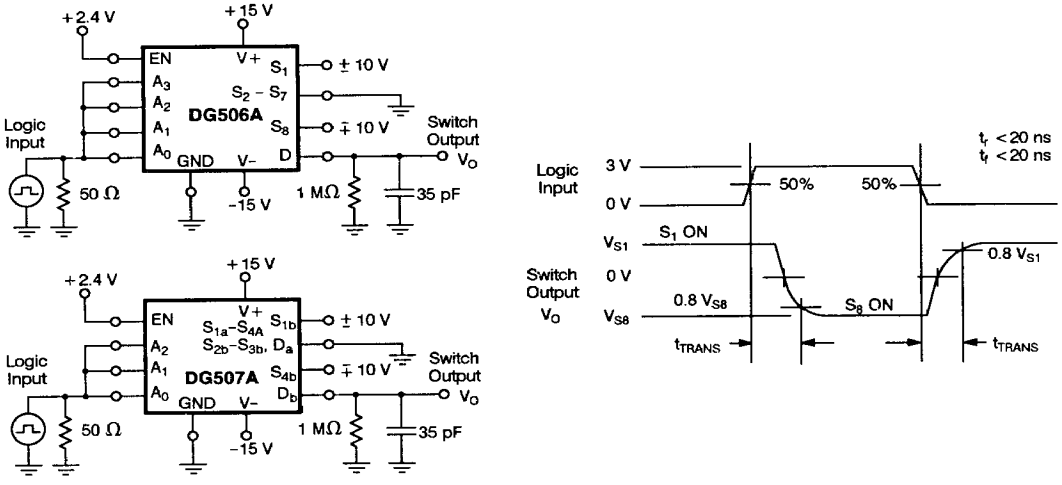


Figure 1. $t_{TRANSITION}$

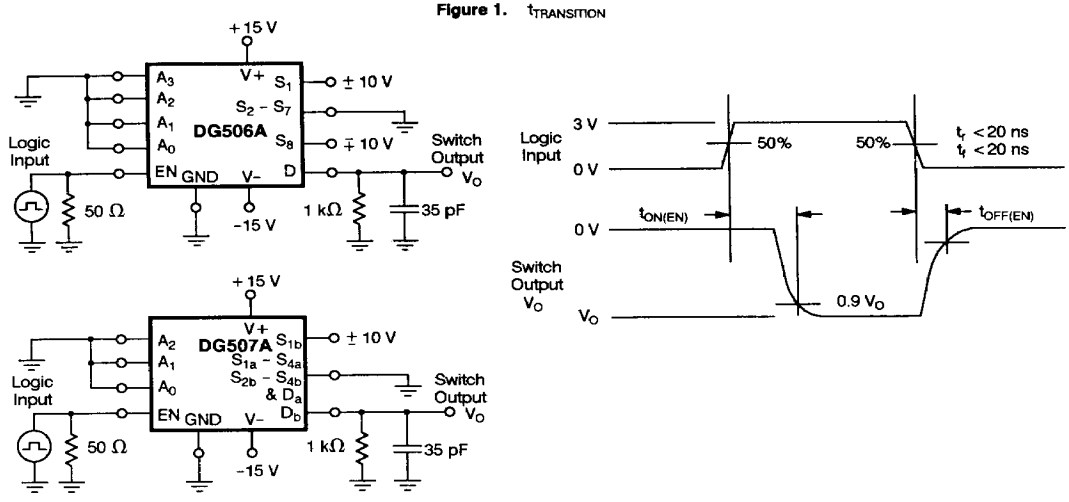


Figure 2. $t_{ON(EN)}$ and $t_{OFF(EN)}$

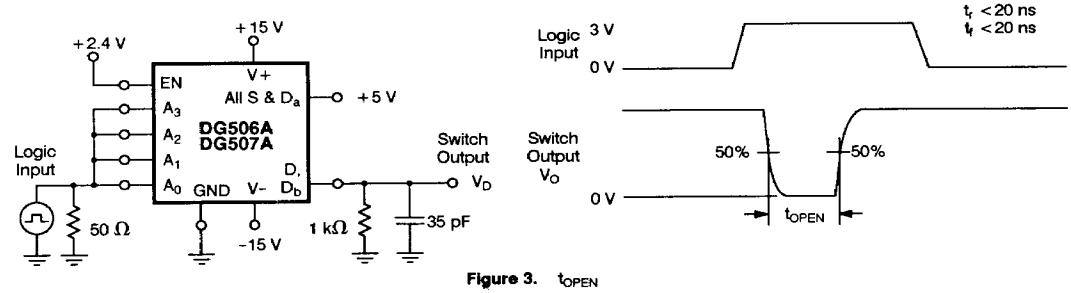


Figure 3. t_{OPEN}

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SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

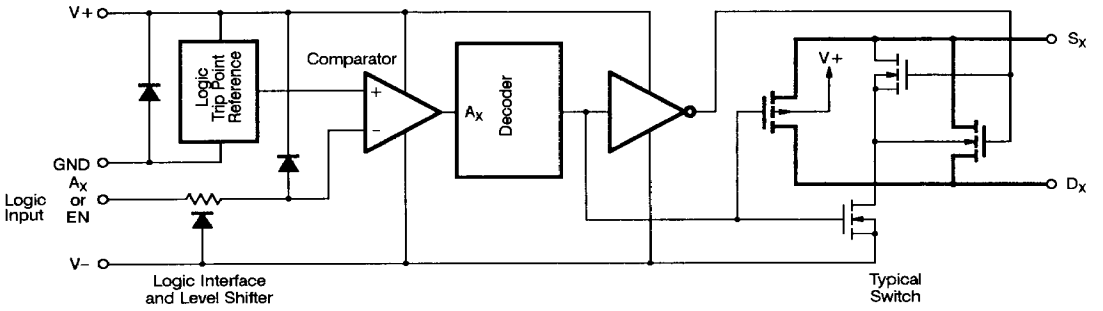

Figure 4.

APPLICATION HINTS*

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	Logic Input Voltage V_{INH} Min/V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
15**	−15	2.4/0.8	−15 to 15
12	−12	2.4/0.8	−12 to 12
10	−10	2.4/0.6	−10 to 10
8***	−8	2.4/0.4	−8 to 8

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
** Specifications chart based on V+ = +15 V, V− = −15 V.
*** Operation below ±8 V is not recommended due to the shift in $V_{INL(MAX)}$.

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 5). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V− value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference between V_S and the V− rail doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V−, but it preserves the low channel resistance and low leakage characteristics.

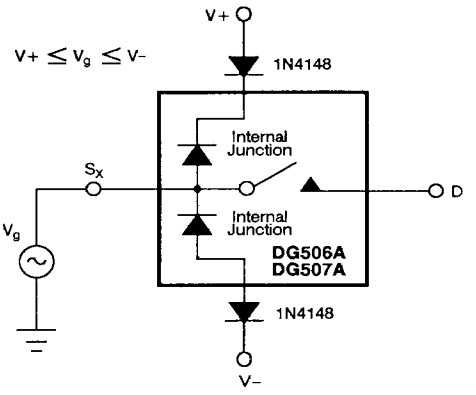

Figure 5. Overvoltage Protection Using Blocking Diodes

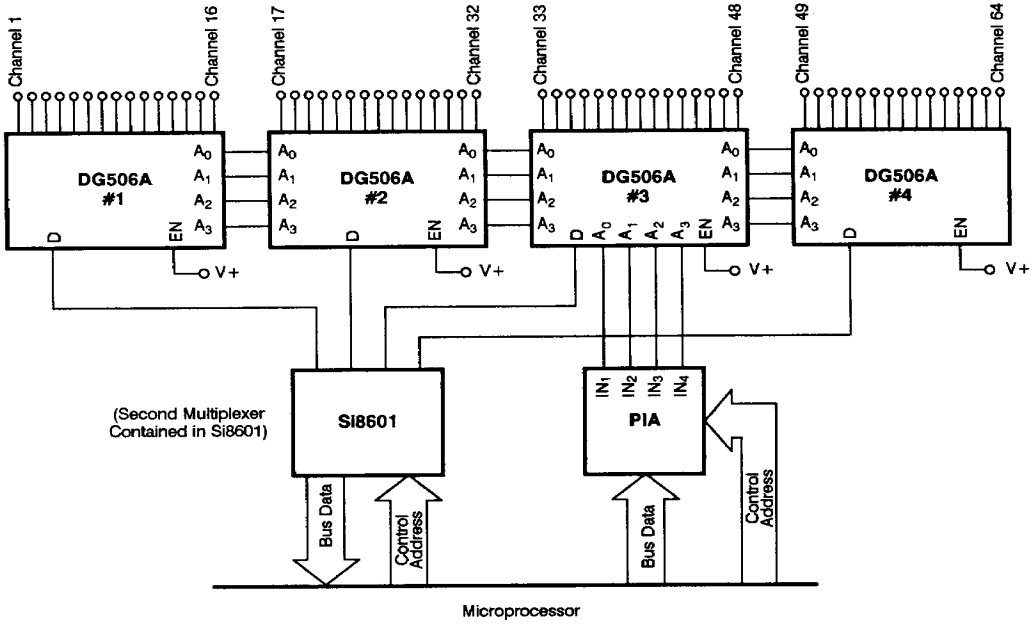

Figure 6. 64-Channel 2-Level Multiplex System

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