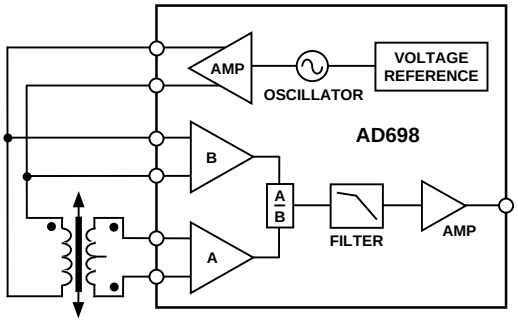
Universal LVDT Signal Conditioner

Data Sheet **AD698**

FEATURES

- **Single Chip Solution, Contains Internal Oscillator and Voltage Reference**
- **No Adjustments Required**
- **Interfaces to Half-Bridge, 4-Wire LVDT**
- **DC Output Proportional to Position**
- **20 Hz to 20 kHz Frequency Range**
- **Unipolar or Bipolar Output**
- **Will Also Decode AC Bridge Signals**
- **Outstanding Performance**
  - **Linearity: 0.05%**
  - **Output Voltage: ±11 V**
  - **Gain Drift: 20 ppm/°C (typ)**
  - **Offset Drift: 5 ppm/°C (typ)**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD698 is a complete, monolithic Linear Variable Differential Transformer (LVDT) signal conditioning subsystem. It is used in conjunction with LVDTs to convert transducer mechanical position to a unipolar or bipolar dc voltage with a high degree of accuracy and repeatability. All circuit functions are included on the chip. With the addition of a few external passive components to set frequency and gain, the AD698 converts the raw LVDT output to a scaled dc signal. The device will operate with half-bridge LVDTs, LVDTs connected in the series opposed configuration (4-wire), and RVDTs.

The AD698 contains a low distortion sine wave oscillator to drive the LVDT primary. Two synchronous demodulation channels of the AD698 are used to detect primary and secondary amplitude. The part divides the output of the secondary by the amplitude of the primary and multiplies by a scale factor. This eliminates scale factor errors due to drift in the amplitude of the primary drive, improving temperature performance and stability.

The AD698 uses a unique ratiometric architecture to eliminate several of the disadvantages associated with traditional approaches to LVDT interfacing. The benefits of this new circuit are: no adjustments are necessary; temperature stability is improved; and transducer interchangeability is improved.

The AD698 is available in two performance grades:

Grade	Temperature Range	Package
AD698AP	–40°C to +85°C	28-Pin PLCC
AD698SQ	–55°C to +125°C	24-Pin Cerdip

PRODUCT HIGHLIGHTS

1. The AD698 offers a single chip solution to LVDT signal conditioning problems. All active circuits are on the monolithic chip with only passive components required to complete the conversion from mechanical position to dc voltage.
2. The AD698 can be used with many different types of position sensors. The circuit is optimized for use with any LVDT, including half-bridge and series opposed, (4 wire) configurations. The AD698 accommodates a wide range of input and output voltages and frequencies.
3. The 20 Hz to 20 kHz excitation frequency is determined by a single external capacitor. The AD698 provides up to 24 volts rms to differentially drive the LVDT primary, and the AD698 meets its specifications with input levels as low as 100 millivolts rms.
4. Changes in oscillator amplitude with temperature will not affect overall circuit performance. The AD698 computes the ratio of the secondary voltage to the primary voltage to determine position and direction. No adjustments are required.
5. Multiple LVDTs can be driven by a single AD698 either in series or parallel as long as power dissipation limits are not exceeded. The excitation output is thermally protected.
6. The AD698 may be used as a loop integrator in the design of simple electromechanical servo loops.
7. The sum of the transducer secondary voltages do not need to be constant.

Rev. C Document Feedback

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AD698—SPECIFICATIONS (@ T_A = +25°C, V_{CM} = 0 V, and V+, V– = ±15 V dc, unless otherwise noted)

Parameter	AD698SQ Min	AD698SQ Typ	AD698SQ Max	AD698AP Min	AD698AP Typ	AD698AP Max	Unit
TRANSFER FUNCTION[1]	$V_{OUT} = \frac{A}{B} \times 500\ \mu A \times R2$						V
OVERALL ERROR T_{MIN} to T_{MAX}		0.4	**1.65**		0.4	**1.65**	% of FS
SIGNAL OUTPUT CHARACTERISTICS							
Output Voltage Range	**±11**			**±11**			V
Output Current, T_{MIN} to T_{MAX}		11			11		mA
Short Circuit Current		20			20		mA
Nonlinearity[2] T_{MIN} to T_{MAX}		75	**±500**		75	**±500**	ppm of FS
Gain Error[3]		0.1	**±1.0**		0.1	**±1.0**	% of FS
Gain Drift		20	**±100**		20	**±100**	ppm/°C of FS
Output Offset		0.02	**±1**		0.02	**±1**	% of FS
Offset Drift		5	**±25**		5	**±25**	ppm/°C of FS
Excitation Voltage Rejection[4]		100			100		ppm/dB
Power Supply Rejection (±12 V to ±18 V)							
PSRR Gain		50	**300**		50	**300**	ppm/V
PSRR Offset		15	**100**		15	**100**	ppm/V
Common-Mode Rejection (±3 V)							
CMRR Gain		25	**100**		25	**100**	ppm/V
CMRR Offset		2	**100**		2	**100**	ppm/V
Output Ripple[5]		4			4		mV rms
EXCITATION OUTPUT CHARACTERISTICS (@ 2.5 kHz)							
Excitation Voltage Range	2.1		24	2.1		24	V rms
Excitation Voltage (Resistors Are 1% Absolute Values)							
(R1 = Open)[6]	**1.2**		**2.15**	**1.2**		**2.15**	V rms
(R1 = 12.7 kΩ)	**2.6**		**4.35**	**2.6**		**4.35**	V rms
(R1 = 487 Ω)	**14**		**21.2**	**14**		**21.2**	V rms
Excitation Voltage TC[7]		100			100		ppm/°C
Output Current	**30**	50		**30**	50		mA rms
T_{MIN} to T_{MAX}		40			40		mA rms
Short Circuit Current		60			60		mA
DC Offset Voltage (Differential, R1 = 12.7 kΩ)							
T_{MIN} to T_{MAX}		30	**±100**		30	**±100**	mV
Frequency	20		20 k	20		20 k	Hz
Frequency TC		200			200		ppm/°C
Total Harmonic Distortion		–50			–50		dB
SIGNAL INPUT CHARACTERISTICS							
A/B Ratio Usable Full-Scale Range	0.1		0.9	0.l		0.9	
Signal Voltage B Channel	0.1		3.5	0.1		3.5	V rms
Signal Voltage A Channel	0.0		3.5	0.0		3.5	V rms
Input Impedance		200			200		kΩ
Input Bias Current (BIN, AIN)		1	5		1	5	μA
Signal Reference Bias Current		2	**10**		2	**10**	μA
Excitation Frequency	0		20 k	0		20 k	Hz
POWER SUPPLY REQUIREMENTS							
Operating Range	13		36	13		36	V
Dual Supply Operation (±10 V Output)	±13			±13			V
Single Supply Operation							
0 V to +10 V Output	17.5			17.5			V
0 V to 10 V Output	17.5			17.5			V
Current (No Load at Signal and Excitation Outputs)		12	**15**		12	**15**	mA
T_{MIN} to T_{MAX}			**18**			**18**	mA
OPERATING TEMPERATURE RANGE	–55		+125	–40		+85	°C

NOTES

[1]A and B represent the Mean Average Deviation (MAD) of the detected sine waves V_A and V_B. The polarity of V_{OUT} is affected by the sign of the A comparator, i.e., multiply $V_{OUT} \times +1$ for $A_{COMP+} > A_{COMP-}$, and $V_{OUT} \times -1$ for $A_{COMP-} > A_{COMP+}$.

[2]Nonlinearity of the AD698 only in units of ppm of full scale. Nonlinearity is defined as the maximum measured deviation of the AD698 output voltage from a straight line. The straight line is determined by connecting the maximum produced full-scale negative voltage with the maximum produced full-scale positive voltage.

[3]See Transfer Function.

[4]For example, if the excitation to the primary changes by 1 dB, the gain of the system will change by typically 100 ppm.

[5]Output ripple is a function of the AD698 bandwidth determined by C1 and C2. A 1000 pF capacitor should be connected in parallel with R2 to reduce the output ripple. See Figures 7, 8 and 13.

[6]R1 is shown in Figures 7, 8 and 13.

[7]Excitation voltage drift is not an important specification because of the ratiometric operation of the AD698.

[8]From T_{MIN} to T_{MAX} the overall error due to the AD698 alone is determined by combining gain error, gain drift and offset drift. For example, the typical overall error for the AD698AP from T_{MIN} to T_{MAX} is calculated as follows: Overall Error = Gain Error at +25°C (±0.2% Full Scale) + Gain Drift from –40°C to +25°C (20 ppm/°C × 65°C) + Offset Drift from –40°C to +25°C (5 ppm/°C × 65°C) = ±0.36% of full scale. Note that 1000 ppm of full scale equals 0.1% of full scale.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tested are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage ($+V_S$ to $-V_S$) . . . . . 36 V
Storage Temperature Range
  P Package . . . . . –65°C to +150°C
  Q Package . . . . . –65°C to +150°C
Operating Temperature Range
  AD698SQ . . . . . –55°C to +125°C
  AD698AP . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C
Power Dissipation Derates above +65°C
  P Package . . . . . 12 mW/°C
  Q Package . . . . . 12 mW/°C

THERMAL CHARACTERISTICS

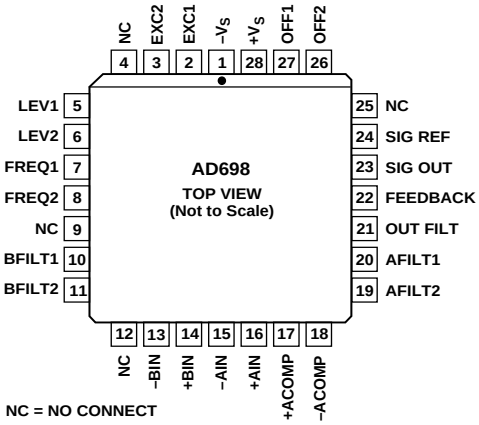
	θ_{JC}	θ_{JA}
P Package	30°C/W	60°C/W
Q Package	26°C/W	62°C/W

ESD CAUTION

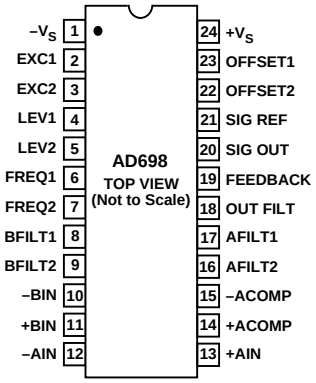
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

CONNECTION DIAGRAMS

28-Pin PLCC



24-Pin Cerdip



Typical Characteristics (at +25°C and V_S = ±15 V unless otherwise noted)

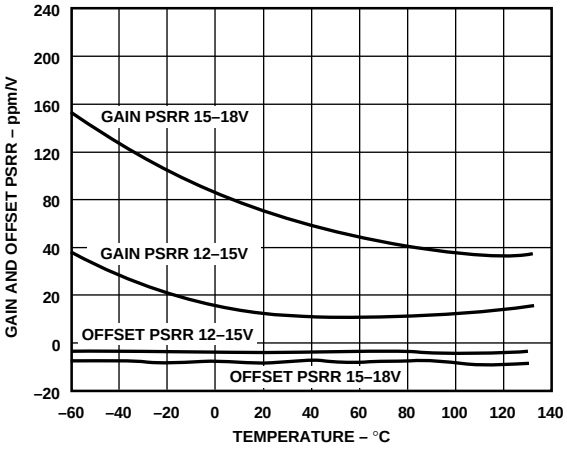


Figure 1. Gain and Offset PSRR vs. Temperature

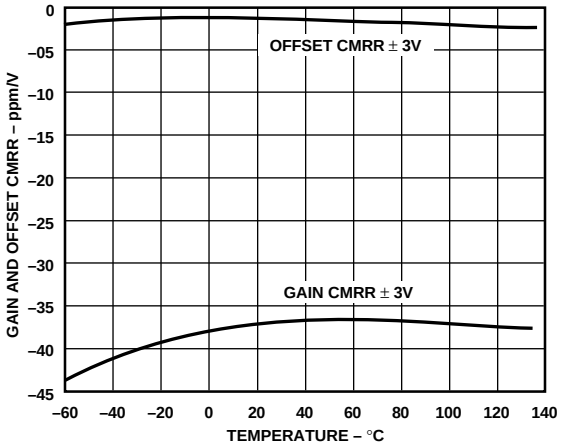


Figure 2. Gain and Offset CMRR vs. Temperature

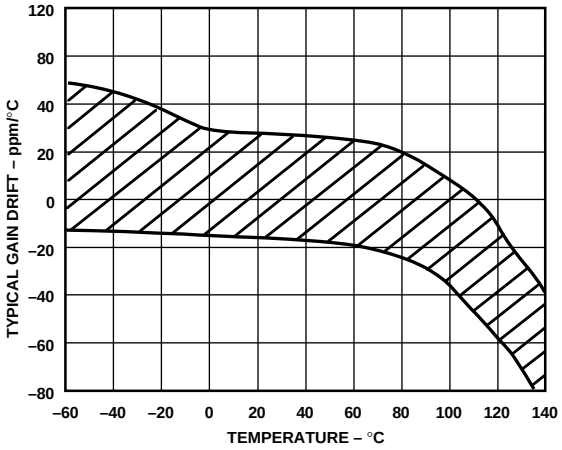


Figure 3. Typical Gain Drift vs. Temperature

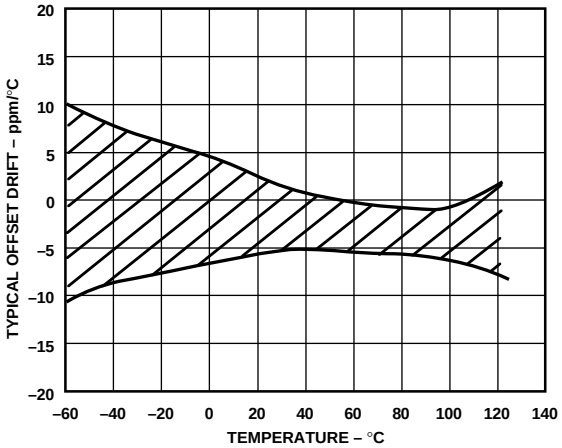


Figure 4. Typical Offset Drift vs. Temperature

THEORY OF OPERATION

A block diagram of the AD698 along with an LVDT (linear variable differential transformer) connected to its input is shown in Figure 5 below. The LVDT is an electromechanical transducer—its input is the mechanical displacement of a core, and its output is an ac voltage proportional to core position. Two popular types of LVDTs are the half-bridge type and the series opposed or four-wire LVDT. In both types the moveable core couples flux between the windings. The series-opposed connected LVDT transducer consists of a primary winding energized by an external sine wave reference source and two secondary windings connected in the series opposed configuration. The output voltage across the series secondary increases as the core is moved from the center. The direction of movement is detected by measuring the phase of the output. Half-bridge LVDTs have a single coil with a center tap and work like an autotransformer. The excitation voltage is applied across the coil; the voltage at the center tap is proportional to position. The device behaves similarly to a resistive voltage divider.

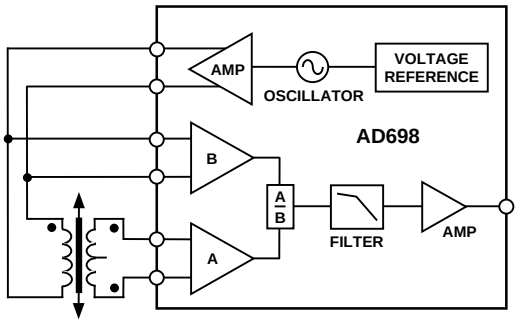


Figure 5. Functional Block Diagram

The AD698 energizes the LVDT coil, senses the LVDT output voltages and produces a dc output voltage proportional to core position. The AD698 has a sine wave oscillator and power amplifier to drive the LVDT. Two synchronous demodulation stages are available for decoding the primary and secondary voltages. A decoder determines the ratio of the output signal voltage to the input drive voltage (A/B). A filter stage and output amplifier are used to scale the resulting output.

The oscillator comprises a multivibrator that produces a triwave output. The triwave drives a sine shaper that produces a low distortion sine wave. Frequency and amplitude are determined by a single resistor and capacitor. Output frequency can range from 20 Hz to 20 kHz and amplitude from 2 V to 24 V rms. Total harmonic distortion is typically –50 dB.

The AD698 decodes LVDTs by synchronously demodulating the amplitude modulated input (secondaries), A, and a fixed input reference (primary or sum of secondaries or fixed input), B. A common problem with earlier solutions was that any drift in the amplitude of the drive oscillator corresponded directly to a gain error in the output. The AD698, eliminates these errors by calculating the ratio of the LVDT output to its input excitation in order to cancel out any drift effects. This device differs from the AD598 LVDT signal conditioner in that it implements a different circuit transfer function and does not require the sum of the LVDT secondaries (A + B) to be constant with stroke length.

The AD698 block diagram is shown below. The inputs consist of two independent synchronous demodulation channels. The B channel is designed to monitor the drive excitation to the LVDT. The full wave rectified output is filtered by C2 and sent to the computational circuit. Channel A is identical except that the comparator is pinned out separately. Since the A channel may reach 0 V output at LVDT null, the A channel demodulator is usually triggered by the primary voltage (B Channel). In addition, a phase compensation network may be required to add a phase lead or lag to the A Channel to compensate for the LVDT primary to secondary phase shift. For half-bridge circuits the phase shift is noncritical, and the A channel voltage is large enough to trigger the demodulator.

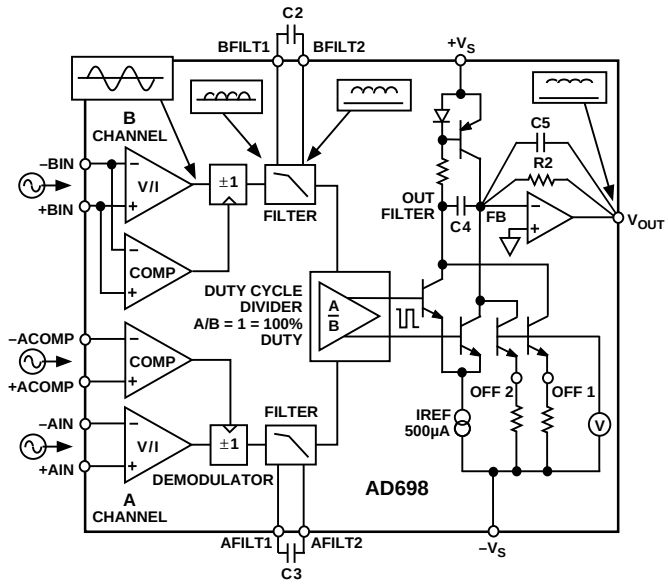


Figure 6. AD698 Block Diagram

Once both channels are demodulated and filtered a division circuit, implemented with a duty cycle multiplier, is used to calculate the ratio A/B. The output of the divider is a duty cycle. When A/B is equal to 1, the duty cycle will be equal to 100%. (This signal can be used as is if a pulse width modulated output is required.) The duty cycle drives a circuit that modulates and filters a reference current proportional to the duty cycle. The output amplifier scales the 500 µA reference current converting it to a voltage. The output transfer function is thus:

$$V_{OUT} = I_{REF} \times A/B \times R2, \text{ where } I_{REF} = 500\ \mu A$$

CONNECTING THE AD698

The AD698 can easily be connected for dual or single supply operation as shown in Figures 7, 8 and 13. The following general design procedures demonstrate how external component values are selected and can be used for any LVDT that meets AD698 input/output criteria. The connections for the A and B channels and the A channel comparators will depend on which transducer is used. In general follow the guidelines below.

Parameters set with external passive components include: excitation frequency and amplitude, AD698 input signal frequency, and the scale factor (V/inch). Additionally, there are optional features; offset null adjustment, filtering, and signal integration, which can be implemented by adding external components.

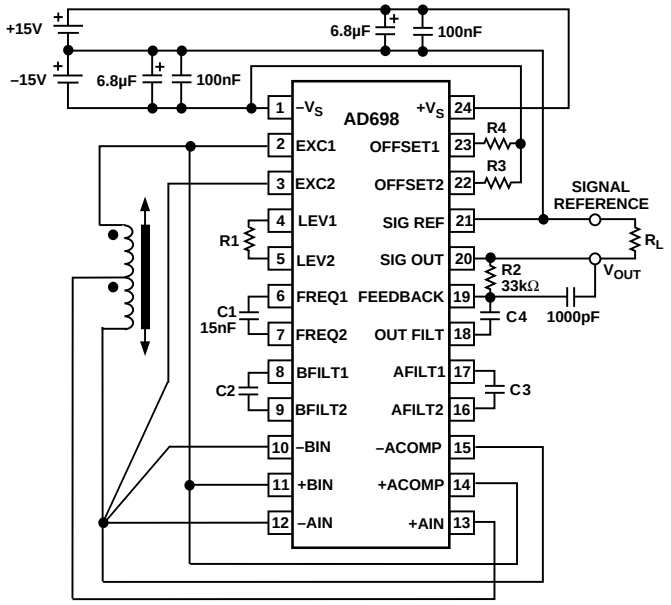


Figure 7. Interconnection Diagram for Half-Bridge LVDT and Dual Supply Operation

DESIGN PROCEDURE

DUAL SUPPLY OPERATION

Figure 7 shows the connection method for half-bridge LVDTs. Figure 8 demonstrates the connections for 3- and 4-wire LVDTs connected in the series opposed configuration. Both examples use dual ±15 volt power supplies.

A. Determine the Oscillator Frequency

Frequency is often determined by the required BW of the system. However, in some systems the frequency is set to match the LVDT zero phase frequency as recommended by the manufacturer; in this case skip to Step 4.

1. Determine the mechanical bandwidth required for LVDT position measurement subsystem, $f_{SUBSYSTEM}$. For this example, assume $f_{SUBSYSTEM}$ = 250 Hz.
2. Select minimum LVDT excitation frequency approximately $10 \times f_{SUBSYSTEM}$. Therefore, let excitation frequency = 2.5 kHz.
3. Select a suitable LVDT that will operate with an excitation frequency of 2.5 kHz. The Schaevitz E100, for instance, will operate over a range of 50 Hz to 10 kHz and is an eligible candidate for this example.
4. Select excitation frequency determining component C1.

$$C1 = 35\ \mu F\ Hz/f_{EXCITATION}$$

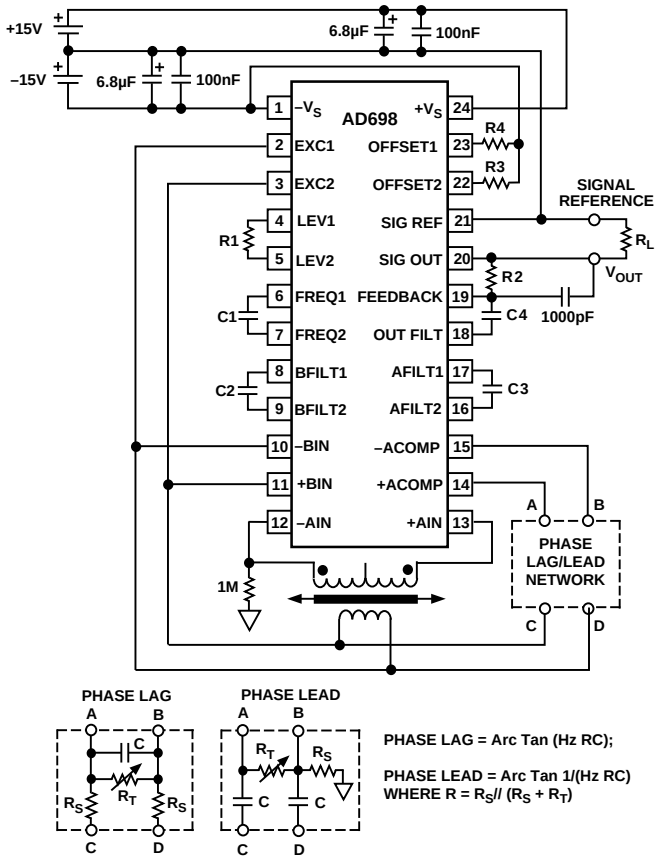


Figure 8. AD698 Interconnection Diagram for Series Opposed LVDT and Dual Supply Operation

B. Determine the Oscillator Amplitude

Amplitude is set such that the primary signal is in the 1.0 V to 3.5 V rms range and the secondary signal is in the 0.25 V to 3.5 V rms range when the LVDT is at its mechanical full-scale position. This optimizes linearity and minimizes noise susceptibility. Since the part is ratiometric, the exact value of the excitation is relatively unimportant.

5. Determine optimum LVDT excitation voltage, V_{EXC}. For a 4-wire LVDT determine the voltage transformation ratio, VTR, of the LVDT at its mechanical full scale. VTR = LVDT sensitivity × Maximum Stroke Length from null.

   LVDT sensitivity is listed in the LVDT manufacturer's catalog and has units of volts output per volts input per inch displacement. The E100 has a sensitivity of 2.4 mV/V/mil. In the event that LVDT sensitivity is not given by the manufacturer, it can be computed. See section on determining LVDT sensitivity.

Multiply the primary excitation voltage by the VTR to get the expected secondary voltage at mechanical full scale. For example, for an LVDT with a sensitivity of 2.4 mV/V/mil and a full scale of ±0.1 inch, the VTR = 0.0024 V/V/Mil × 100 mil = 0.24. Assuming the maximum excitation of 3.5 V rms, the maximum secondary voltage will be 3.5 V rms × 0.24 = 0.84 V rms, which is in the acceptable range.

Conversely the VTR may be measured explicitly. With the LVDT energized at its typical drive level V_{PRI}, as indicated by the manufacturer, set the core displacement to its mechanical full-scale position and measure the output V_{SEC} of the secondary. Compute the LVDT voltage transformation ratio, VTR. VTR = V_{SEC}//VPRI. For the E100, V_{SEC} = 0.72 V for V_{PRI} = 3 V. VTR = 0.24.

For situations where LVDT sensitivity is low, or the mechanical FS is a small fraction of the total stroke length, an input excitation of more than 3.5 V rms may be needed. In this case a voltage divider network may be placed across the LVDT primary to provide smaller voltage for the +BIN and –BIN input. If, for example, a network was added to divide the B Channel input by 1/2, then the VTR should also be reduced by 1/2 for the purpose of component selection.

Check the power supply voltages by verifying that the peak values of V_A and V_B are at least 2.5 volts less than the voltages at $+V_S$ and $-V_S$.

6. Referring to Figure 9, for V_S = ±15 V, select the value of the amplitude determining component R1 as shown by the curve in Figure 9.

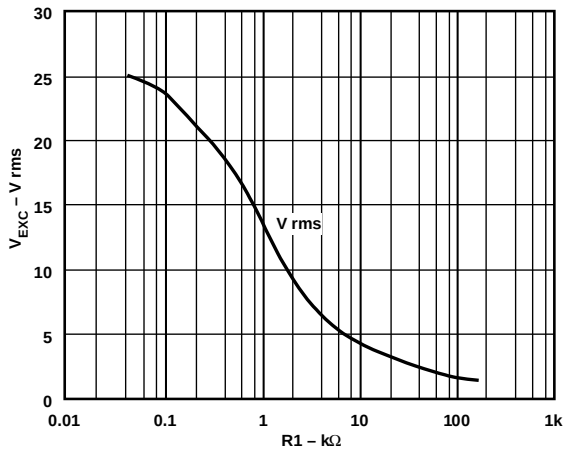


Figure 9. Excitation Voltage V_{EXC} vs. R1

7. C2, C3 and C4 are a function of the desired bandwidth of the AD698 position measurement subsystem. They should be nominally equal values.

$$C2 = C3 = C4 = 10^{-4}\ Farad\ Hz/f_{SUBSYSTEM}\ (Hz)$$

If the desired system bandwidth is 250 Hz, then

$$C2 = C3 = C4 = 10^{-4}\ Farad\ Hz/250\ Hz = 0.4\ \mu F$$

See Figures 14, 15 and 16 for more information about AD698 bandwidth and phase characterization.

D. Set the Full-Scale Output Voltage

8. To compute R2, which sets the AD698 gain or full-scale output range, several pieces of information are needed:

a. LVDT sensitivity, S

b. Full-scale core displacement from null, d

S × d = VTR and also equals the ratio A/B at mechanical full scale. The VTR should be converted to units of V/V.

For a full-scale displacement of d inches, voltage out of the AD698 is computed as

$$V_{OUT} = S \times d \times 500\ \mu A \times R2$$

V_{OUT} is measured with respect to the signal reference, Pin 21, shown in Figure 7.

Solving for R2,

$$R2 = \frac{V_{OUT}}{S \times d \times 500\ \mu A} \qquad (1)$$

For V_{OUT} = ±10 V full-scale range (20 V span) and d = ±0.1 inch full-scale displacement (0.2 inch span)

$$R2 = \frac{20\ V}{2.4 \times 0.2 \times 500\ \mu A} = 83.3\ k\Omega$$

V_{OUT} as a function of displacement for the above example is shown in Figure 10.

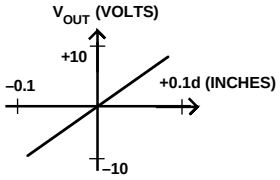


Figure 10. V_{OUT} (±10 V Full Scale) vs. Core Displacement (±0.1 Inch)

E. Optional Offset of Output Voltage Swing

9. Selections of R3 and R4 permit a positive or negative output voltage offset adjustment.

$$V_{OS} = 1.2\ V \times R2 \times \left(\frac{1}{R3 + 2\ k\Omega} - \frac{1}{R4 + 2\ k\Omega} \right) \qquad (2)$$

For no offset adjustment R3 and R4 should be open circuit.

To design a circuit producing a 0 V to +10 V output for a displacement of +0.1 inch, set V_{OUT} to +10 V, d = 0.2 inch and solve Equation (1) for R2.

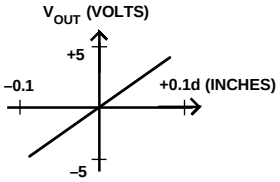


Figure 11. V_{OUT} (±5 V Full Scale) vs. Core Displacement (±0.1 Inch)

This will produce a response shown in Figure 11.

In Equation (2) set V_{OS} = 5 V and solve for R3 and R4. Since a positive offset is desired, let R4 be open circuit. Rearranging Equation (2) and solving for R3

$$R3 = \frac{1.2 \times R2}{V_{OS}} - 2\ k\Omega = 7.02\ k\Omega$$

Note that V_{OS} should be chosen so that R3 cannot have negative value .

Figure 12 shows the desired response.

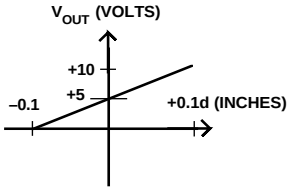


Figure 12. V_{OUT} (0 V–10 V Full Scale) vs. Displacement (±0.1 Inch)

DESIGN PROCEDURE

SINGLE SUPPLY OPERATION

Figure 13 shows the single supply connection method.

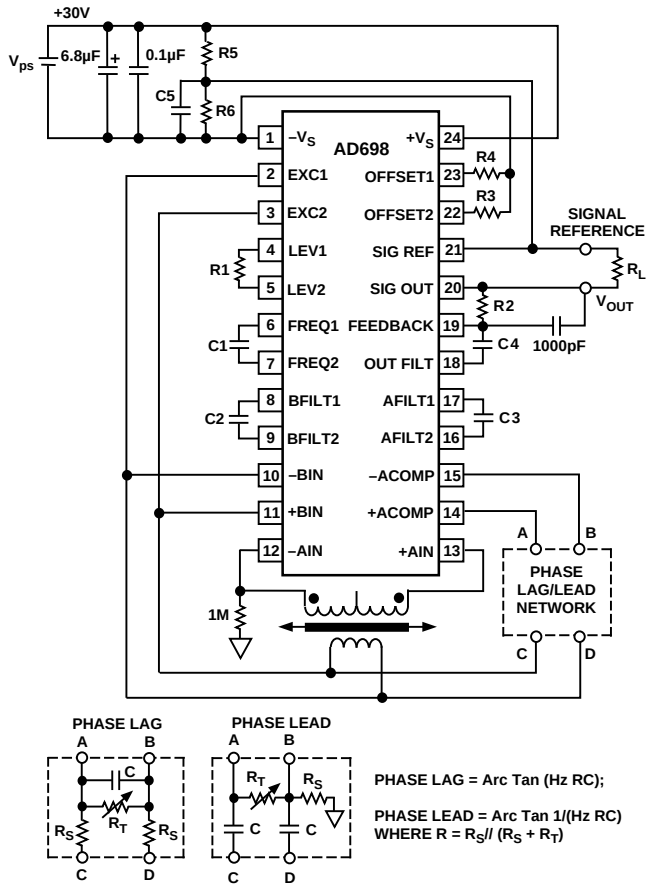


Figure 13. Interconnection Diagram for Single Supply Operation

For single supply operation, repeat Steps 1 through 10 of the design procedure for dual supply operation. R5, R6 and C5 are additional component values to be determined. V_{OUT} is measured with respect to SIGNAL REFERENCE.

10. Compute a maximum value of R5 and R6 based upon the relationship

$$R5 + R6 \le V_{PS}/100\ \mu A$$

11. The voltage drop across R5 must be greater than

$$2 + 10\ k\Omega \left(\frac{1.2V}{R4 + 2\ k\Omega} + 250\ \mu A + \frac{V_{OUT}}{4 \times R2} \right) Volts$$

Therefore

$$R5 \ge \frac{2 + 10\ k\Omega \left(\frac{1.2V}{R4 + 2\ k\Omega} + 250\ \mu A + \frac{V_{OUT}}{4 \times R2} \right)}{100\ \mu A} Ohms$$

Based upon the constraints of R5 + R6 (Step 10) and R5 (Step 11), select an interim value of R6.

12. Load current through R_L returns to the junction of R5 and R6, and flows back to V_{PS}. Under maximum load conditions, make sure the voltage drop across R5 is met as defined in Step 11.

    As a final check on the power supply voltages, verify that the peak values of V_A and V_B are at least 2.5 volts less than the voltage between $+V_S$ and $–V_S$.

13. C5 is a bypass capacitor in the range of 0.1 µF to 1 µF.

Gain Phase Characteristics

To use an LVDT in a closed-loop mechanical servo application, it is necessary to know the dynamic characteristics of the transducer and interface elements. The transducer itself is very quick to respond once the core is moved. The dynamics arise primarily from the interface electronics. Figures 14, 15 and 16 show the frequency response of the AD698 LVDT Signal Conditioner. Note that Figures 15 and 16 are basically the same; the difference is frequency range covered. Figure 15 shows a wider range of mechanical input frequencies at the expense of accuracy.

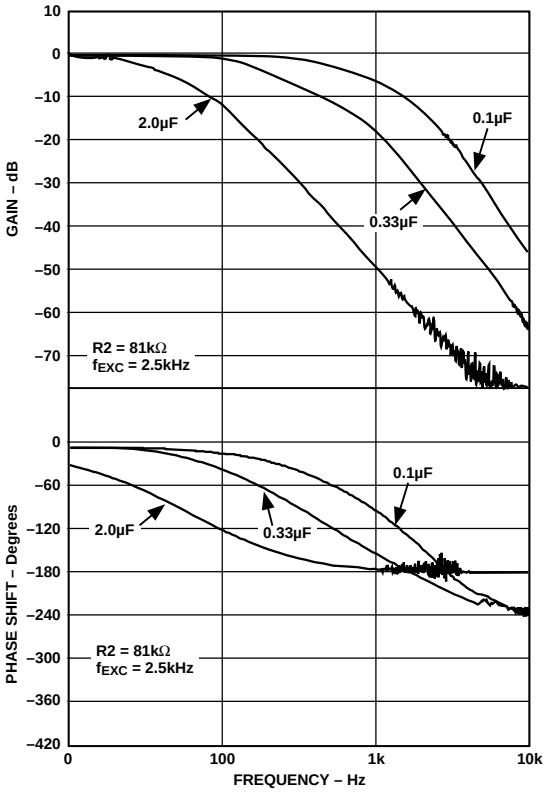


Figure 14. Gain and Phase Characteristics vs. Frequency (0 kHz–10 kHz)

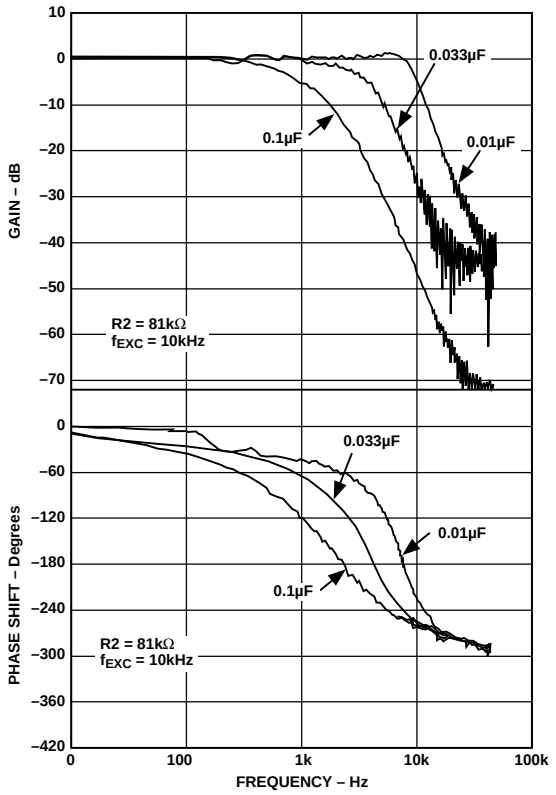


Figure 15. Gain and Phase Characteristics vs. Frequency (0 kHz–50 kHz)

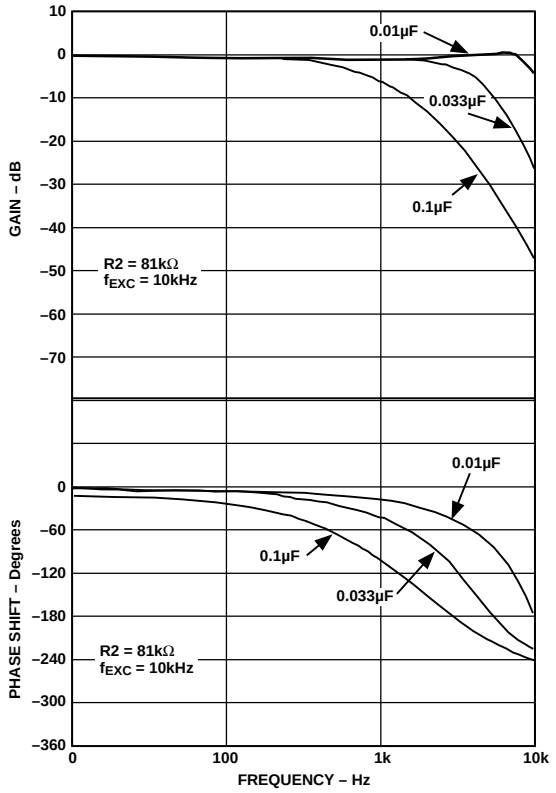


Figure 16. Gain and Phase Characteristics vs. Frequency (0 kHz–10 kHz)

Figure 16 shows a more limited frequency range with enhanced accuracy. The figures are transfer functions with the input to be considered as a sinusoidally varying mechanical position and the output as the voltage from the AD698; the units of the transfer function are volts per inch. The value of C2, C3, and C4, from Figure 7, are all equal and designated as a parameter in the figures. The response is approximately that of two real poles. However, there is appreciable excess phase at higher frequencies. An additional pole of filtering can be introduced with a shunt capacitor across R2, Figure 7; this will also increase phase lag.

When selecting values of C2, C3 and C4 to set the bandwidth of the system, a trade-off is involved. There is ripple on the "dc" position output voltage, and the magnitude is determined by the filter capacitors. Generally, smaller capacitors will give higher system bandwidth and larger ripple. Figures 17 and 18 show the magnitude of ripple as a function of C2, C3 and C4, again all equal in value. Note also a shunt capacitor across R2, Figure 7, is shown as a parameter. The value of R2 used was 81 kΩ with a Schaevitz E100 LVDT.

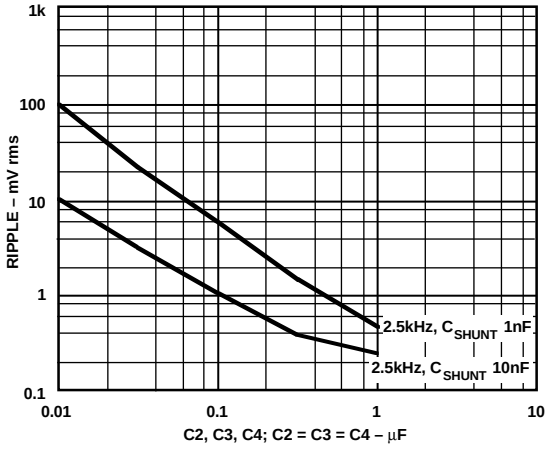


Figure 17. Output Voltage Ripple vs. Filter Capacitance

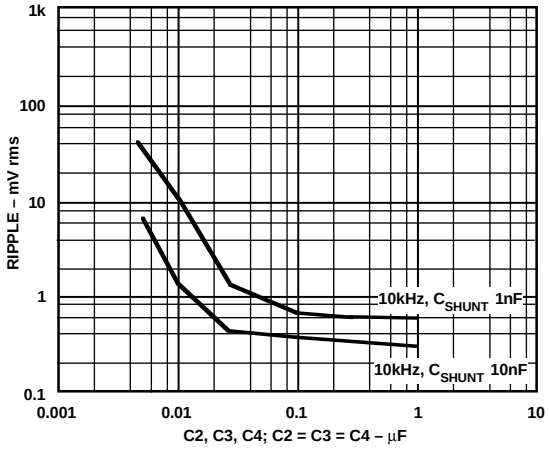


Figure 18. Output Voltage Ripple vs. Filter Capacitance

Determining LVDT Sensitivity
LVDT sensitivity can be determined by measuring the LVDT secondary voltages as a function of primary drive and core position, and performing a simple computation.

Energize the LVDT at its recommended primary drive level, V_{PRI} (3 V rms for the E100). Set the core displacement to its mechanical full-scale position and measure secondary voltages V_A and V_B.

$$Sensitivity = \frac{V_{SECONDARY}}{V_{PRI} \times d}$$

From Figure 19,

$$Sensitivity = \frac{0.72}{3\,V \times 100\ mils} = 2.4\ mV/V\ mil$$

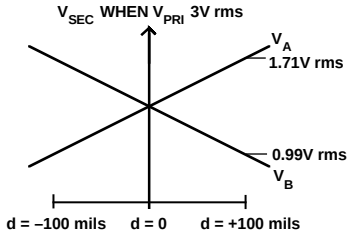


Figure 19. LVDT Secondary Voltage vs. Core Displacement

Thermal Shutdown and Loading Considerations
The AD698 is protected by a thermal overload circuit. If the die temperature reaches 165°C, the sine wave excitation amplitude gradually reduces, thereby lowering the internal power dissipation and temperature.

Due to the ratiometric operation of the decoder circuit, only small errors result from the reduction of the excitation amplitude. Under these conditions the signal-processing section of the AD698 continues to meet its output specifications.

The thermal load depends upon the voltage and current delivered to the load as well as the power supply potentials. An LVDT Primary will present an inductive load to the sine wave excitation. The phase angle between the excitation voltage and current must also be considered, further complicating thermal calculations.

APPLICATIONS
Most of the applications for the AD598 can also be implemented with the AD698. Please refer to the applications written for the AD598 for a detailed explanation.

See AD598 data sheet for:

– Proving Ring-Weigh Scale
– Synchronous Operation of Multiple LVDTs
– High Resolution Position-to-Frequency Circuit
– Low Cost Setpoint Controller
– Mechanical Follower Servo Loop
– Differential Gaging and Precision Differential Gaging

AC BRIDGE SIGNAL CONDITIONER
Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, 1/f noise, dc drifts in the electronics, and line noise pickup. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low-pass filter.

The AD698 with the addition of a simple ac gain stage can be used to implement an ac bridge. Figure 20 shows the connections for such a system. The AD698 oscillator provides ac excitation for the bridge. The low level bridge signal is amplified by the gain stage created by A1, A2 to provide a differential input to the A Channel of the AD698. The signal is then synchronously detected by A Channel. The B Channel is used to detect the level of the bridge excitation. The ratio of A/B is then calculated and converted to an output voltage by R2. An optional phase lag/lead network can be added in front of the A comparator to adjust for phase delays through the bridge and the amplifier, or if the phase delay is small, it can be ignored or compensated for by a gain adjustment.

This circuit can be used for resistive bridges such as strain gages, or for inductive or capacitive bridges that are commonly used for pressure or flow sensors. The low level signal outputs of these sensors are susceptible to noise and interference and are good candidates for ac signal processing techniques.

Component Selection
Amplifiers A1, A2 will be chosen depending on the type of bridge that is conditioned. Capacitive bridges should use an amplifier with low bias current; a large bleeder resistor will be required from the amplifier inputs to ground to provide a path for the dc bias current. Resistive and inductive bridges can use a more general purpose amplifier. The dc performance of A1, A2 are not as important as their ac performance. DC errors such as voltage offset will be chopped out by the AD698 since they are not synchronous to the carrier frequency.

The oscillator amplitude and span resistor for the AD698 may be chosen by first computing the transfer function or sensitivity of the bridge and the ac amplifier. This ratio will correspond to the A/B term in the AD698 transfer function. For example, suppose that a resistive strain gage with a sensitivity, S, of 2 mV/V at full scale is used. Select an arbitrary target value for A/B that is close to its maximum value such as A/B = 0.8. Then choose a gain for the ac amplifier so that the strain gage transfer function from excitation to output also equals 0.8. Thus the required amplifier gain will be [A/B]/ S; or 0.8/ 0.002 V/V = 400. Then select values for R_S and R_G. For the gain stage:

$$V_{OUT} = \left[\frac{2 \times R_S}{R_G + 1}\right] \times V_{IN}$$

Solving for V_{OUT}/V_{IN} = 400 and setting R_G = 100 Ω then:

$$R_S = [400 - 1] \times R_G/2 = 19.95\ k\Omega$$

Choose an oscillator amplitude that is in the range of 1 V to 3.5 V rms. For an input excitation level of 3 V rms, the output signal from the amplifier gain stage will be 3.5 V rms × 0.8 V or 2.4 V rms, which is in the acceptable range.

Since A/B is known, the value of R2, the output FS resistor may be chosen by the formula:

$$V_{OUT} = A/B \times 500\ \mu A \times R2$$

For a 10 V output at FS, with an A/B of 0.8; solve for R2.

$$R2 = 10\ V\ [0.8 \times 500\ \mu A] = 25.0\ k\Omega$$

This will result in a V_{OUT} of 10 V for a full-scale signal from the bridge. The other components, C1, C2, C3, C4 may be selected by following the guidelines on general device operation mentioned earlier.

If a gain trim is required, then a trim resistor can be used to adjust either R2 or R_G. Bridge offsets should be adjusted by a trim network on the OFFSET 1 and OFFSET 2 pins of the AD698.

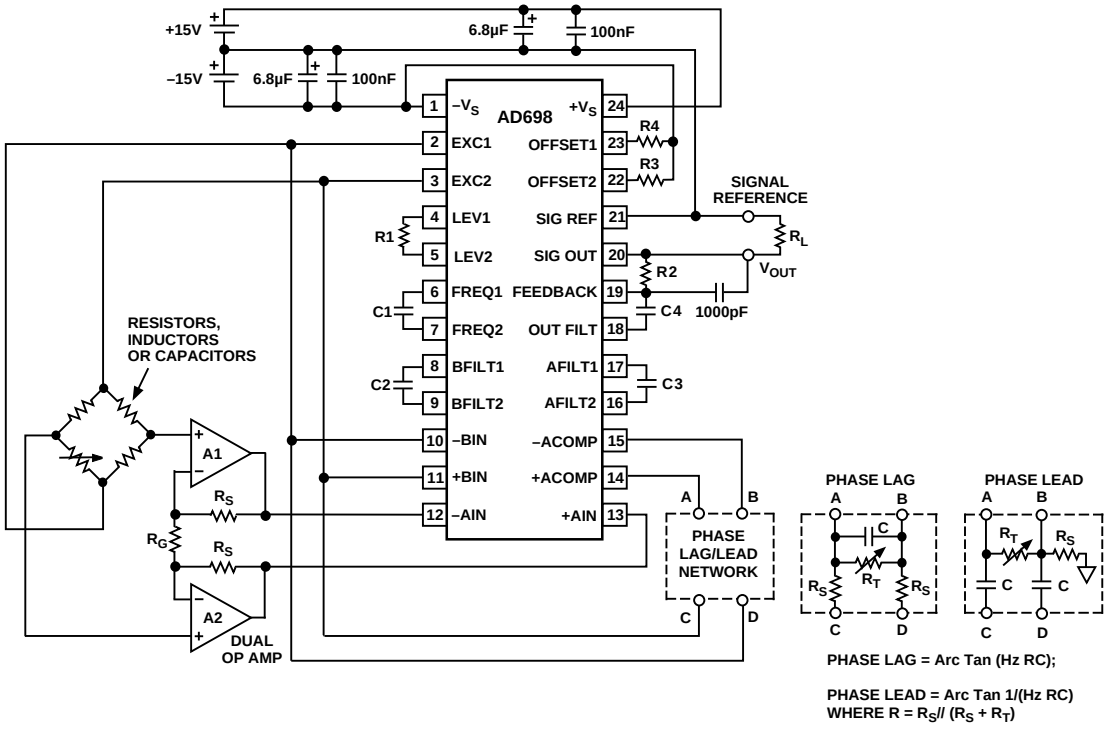
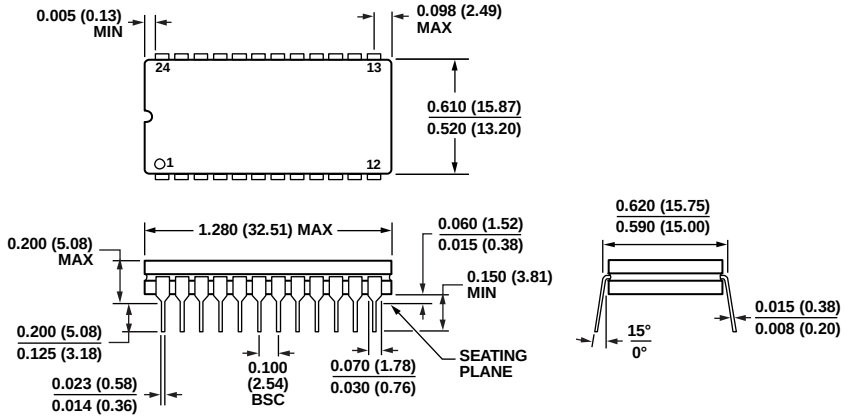


Figure 20. AD698 Interconnection Diagram for AC Bridge Applications

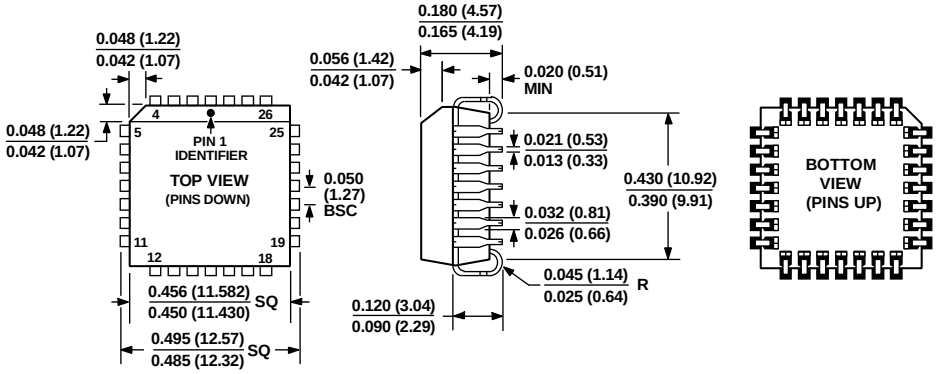
OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

081908-A

Figure 1. 24-Lead Ceramic Dual In-Line Package [CERDIP]
Wide Body
(Q-24-2)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-047-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

042508-A

Figure 2. 28-Lead Plastic Leaded Chip Carrier [PLCC]
(P-28)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD698AP	−40°C to +85°C	28-Lead PLCC	P-28
AD698APZ	−40°C to +85°C	28-Lead PLCC	P-28
AD698SQ	−55°C to +125°C	24-Lead CERDIP	Q-24-2

[1] Z = RoHS Compliant Part.

REVISION HISTORY

1/2018—Rev. B to Rev. C

Updated Outline Dimensions....12
Changes to Ordering Guide....12