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Freescale Semiconductor
Advance Information

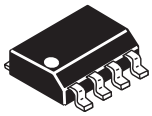
Document Number: MC34653
Rev. 8.0, 2/2007

RoHS

1.0 A Negative Voltage Hot Swap Controller

34653

HOT SWAP



EF SUFFIX (Pb-Free)
98ASB42564B
8-PIN SOICN

The 34653 is a highly integrated -48 V hot swap controller with an internal Power MOSFET. It provides the means to safely install and remove boards from live -48 V backplanes without having to power down the entire system. It regulates the inrush current, from the supply to the load's filter capacitor, to a user-programmable limit, allowing the system to safely stabilize. A disable function allows the user to disable the 34653 manually or through a microprocessor and safely disconnect the load from the main power line.

The 34653 has active high and active low power good output signals that can be used to directly enable a power module load. Undervoltage and overvoltage detection circuitry monitors the input voltage to check that it is within its operating range. A start-up delay timer ensures that it is safe to turn on the Power MOSFET and charge the load capacitor.

A two-level current limit approach to controlling the inrush current and switching on the load limits the peak power dissipation in the Power MOSFET. Both current limits are user programmable.

Features

- Integrated Power MOSFET and Control IC in a Small Outline Package
- Input Voltage Operation Range from -39 V to -74 V
- Programmable Overcurrent Limit with Auto Retry
- Programmable Charging Current Limit Independent of Load Capacitor
- Start-Up and Retry Delay Timer
- Overvoltage and Undervoltage Detection
- Active High and Low Power Good Output Signals
- Thermal Shutdown
- Pb-Free Packaging Designated by Suffix Code EF

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MCZ34653EF/R2	-40°C to 85°C	8 SOICN
MC34653EF/R2		

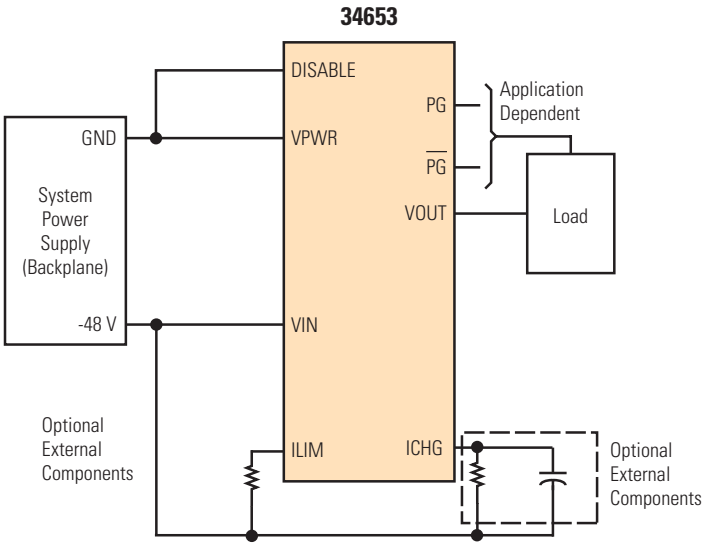


Figure 1. 34653 Simplified Application Diagram

* This document contains certain information on a new product.
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INTERNAL BLOCK DIAGRAM

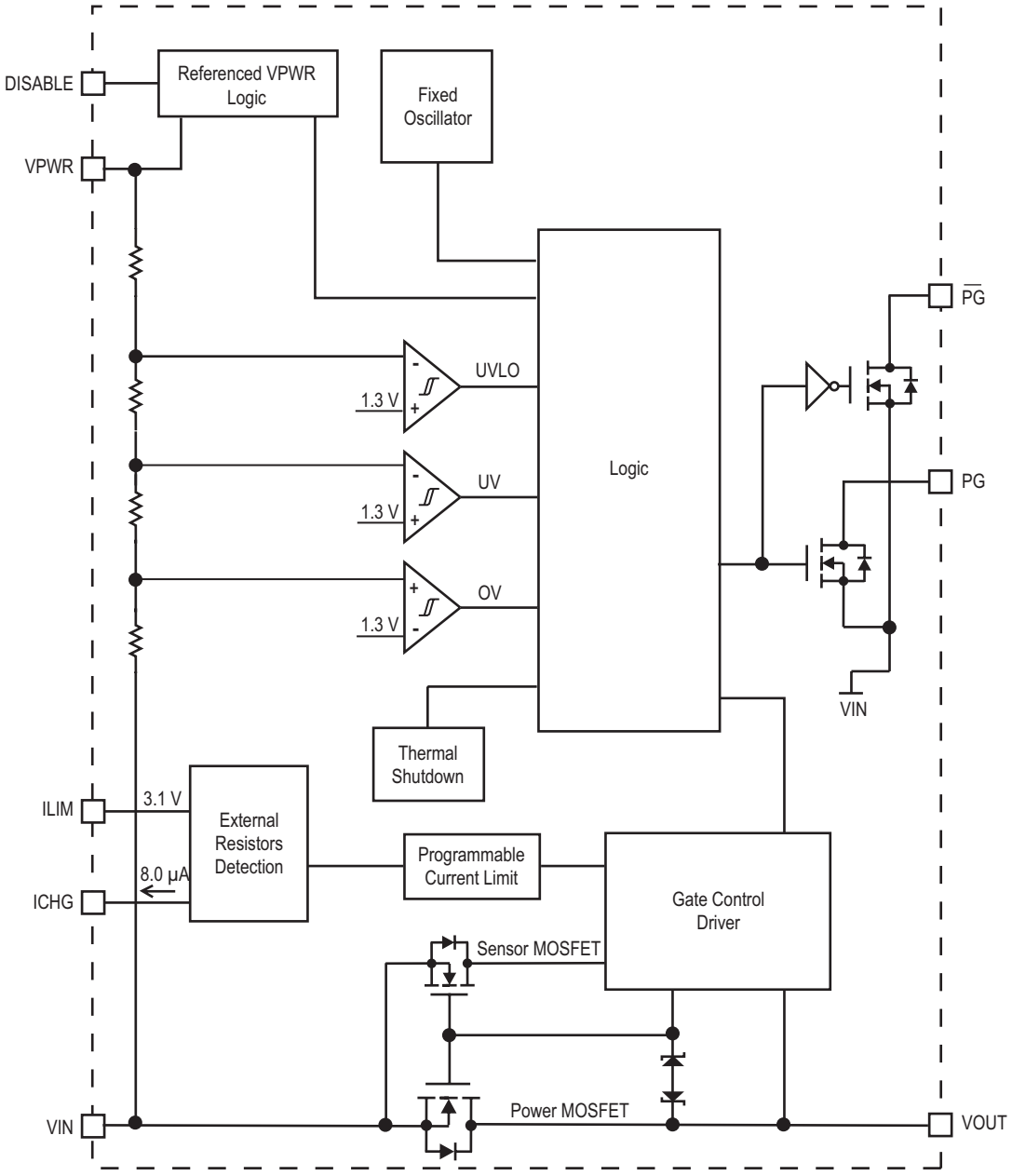

Figure 2. 34653 Simplified Internal Block Diagram

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PIN CONNECTIONS

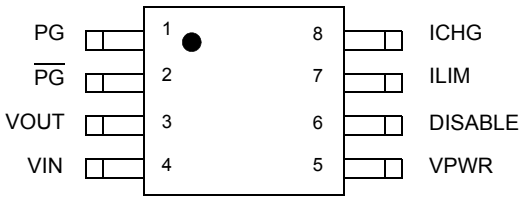

Figure 3. 8-SOICN Pin Connections

Table 1. 8-SOICN Pin Definitions

A functional description of each pin can be found in the FUNCTIONAL PIN DESCRIPTION section beginning on page 8.

Pin	Pin Name	Formal Name	Definition
1	PG	Power Good Output (Active High)	This is an active high power good output signal. This pin is referenced to VIN.
2	$\overline{PG}$	Power Good Output (Active Low)	This is an active low power good output signal. This pin is referenced to VIN.
3	VOUT	Voltage Output	This pin is the drain of the internal Power MOSFET and supplies a current limited voltage to the load.
4	VIN	Negative Supply Voltage Input	This is the most negative power supply input. All pins except DISABLE are referenced to this input.
5	VPWR	Positive Supply Voltage Input	This is the most-positive power supply input. The load connects between this pin and the VOUT pin.
6	DISABLE	Disable Input Control	This pin is used to easily disconnect or connect the load from the main power line by disabling or enabling the 34653. It can also be used to reset the fault conditions that cause a “Power No Good” signal. This pin is referenced to VPWR.
7	ILIM	Current Limit Control	This pin is used to set the overcurrent limit during normal operation.
8	ICHG	Charging Current Limit Control	This pin is used to set the load’s input capacitor charging current limit, hence limiting the inrush current to a known constant value.

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ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage	V_{PWR}	85	V
Power MOSFET Energy Capability	E_{MOSFET}	Varies (1)	mJ
Continuous Output Current (2)	$I_{O(CONT)}$	1.0	A
Maximum Voltage			V
DISABLE Pin	—	V_{IN} - 0.3 to V_{PWR} + 5.5	
ILIM and ICHG Pins	—	5.0	
PG Pin (V_{PG} - V_{IN})	—	85	
$\overline{PG}$ Pin ($V_{\overline{PG}}$ - V_{IN})	—	85	
All Pins Minimum Voltage	—	-0.3	V
PG, $\overline{PG}$ Maximum Current	—	Internally Limited	A
ESD Voltage, All Pins (3)			V
Human Body Model	V_{ESD3}	±2000	
Machine Model	V_{ESD4}	±200	
THERMAL RATINGS			
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature			°C
Ambient (4)	T_A	-40 to 85	
Junction	T_J	-40 to 160	
Peak Package Reflow Temperature During Reflow (5), (6)	T_{PPRT}	Note 6	°C
Thermal Resistance (7), (8)			°C/W
Junction-to-Ambient, Single-Layer Board (9)	$R_{\theta JA}$	167	
Junction-to-Ambient, Four-Layer Board (10)	$R_{\theta JMA}$	115	

Notes

1. Refer to the section titled Power MOSFET Energy Capability on page 21 for a detailed explanation on this parameter.
2. Continuous output current capability so long as T_J is ≤ 160°C.
3. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP}=100 pF, R_{ZAP}=1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω).
4. The limiting factor is junction temperature, taking into account power dissipation, thermal resistance, and heatsinking.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
7. Refer to the section titled Thermal Shutdown on page 15 for more thermal resistance values under various conditions.
8. The VOUT and VIN pins comprise the main heat conduction paths.
9. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
10. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal. There are no thermal vias connecting the package to the two planes in the board.

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STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 36 V ≤ V_{PWR} ≤ 80 V and -40°C ≤ T_A ≤ 85°C. All voltages are referenced to VIN unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY PIN (VPWR)					
Supply Voltage	V_{PWR}	36	—	80	V
Operating Voltage Range	V_{PWR}	$V_{UV(ON)}$		$V_{OV(ON)}$	V
Supply Current, Device Enabled, Default Mode, Normal Operation (11)	I_{IN}	—	900	1400	µA
Undervoltage Lockout Threshold (UVLO)					V
Rising	V_{UVLOR}	7.0	8.0	9.0	
Falling	V_{UVLOF}	6.0	7.0	8.0	
Hysteresis	V_{UVLOHY}	—	1.0	—	
UNDERVOLTAGE CONTROL					
UV Threshold (Default)					V
Rising	$V_{UV(ON)}$	—	38	—	
Falling	$V_{UV(OFF)}$	—	37	—	
Hysteresis	V_{UVHY}	—	1.0	—	
OVERVOLTAGE CONTROL					
OV Threshold (Default)					V
Rising	$V_{OV(OFF)}$	—	78	—	
Falling	$V_{OV(ON)}$	—	76	—	
Hysteresis	V_{OVHY}	—	2.0	—	
DISABLE INPUT CONTROL PIN (DISABLE) (12)					
DISABLE Input Voltage					V
Inactive State	V_{DISL}	V_{PWR} - 1.2	—	V_{PWR} + 1.2	
Active State, Positive Signal	V_{DISHP}	V_{PWR} + 2.0	—	—	
Active State, Negative Signal	V_{DISHN}	—	—	V_{PWR} - 2.0	
DISABLE Input Current	I_{DIS}				µA
V_{DIS} = V_{PWR} + 3.3 V		20	60	140	
V_{DIS} = V_{PWR} - 3.3 V		-20	-60	-140	
V_{DIS} = V_{IN}		-50	-150	-250	

Notes

11. The supply current depends on operation mode and can be calculated as follows:
    - Start-Up Mode: I_{IN} = 539 µA + 548 µ * I_{CHG}(A) + 216 µ * I_{LIM}(A) + V_{PWR}(V) / 460(kΩ)
    - Normal Mode: I_{IN} = 539 µA + 240 µ * I_{LIM}(A) + 288 µ * I_{LOAD}(A) + V_{PWR}(V) / 460(kΩ)
    - Overcurrent Mode: I_{IN} = 539 µA + 612 µ * I_{LIM}(A) + V_{PWR}(V) / 460(kΩ)
    - Disable Mode: I_{IN} = 539 µA + 240 µ * I_{LIM}(A) + I_{DIS}(µA) + V_{PWR}(V) / 460(kΩ)
12. Referenced to VPWR.

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Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 36 V ≤ V_{PWR} ≤ 80 V and -40°C ≤ T_A ≤ 85°C. All voltages are referenced to VIN unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT LIMIT PINS (ILIM, ICHG)					
Overcurrent Limit Steady State	I_{LIM}				A
Default		—	1.0	—	
Maximum with External Resistor		—	1.25	—	
Minimum with External Resistor		—	0.15	—	
Current Limit During Start-Up	I_{CHG}				A
Default		—	0.1	—	
Maximum with External Resistor		—	0.5	—	
Minimum with External Resistor		—	0.05	—	
Short Circuit Current Limit	I_{SHORT}	—	5.0	—	A
I_{LIM} Current Limit Hysteresis	I_{LIMHY}	—	12	—	%
I_{LIM} Current Limit Accuracy	I_{LIMCLA}	-20	—	20	%
I_{CHG} Current Limit Accuracy	I_{CHGCLA}	-35	—	35	%
ILIM Pin Voltage	V_{ILIM}	—	3.1	—	V
I_{LIM} to R_{ILIM} Setting Constant	I_{LIMCNS}	—	129	—	A * kΩ
I_{CHG} Reference Current	I_{CHGOUT}	—	-8.0	—	µA
I_{CHG} to R_{ICHG} Setting Constant	I_{CHGCNS}	—	335	—	kΩ/A
POWER GOOD PINS (PG, $\overline{PG}$) (13)					
Power Good Output Low Voltage	V_{PGL}				V
I_{PG} = 1.6 mA		—	—	0.5	
Power Good Leakage Current	I_{PGLG}	—	—	10	µA
Power Good Current Limit	I_{PGCL}				mA
V_{PG} or $V_{\overline{PG}}$ = 3.0 V		—	—	7.0	
OUTPUT VOLTAGE PIN (VOUT)					
VOUT Leakage Current	I_{OUTLG}	—	—	50	µA
POWER MOSFET					
ON Resistance @ 25°C	$R_{DS(ON)}$	—	144	—	mΩ
THERMAL SHUTDOWN					
Thermal Shutdown Temperature	T_{SD}	—	160	—	°C
Thermal Shutdown Temperature Hysteresis	T_{SDHY}	—	25	—	°C

Notes
13. Referenced to VIN.

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DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 36 V ≤ V_{PWR} ≤ 80 V and -40°C ≤ T_A ≤ 85°C. All voltages are referenced to VIN unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
UNDERVOLTAGE CONTROL					
Undervoltage Active to Gate Low Filter Time	t_{UVAL}	—	1.0	—	ms
OVERVOLTAGE CONTROL					
Overvoltage Active to Gate Low Filter Time	t_{OVAL}	—	1.0	—	ms
DISABLE INPUT CONTROL PIN (DISABLE) (14)					
DISABLE Active to Gate Low Filter Time	t_{DISAL}	—	1.0	—	ms
CURRENT LIMIT CONTROL PINS (ILIM, ICHG)					
Short Circuit Protection Delay	t_{SCPD}	—	—	10	µs
Overcurrent Limit Filter Time	t_{OCFT}	—	100	—	µs
Overcurrent Limit Regulation Time	t_{OC}	—	3.0	—	ms
I_{CHG} Rise Time	t_{ICHGR}				ms
Default		—	1.0	—	
Adjustable with an External Capacitor		1.0	—	—	
POWER GOOD OUTPUT PINS (PG, $\overline{PG}$) (15)					
Power Good Output Delay Time, from Power MOSFET Enhancement to PG and $\overline{PG}$ Asserted	t_{PG}	10	28	46	ms
FAULT TIMER					
Start-Up and Retry Delay Timer	t_{TIMER}				ms
Default		130	200	270	

Notes
14. Referenced to VPWR.
15. Referenced to VIN.

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FUNCTIONAL DESCRIPTION

INTRODUCTION

Most telecom and data transfer networks require that circuit boards be inserted and removed from the system without powering down the entire system. When a circuit board is inserted into or removed from a live backplane, the filter or bypass capacitors at the input of the board's power module or switching power supply can cause large transient currents when being charged or discharged. These currents can cause severe and permanent damage to the boards, thus making the system unstable. Figure 4 displays the inrush current to the filter capacitor if a hot swap device is absent. The inrush current reached an unsafe value of more than 55 A.

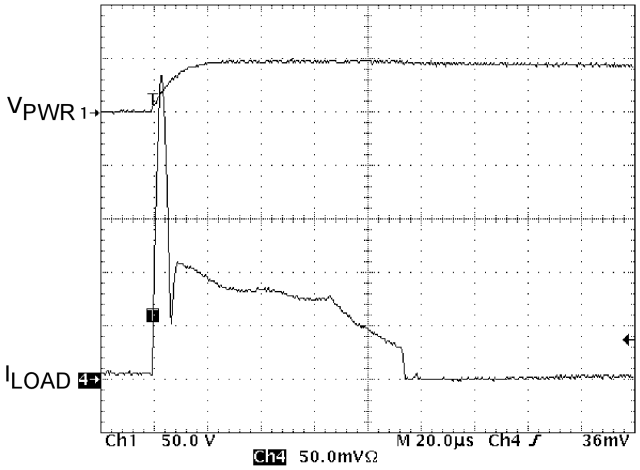

Figure 4. Circuit Board Insertion Without a Hot Swap Device, Inrush Current Not Limited

The 34653 is an integrated negative voltage hot swap controller with an internal Power MOSFET. The 34653 resides on the plug-in boards and allows the boards to be safely inserted or removed by powering up the supply voltages in a controlled manner and regulating the inrush current to a user-programmable limit, thus allowing the system to safely stabilize (see Figure 5). The 34653 provides protection against overcurrent, undervoltage, overvoltage, and overtemperature. Furthermore, it protects the system from short circuits.

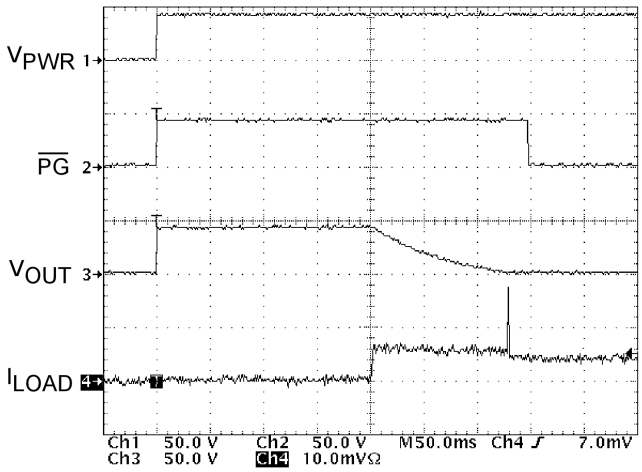

Figure 5. Circuit Board Insertion With the Hot Swap Device, Inrush Current Limited

By integrating the control circuitry and the Power MOSFET switch into a space-efficient package, the 34653 offers a complete, cost-effective, and simple solution that takes much less board space than a similar part with an external Power MOSFET requires.

The 34653 can be used in -48 V telecom and networking systems, servers, electronic circuit breakers, -48 V distributed power systems, negative power supply control, and central office switching.

FUNCTIONAL PIN DESCRIPTION

NEGATIVE SUPPLY INPUT VOLTAGE (VIN)

This is the most negative power supply input. All pins except DISABLE, PG, and $\overline{PG}$ are referenced to this input.

POWER GOOD OUTPUT (ACTIVE HIGH) (PG)

The PG pin is the active high power good output signal that is used to enable or disable a load. This signal goes active after a successful power-up sequence and stays active as long as the device is in normal operation and is not experiencing any faults.

The signal is deactivated under the following conditions:

- Power is turned off.
- The device is disabled for more than 1.0 ms.
- The device exceeded its thermal shutdown threshold for more than 12 µs.
- The device is in overvoltage or undervoltage mode for more than 1.0 ms.
- Load current exceeded the overcurrent limit for more than 3.0 ms.

This pin is referenced to VIN.

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POWER GOOD OUTPUT (ACTIVE LOW) $\overline{PG}$

The $\overline{PG}$ pin is the active low power good output signal that is used to enable or disable a load. This signal goes active after a successful power-up sequence and stays active as long as the device is in normal operation and is not experiencing any faults.

The signal is deactivated under the following conditions:

- Power is turned off.
- The device is disabled for more than 1.0 ms.
- The device exceeded its thermal shutdown threshold for more than 12 μs.
- The device is in overvoltage or undervoltage mode for more than 1.0 ms.
- Load current exceeded the overcurrent limit for more than 3.0 ms.

This pin is referenced to VIN.

OUTPUT VOLTAGE (VOUT)

The VOUT pin is the drain of the internal Power MOSFET and supplies a current-limited voltage to the load. The load connects between the VOUT and VPWR pins.

POSITIVE SUPPLY VOLTAGE INPUT (VPWR)

The VPWR pin is the most-positive power supply input. The load connects between the VPWR and VOUT pins.

DISABLE INPUT CONTROL (DISABLE)

The DISABLE pin is used to easily disconnect or connect the load from the main power line by disabling or enabling the 34653. It can also be used to reset the fault conditions that cause a “Power No Good” signal.

If left open or connected to VPWR, the DISABLE pin is inactive and the device is enabled. If a positive voltage (above V_{PWR}) or a negative voltage (below V_{PWR}) is applied to DISABLE, it is active and the device is disabled. The disable function has a 1.0 ms filter timer.

This pin is referenced to VPWR.

CURRENT LIMIT CONTROL (ILIM)

The ILIM pin is used to set the overcurrent limit during normal operation. This pin can be left unconnected for a default overcurrent limit value of 1.0 A or the user can connect an external resistor between the ILIM and VIN pins to set the overcurrent limit value. This value can vary between 0.15 A and 1.25 A. The overcurrent detection circuit has a 100 μs filter timer.

CHARGING CURRENT LIMIT CONTROL (ICHG)

The ICHG pin is used to set the current limit that is used to charge the load’s input capacitor, hence limiting the inrush current to a known constant value. This pin can be left unconnected for a default charging current limit value of 0.1 A and a default I_{CHG} rise time of 1.0 ms. Or the user can connect an external resistor between the ICHG and VIN pins to set the current limit value between 0.05 A and 0.5 A and an external capacitor to increase the I_{CHG} rise time. The recommended maximum rise time is 10 ms.

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FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

START-UP SEQUENCE

When power is first applied to the 34653 by connecting the VIN pin to the negative voltage rail and the VPWR pin to the positive voltage rail, the 34653 keeps the Power MOSFET turned off, deactivates the power good output signals, and resets the retry counter. If the device is disabled, no further activities will occur and power-up would not start. If the device is enabled, it starts to establish an internally regulated supply voltage required for the internal circuitry. The Power MOSFET will stay off until the start of the charging process.

After the Power-ON Reset (POR) and once the Undervoltage Lockout (UVLO) threshold is cleared, the 34653 checks for external components on two pins—ILIM and ICHG—to set the levels of the Overcurrent Limit and the Charging Current Limit, respectively. The device then initiates the start-up timer (Point A in Figure 6) and checks for the start-up conditions (see next paragraph). The duration of the timer is a default value. For undervoltage and overvoltage faults during power up the 34652 retries infinitely until normal input voltage is attained. If the die temperature ever increased beyond the thermal shutdown threshold or the device is disabled, then the start-up timer resets and the retry counter increments. If after 10 retries the die temperature is still high and the device is still disabled, the 34652 will not retry again and the power in the device must be recycled or the device must be disabled to reset the retry counter.

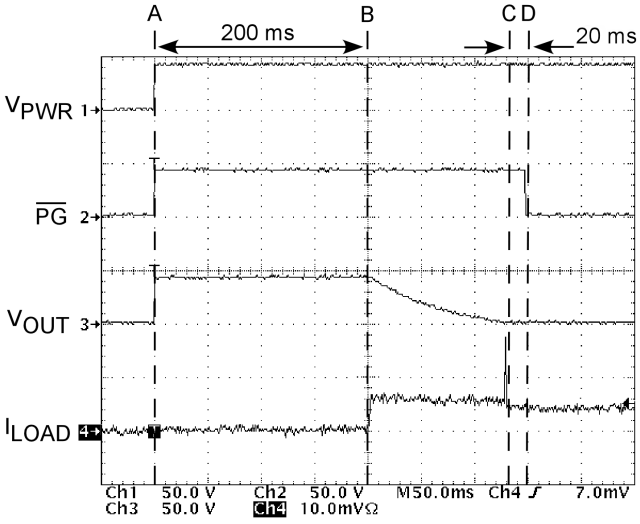

Figure 6. Start-Up Sequence

Start-Up Conditions

The start-up conditions are as follows:

- Input voltage is below the overvoltage turn-off threshold. This threshold is a default.
- Input voltage is above the undervoltage turn-off threshold. This threshold is a default.
- Die temperature is less than the thermal shutdown temperature.
- Device is enabled.

If the start-up conditions are satisfied for a time equal to the length of the start-up timer and the retry counter is less than or equal to 10, the device starts to turn on the Power MOSFET gradually to control the inrush current that charges up the load capacitor to eventually switch on the load (Point B in Figure 6).

Charging Process

When charging a capacitor from a fixed voltage source, a definite amount of energy will be dissipated in the control circuit, no matter what the control algorithm is. This energy is equal to the energy transferred to the capacitor—$\frac{1}{2}CV^2$. With this in mind, the Power MOSFET in the 34653 cannot absorb this pulse of energy instantaneously, so the pulse must be dissipated over time. To limit the peak power dissipation in the Power MOSFET and to spread out the duration of the energy dissipation in the Power MOSFET, the circuit uses a two-level current approach to controlling the inrush current and switching on the load as explained in the following paragraphs.

When the Power MOSFET is turned on, the current limit is set gradually from 0 A to I_{CHG} (between Points A and B in Figure 7). The low charging current value and the gradual rise time of I_{CHG} are either defaults or they can be user programmable (2.0 ms rise time in the example in Figure 7). The low charging current value of I_{CHG} is intended to limit the temperature increase during the load capacitor charging process, and the gradual rise to I_{CHG} is to prevent transient dips in the input voltage due to sharp increases in the current. This prevents the input voltage from drooping due to current steps acting on the input line inductance, and that in turn prevents a premature activation of the UV detection circuit.

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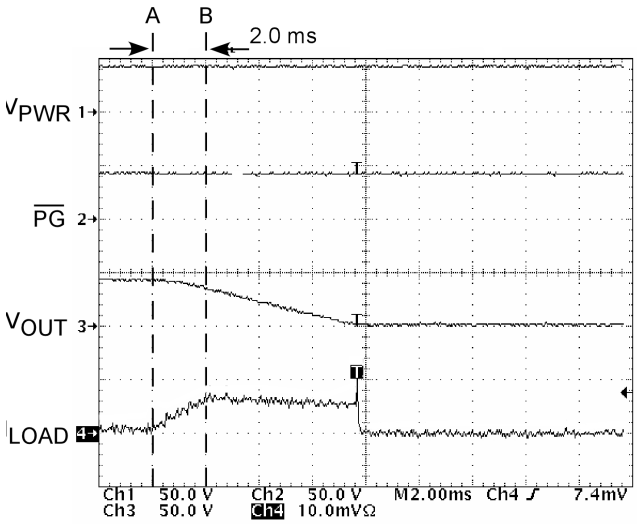

Figure 7. Power MOSFET Turn-On and the Gradual Increase in the Charging Current from 0 A to I_{CHG} (2.0 ms in Example)

The I_{CHG} current charges up the load capacitor relatively slowly. When the load capacitor is fully charged, the Power MOSFET reaches its full enhancement, which triggers the current limit detection to change from I_{CHG} to I_{LIM} and the load current to decrease (Point C in Figure 6, page 10). The current spike at Point C in Figure 6 is better displayed in Figure 8. We can see that when the $|V_{OUT} - V_{IN}| < 0.5$ V, the Power MOSFET fully turns on to reach its full enhancement, charging the capacitor an additional 0.5 V with a higher current value that quickly ramps down. This eliminates the need for a current slew rate control because the hazard for a voltage change is less than 0.5 V. The power good output signals activate after a 20 ms delay (Point D in Figure 6), which in turn enables the load. The 34653 is now in normal operation mode and the retry counter resets.

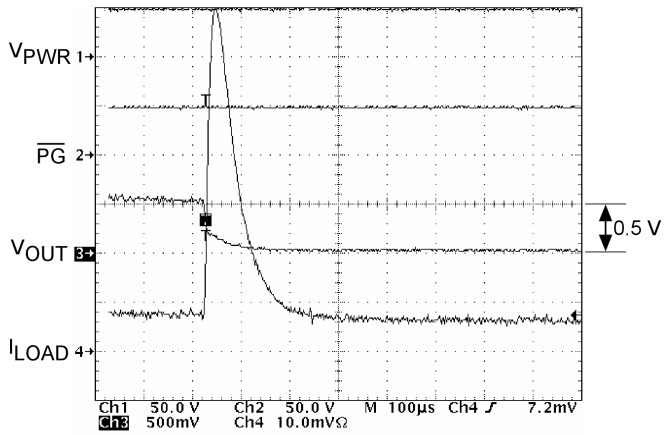

Figure 8. Full Power MOSFET Turn-On and Current Spike Associated with It. End of Charging Process

NORMAL MODE

If one of the start-up conditions (list on page 10) is violated any time from the start of the Power MOSFET enhancement process and thereafter during normal operation, the Power MOSFET turns off and the power good output signals deactivate, disabling the load, and a new timer cycle starts as explained previously. The 34653 also monitors the load current to prevent any overload or short circuit conditions from happening to protect the load from damage.

LOAD CURRENT CONTROL

When in normal operation mode, the 34653 monitors the load and provides two modes of current control as explained in the paragraphs below.

Overcurrent Mode

The 34653 monitors the load for overcurrent conditions. If the current going through the load becomes larger than the overcurrent limit for longer than the overcurrent limit filter timer of 100 µs, the overcurrent signal is asserted and the gate of the Power MOSFET is discharged to try to regulate the current at the I_{LIM} value (Point A in Figure 9). The 34653 is in overcurrent mode for 3.0 ms. If after a 3.0 ms filter timer the device is still in overcurrent mode, the device turns off the Power MOSFET and deactivates the power good output signals (Point B in Figure 9). The 34653 then initiates another start-up timer and goes back through the enhancement process. If during the 3.0 ms timer the fault was cleared, then the 34653 goes back to the normal operation mode and the power good output signals stay activated as shown in Figure 10. This way the device overcomes temporary overcurrent situations and at the same time protects the load from a more severe overcurrent situation.

Short Circuit Mode

If the current going through the load becomes >5.0 A, the Power MOSFET is discharged very fast (in less than 10 µs) to try to regulate the current at the I_{LIM} value, and the 34653 is in the overcurrent mode for 3.0 ms. Then it follows the pattern outlined in the Overcurrent Mode paragraph above.

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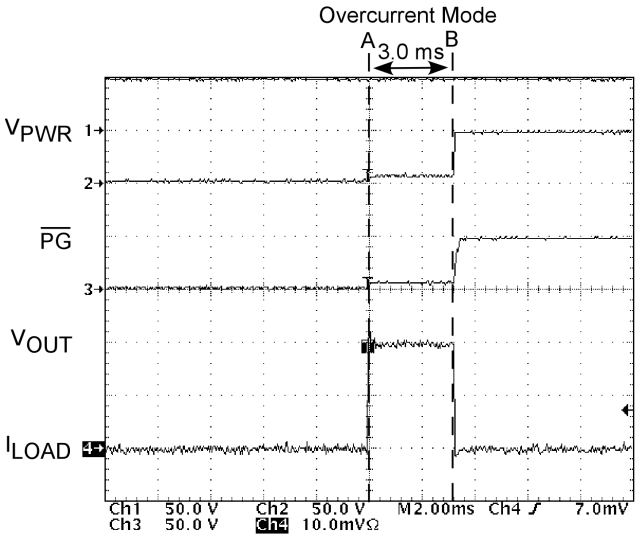

Figure 9. Overcurrent Mode for More Than 3.0 ms

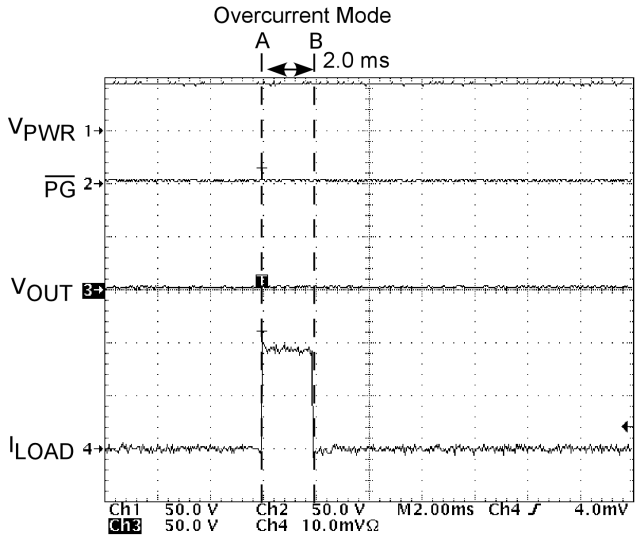

Figure 10. Overcurrent Mode for Less Than 3.0 ms

DISABLING AND ENABLING THE 34653

When a negative voltage (< 1.8 V below V_{PWR}) is applied to the DISABLE pin for more than 1.0 ms (Point A in Figure 11), the 34653 is disabled, the Power MOSFET turns off, and the power good output signals deactivate. The 34653 stays in this state until the voltage on the DISABLE pin is brought to within ±1.2 V of V_{PWR} for more than 1.0 ms to enable the device (Point B in Figure 11). Then a new start-up sequence initiates as described on page 10. Applying a positive voltage (> 1.8 V above V_{PWR}) would also disable the 34653 in the same manner.

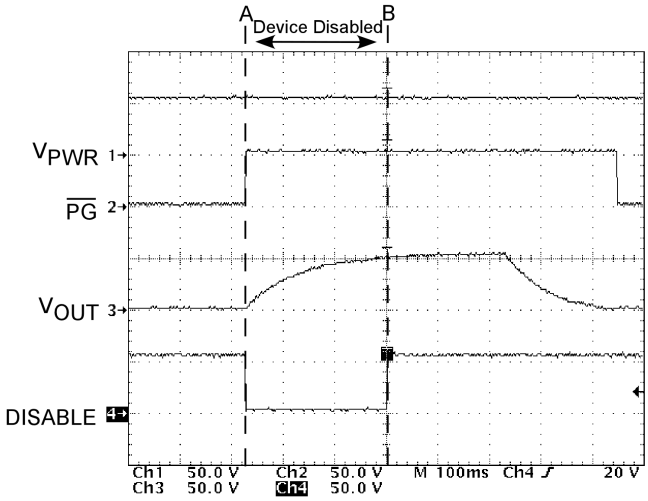

Figure 11. Disabling and Enabling the 34653

Figure 12 demonstrates that the 34653 must be enabled for the length of the start-up timer to start turning on the Power MOSFET. After the fourth disable signal, the 34653 was enabled for the length of the start-up timer. And because the retry counter is less than 10, the 34653 turns on the Power MOSFET and starts the charging process (refer to Charging Process, pages 10–11).

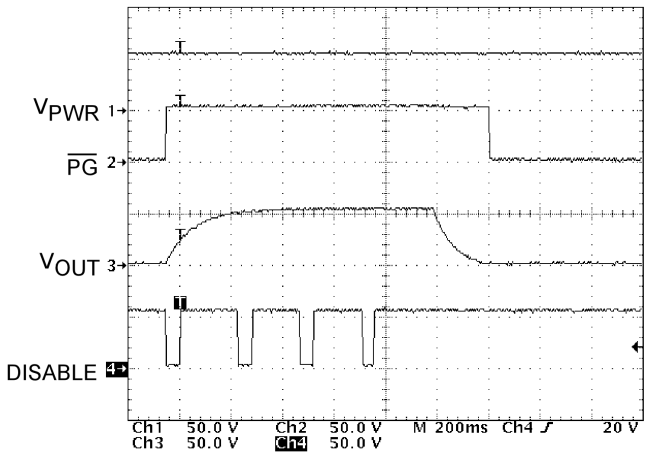

Figure 12. Start-Up Timer Versus Disable

BOARD REMOVAL

When the board is removed, its power ramps down. As soon as the 34653's input voltage reaches the undervoltage turn-off threshold, the undervoltage detection circuit activates and the Power MOSFET turns off for having violated one of the start-up conditions (list on page 10).

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STATE MACHINE

Figure 13 is a representation of the 34653 behavior in different modes of operation.

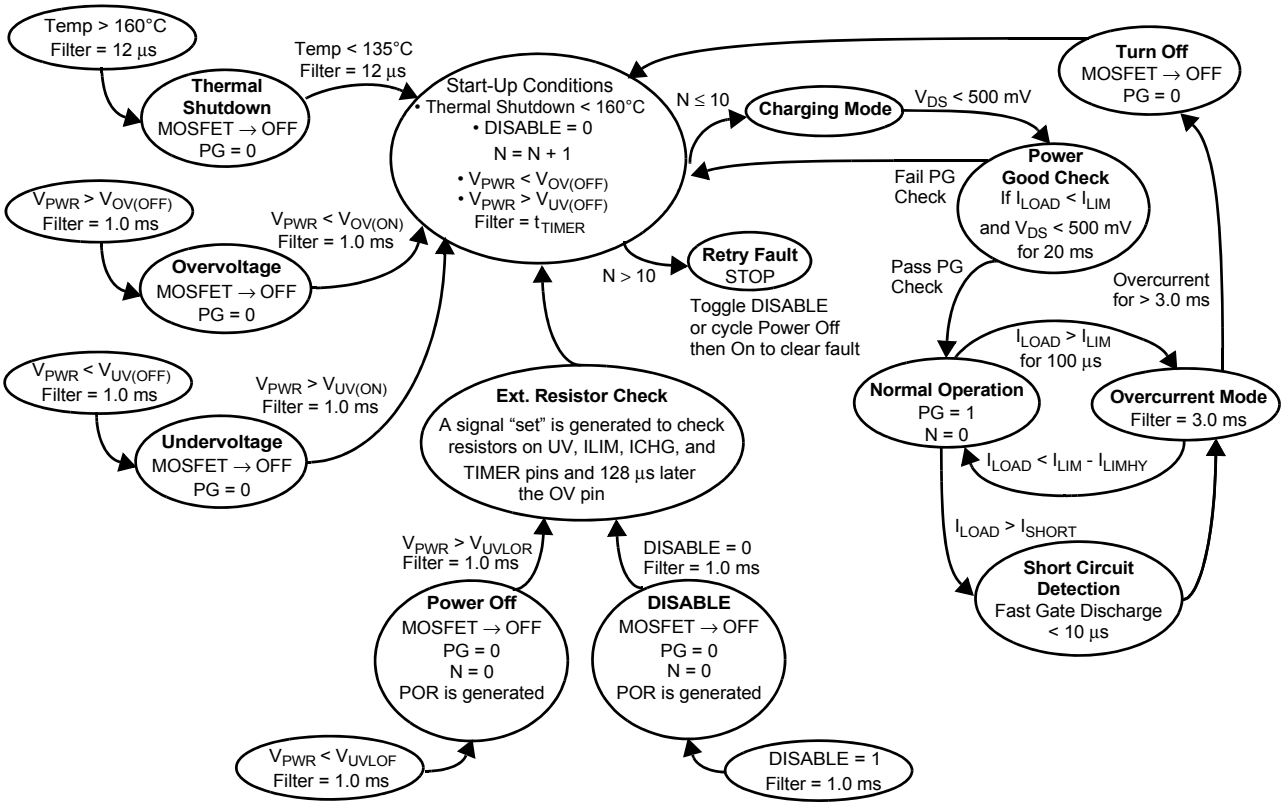

Figure 13. State Diagram

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PROTECTION AND DIAGNOSIS FEATURES

UNDERVOLTAGE

When the input voltage drops below the undervoltage falling threshold for more than 1.0 ms, an undervoltage fault is detected and one of the start-up conditions (list on page 10) is violated. The 34653 turns off the Power MOSFET and deactivates the power good output signals, disabling the load (Point A in Figure 14). The 34653 stays in this state until the input voltage rises above the undervoltage rising threshold for more than 1.0 ms, signaling that the supply voltage is in the normal operation range (Point B in Figure 14). Then a new start-up sequence initiates as described on page 10. The undervoltage detection circuit is also equipped with a 1.0 V hysteresis.

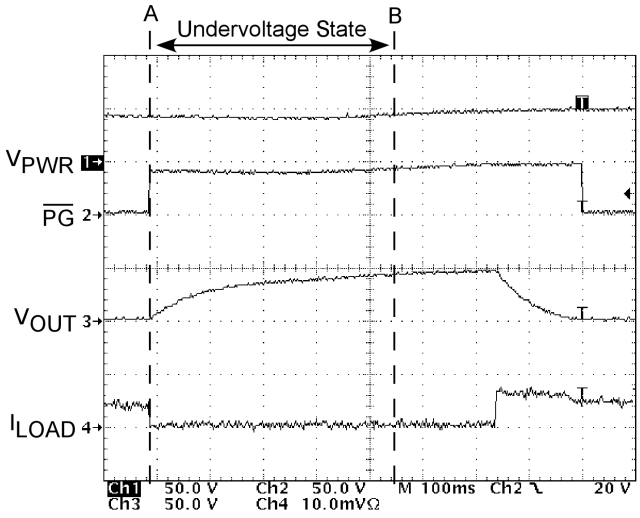

Figure 14. Undervoltage Fault Followed by a New Start-Up Sequence

Figure 15 shows how the 34653 uses the start-up timer to make sure that the input voltage is above the undervoltage falling threshold. The 34653 was in normal operation before Point A. At Point A an undervoltage fault occurs. Then the fault is cleared at Point B, and the 34653 initiates a start-up sequence. Before the end of the start-up timer another undervoltage fault occurs at Point C, so the 34653 does not turn on the Power MOSFET. At Point D the fault is cleared again for the length of the start-up timer and the 34653 turns on the Power MOSFET and starts the charging process (refer to Charging Process, pages 10–11).

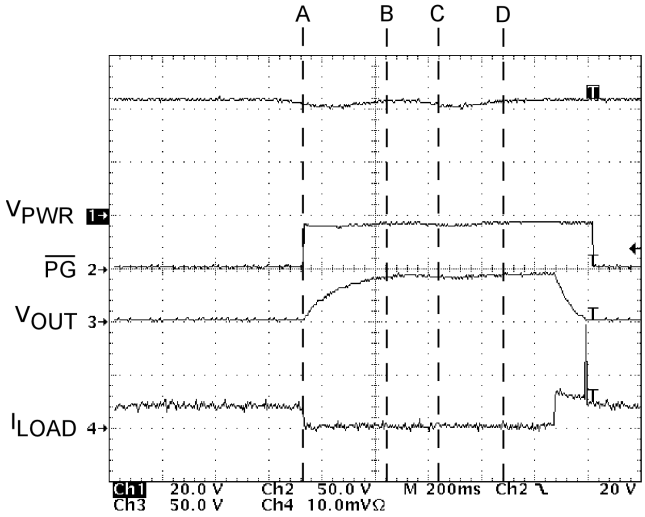

Figure 15. Start-Up Timer Protection Against Undervoltage Faults

OVERVOLTAGE

When the input voltage exceeds the overvoltage rising threshold for more than 1.0 ms, an overvoltage fault is detected and one of the start-up conditions (list on page 10) is violated. The 34653 turns off the Power MOSFET and deactivates the power good output signals, disabling the load. The 34653 stays in this state until the input voltage falls below the overvoltage falling threshold for more than 1.0 ms, signaling that the supply voltage is in the normal operation range. Then a new start-up sequence initiates as described on page 10. The overvoltage detection circuit is also equipped with a 2.0 V hysteresis.

The waveforms for an overvoltage fault are shown in Figure 16.

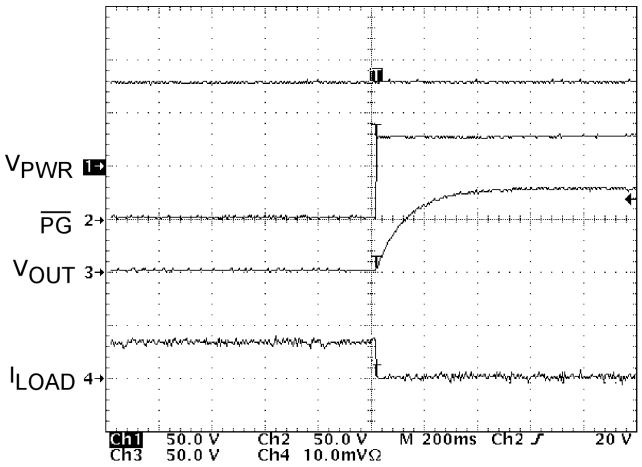

Figure 16. Overvoltage Fault

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THERMAL SHUTDOWN

The thermal shutdown feature helps protect the internal Power MOSFET and circuitry from excessive temperatures. During start-up and thereafter during normal operation, the 34653 monitors the temperature of the internal circuitry for excessive heat. If the temperature of the device exceeds the thermal shutdown temperature of 160°C, one of the start-up conditions (list on page 10) is violated, and the device turns off the Power MOSFET and deactivates the power good output signals. Until the temperature of the device goes below 135°C, a new start-up sequence will not be initiated. This feature is an advantage over solutions with an external Power MOSFET, because it is not easy for a device with an external MOSFET to sense the temperature quickly and accurately. The thermal shutdown circuit is equipped with a 12 µs filter.

Thermal design is critical to proper operation of the 34653. The typical $R_{DS(ON)}$ of the internal Power MOSFET is 0.144 Ω at room ambient temperature and can reach up to 0.251 Ω at high temperatures. The thermal performance of the 34653 can vary depending on many factors, among them:

- The ambient operating temperature (T_A).
- The type of PC board—whether it is single layer or multi-layer, has heat sinks or not, etc.—all of which affects the value of the junction-to-ambient thermal resistance ($R_{\theta JA}$).
- The value of the desired load current (I_{LOAD}).

When choosing an overcurrent limit, certain guidelines need to be followed to make sure that if the load current is running close to the overcurrent limit the 34653 does not go into thermal shutdown. It is good practice to set the parameters so that the resulting maximum junction temperature is below the thermal shutdown temperature by a safe margin.

Equation 1 can be used to calculate the maximum allowable overcurrent limit based on the maximum desired junction temperature or vice versa.

The power dissipation in the device can be calculated as follows:

$$P = I^2_{(LOAD)} * R_{DS(ON)}$$

OR

$$P = [T_J(max) - T_A(max)] / R_{\theta JA}$$

Combining the two equations:

$$I^2_{(LOAD)} = [T_J(max) - T_A(max)] / [R_{\theta JA} * R_{DS(ON)}] \quad \textbf{Eq 1}$$

For example:

$T_A(max) = 55°C$

$R_{\theta JA} = 111$ °C/W for a four-layer board

$R_{DS(ON)} = 0.251$ Ω at high temperatures

Then:

$I^2_{(LOAD)} = [T_J(max) - 55\ °C] / [111\ °C/W * 0.251\ \Omega]$

$I^2_{(LOAD)} = [T_J(max) - 55\ °C] / 27.86\ °C/A^2$

So if the overcurrent limit is 1.0 A, then the maximum junction temperature is 82.86 °C, which is well below the thermal shutdown temperature that is allowed.

The previous explanation applies to steady state power when the device is in normal operation. During the charging process, the power is dominated by the I * V across the Power MOSFET. When charging starts, the power in the Power MOSFET rises up and reaches a maximum value of I * V, then quickly ramps back down to the steady state level in a period governed by the size of the load's input capacitor that is being charged and by the value of the charging current limit I_{CHG}. In this case the instantaneous power dissipation is much higher than the steady state case, but it is on for a very short time.

For example:

$I_{CHG} = 100$ mA, the default value

$C_{LOAD} = 400$ µF, a very large capacitor

$V_{PWR} = 80$ V, worst case

Then:

The power pulse magnitude = $I_{CHG} * V_{PWR} = 8.0$ W

The power pulse duration = $C_{LOAD} * V_{PWR} / I_{CHG} = 320$ ms

Figure 17 displays the temperature profile of the device under the instantaneous power pulse during the charging process. Table 5 depicts thermal resistance values for different board configurations.

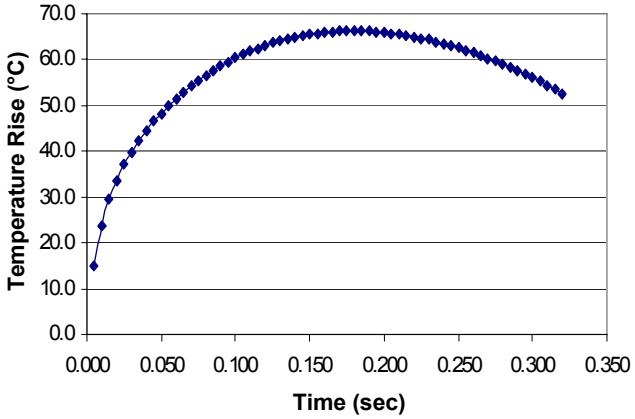

Figure 17. Instantaneous Temperature Rise of an 8.0 W Power Pulse that Decreases Linearly at End of a 320 ms Period

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Table 5. Thermal Resistance Data

Type	Condition	Symbol	Value	Unit
Junction to Ambient	Single-layer board (1s), per JEDEC jesd51-2 with board (JESD51-3) horizontal	$R_{\theta JA}$	167	°C/W
Junction to Ambient	Four-layer board (2s2p), per JEDEC JESD51-2 with board (JESD51-3) horizontal	$R_{\theta JMA}$	115	°C/W
Junction to Ambient	Single-layer board with a 300 mm^2 radiator pad on its top surface, not standard JEDEC	–	145	°C/W
Junction to Ambient	Single-layer board with a 600 mm^2 radiator pad on its top surface, not standard JEDEC	–	143	°C/W
Junction to Ambient	Four-layer board with a via for each thermal lead, not standard JEDEC	–	111	°C/W
Junction to Ambient	Four-layer board with a 300 mm^2 radiator pad on its top surface and a full array of vias between radiator pad and top surface, not standard JEDEC	–	107	°C/W
Junction to Ambient	Four-layer board with a 600 mm^2 radiator pad on its top surface and a full array of vias between radiator pad and top surface, not standard JEDEC	–	107	°C/W
Junction to Board	Thermal resistance between die and board per JEDEC JESD51-8	$R_{\theta JB}$	62	°C/W
Junction to Case	Thermal resistance between die and case top	$R_{\theta JC}$	57	°C/W
Junction to Package Top	Temperature difference between package top and junction per JEDEC JESD51-2	Ψ_{JT}	18	°C/W

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TYPICAL APPLICATIONS

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The 34653 resides on the plug-in board (see Figures 18 and 19), allowing the board to be safely inserted or removed without damaging electrical equipment. The 34653 can be operated with no external components other than the power good output signal pull-up resistor if the default mode was selected for all the programmable features. This is one of the great advantages of the 34653: it operates with minimal user interface and minimal external component count and still offers complete hot swapping functionality with all the necessary protection features, from undervoltage/ overvoltage detection, to current limiting, to short circuit protection and power good output signaling. The default values were chosen to be sufficient for many standard applications.

Figure 18 is a typical application diagram depicting the default mode and using the power good output signal pullup resistor. Refer to the static and dynamic electrical characteristics tables on pages 5 through 7 for the various default values.

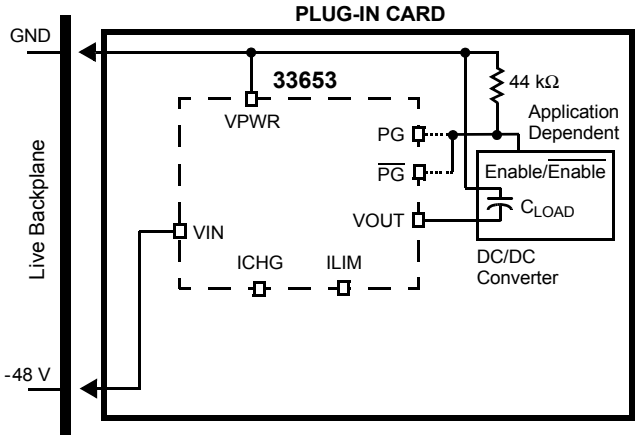

Figure 18. Typical Application Diagram with Default Settings and Minimal External Components

The 34653 can be also programmed for different values of the Overcurrent Limit and the Charging Current Limit using external components connected to the device. Figure 19 shows the 34653 with the required external components that allow access to all programmable features in the device.

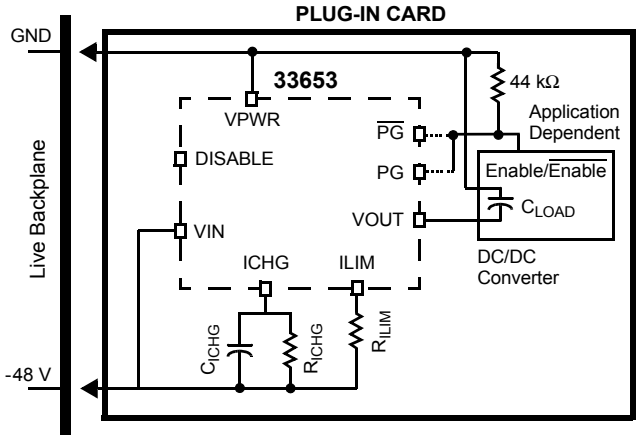

Figure 19. Typical Application Diagram with External Components Necessary to Program the Device

UNDERVOLTAGE AND OVERVOLTAGE DETECTION

The 34653 monitors the input voltage to ensure that it is within the operating range and that there are no overvoltage or undervoltage conditions, and to quickly turn off the Power MOSFET if there are. Internal comparators connected to an internal resistor divider between the VPWR and VIN input pins compare the supply voltages with a reference voltage. The typical default values of 37 V for the UV turn-off threshold (falling threshold) and 78 V for the OV turn-off threshold (rising threshold) will give a typical operating range of 38 V to 76 V. This range is suitable for telecom industry standards.

When the device passes the UVLO threshold, it uses the UV/OV detection circuits to check the input supply levels before turning on the Power MOSFET during the start-up Timer delay and thereafter. As long as the voltage is above the undervoltage falling threshold and below the overvoltage rising threshold, the supply is within operating range and the Power MOSFET is allowed to turn on and stay on. If the input voltage falls below its undervoltage falling threshold or rises above its overvoltage rising threshold, then one of the start-up conditions (list on page 10) is violated and the Power MOSFET turns off, the power good signal deactivates, and a new start-up timer initiates. The undervoltage and overvoltage detection circuits are equipped with a 1.0 ms filter to filter out momentary input supply dips.

TIMER

The Timer function on the 34653 provides the time base used to generate the timing sequences at start-up. The same timer controls the retry delay when the device experiences any fault. The Timer function has a default timer value of

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200 ms. During start-up and if any fault occurred, this timer value is used when initiating a start-up sequence.

POWER GOOD OUTPUT SIGNALS

The power good pins PG and $\overline{PG}$ are output pins that are used to directly enable a power module load. The device has active high and active low power good output signals. Choosing which power good active signal depends on the Enable signal requirement of the load. This feature allows the 34653 to adapt to different applications and a wide variety of loads.

The power good output signal is active if the Power MOSFET is fully enhanced and the device is in normal operation. The signal goes active after a typical 20 ms delay. The signal deactivates if one of the following occurs:

- Power is turned off.
- The device is disabled for more than 1.0 ms.
- The device exceeded its thermal shutdown threshold for more than 12 μs.
- The device is in overvoltage or undervoltage mode for more than 1.0 ms.
- Load current exceeded the overcurrent limit for more than 3.0 ms.

When the power good output signal becomes inactive, it disables the load, protecting it from any faults or damage. These loads are usually DC/DC converters, depicted in Figure 19, page 17. An LED can also be connected to $\overline{PG}$ to indicate that the power is good.

The PG and $\overline{PG}$ pins are referenced to VIN and require a pullup resistor connected to VPWR (Figures 18 and 19, page 17).

DISABLING AND ENABLING THE 34653

The Disable control input (DISABLE) provides two functions:

- External enable/disable control.
- Manual resetting of the device and the retry counter after a fault has occurred.

Using the DISABLE pin, a user can enable/disable the 34653 device, which facilitates easy access to connect the load to or disconnect it from the main power rail.

When power is first applied, the DISABLE pin must be inactive in order for the 34653 to initiate a start-up sequence. If the DISABLE pin is active, the device makes no further steps until the pin is inactive. At any point during the start-up and thereafter during normal operation, if the DISABLE pin is activated, then the retry counter resets, the Power MOSFET turns off and the power good output signals deactivate. The DISABLE circuit is equipped with a 1.0 ms filter to filter out any glitches or transients on the DISABLE input and prevent the Power MOSFET from turning off prematurely.

The DISABLE pin is referenced to VPWR. If left open or connected to VPWR, meaning the voltage at the DISABLE pin is between V_{PWR} + 1.2 V and V_{PWR} - 1.2 V, it is inactive and the device is enabled. If a positive voltage (1.8 V above V_{PWR}) or a negative voltage (1.8 V below V_{PWR}) is applied to DISABLE, it is active and the device is disabled.

CHARGING CURRENT LIMIT

When the device passes the UVLO threshold, it checks if there is any external resistor or external capacitor connected to the ICHG pin. If there is, then it determines the value of the charging current limit value and the charging current limit rise time accordingly. If there is not, it uses the default charging current limit value of 100 mA and rise time of 1.0 ms.

Note Users are allowed to connect an external capacitor to ICHG pin only if an external resistor is also connected. During the external components' check, a capacitor produces an impulse of current and an external resistor will be detected, even it the external resistor is absent.

When the Power MOSFET is turned on, the current limit is set gradually from 0 A to I_{CHG}. This current charges up the load capacitor relatively slowly. When the load capacitor is fully charged, the Power MOSFET reaches its full enhancement, which triggers the current limit to change from I_{CHG} to I_{LIM} and the load current to decrease. The power good output signals activate after a 20 ms delay, which in turn enables the load. The 34653 is now in normal operation mode and the retry counter resets.

The low charging current value of I_{CHG} is intended to limit the temperature increase during the load capacitor charging process, and the gradual rise to I_{CHG} is to prevent transient dips in the input voltage due to sharp increases in the limit current. This prevents the input voltage from drooping due to current steps acting on the input line inductance, and that in turn prevents a premature activation of the UV detection circuit.

Choosing the External Resistor R_{ICHG} Value

The user can change the value of the charging current limit by adding a resistor (R_{ICHG}) between the ICHG and VIN pins, as shown in Figure 19, page 17. The charging current value ranges between 50 mA and 500 mA, with a default value of 100 mA. Table 6 lists examples of R_{ICHG} for different values of I_{CHG} and Figure 20 shows a plot of R_{ICHG} versus I_{CHG}. It is recommended that the closest 1% standard resistor value to the actual value be chosen.

Note Accuracy requirements are application dependent.

To calculate the value of the R_{ICHG} resistor we use the following equations:

$$I_{CHG}(A) = [R_{ICHG}(k\Omega) + 1.4\ k\Omega] / 335$$

$$R_{ICHG}(k\Omega) = 335 * I_{CHG}(A) - 1.4\ k\Omega$$

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Table 6. R_{ICHG} Values for Some Desired I_{CHG} Values

I_{CHG}(A)	R_{ICHG}(kΩ)
0.05	15.35
0.1	32.10
0.15	48.85
0.2	65.60
0.25	82.35
0.3	99.10
0.35	115.85
0.4	135.60
0.45	149.35
0.5	166.10

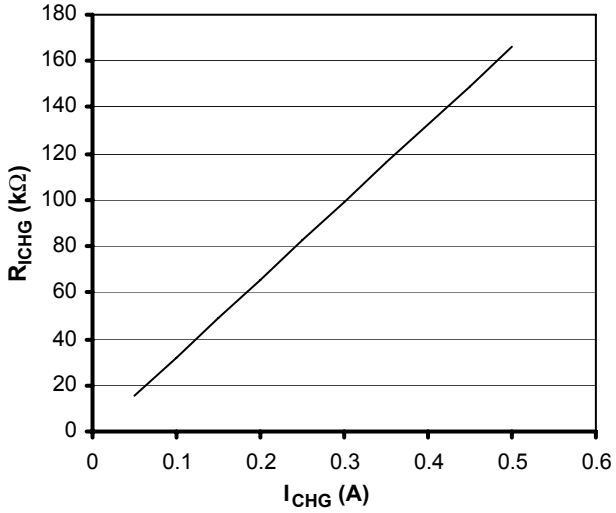

Figure 20. External Resistor (R_{ICHG}) Value Versus Charging Current Limit Value (I_{CHG})

Choosing the External Capacitor C_{ICHG} Value

The user can also change the charging current rise time by adding a capacitor (C_{ICHG}) between the ICHG and VIN pins, as shown in Figure 19, page 17. The charging current rise time ranges between 1.0 ms (default value) and a recommended maximum of 10 ms. Table 7 lists examples of C_{ICHG} for different values of t_{ICHGR} and Figure 21 shows a plot of C_{ICHG} versus t_{ICHGR}.

To calculate the value of the C_{ICHG} capacitor we use the following equation:

$$C_{ICHG}(nF) = 1000 * t_{ICHGR}(ms) / [3 * R_{ICHG}(k\Omega)]$$

Table 7. C_{ICHG} Values for Some Desired t_{ICHGR} Values at a Specific I_{CHG} Value

t_{ICHGR}(ms)	C_{ICHG}(nF) I_{CHG} = 0.05 A	C_{ICHG}(nF) I_{CHG} = 0.1 A	C_{ICHG}(nF) I_{CHG} = 0.5 A
1.0	21.72	10.38	2.01
2.0	43.43	20.77	4.01
3.0	65.15	31.15	6.02
4.0	86.86	41.54	8.03
5.0	108.58	51.92	10.03
6.0	130.29	62.31	12.04
7.0	152.01	72.69	14.05
8.0	173.72	83.07	16.05
9.0	195.44	93.46	18.06
10	217.16	103.84	20.07

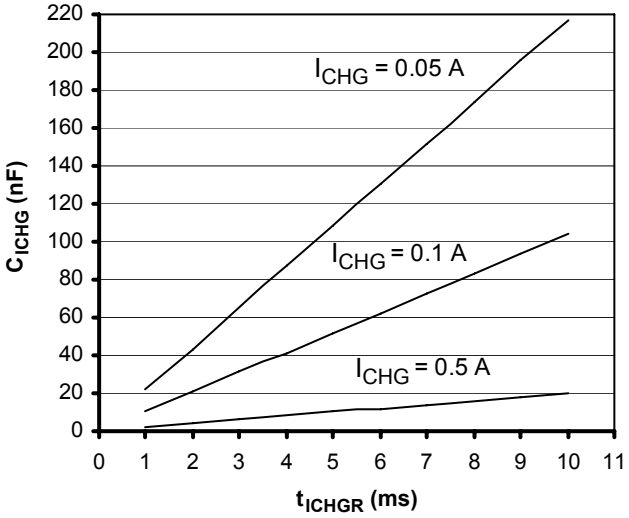

Figure 21. Charging Current External Capacitor (C_{ICHG}) Versus Charging Current Rise Time t_{ICHGR}

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OVERCURRENT LIMIT

When in normal operation mode, the 34653 monitors the load and compares (with a hysteresis) the current going through a Sensor MOSFET with a reference current value generated in reference to the current limit value I_{LIM}. If the current going through the Sensor MOSFET becomes larger than the reference current for more than 100 μs, the overcurrent signal is asserted, the gate of the Power MOSFET is discharged fast (in less than 10 μs) to try to regulate the current, and the 34653 is in overcurrent mode for 3.0 ms. If after a 3.0 ms filter time the device is still in overcurrent mode, the device turns off the Power MOSFET and deactivates the power good output signals. The 34653 then initiates another start-up timer and goes back through the enhancement process. If during the 3.0 ms timer the fault was cleared where the load current was less than I_{LIM} minus the hysteresis value, which is 12% of I_{LIM} value, then the 34653 goes back to the normal operation mode and the power good output signals stay activated. This way the device overcomes temporary overcurrent situations and at the same time protects the load from more severe overcurrent situations.

When the device passes the UVLO threshold, it checks if there is any external resistor connected to the ILIM pin. If there is, it determines the value of the overcurrent limit. If there is not, it uses the default overcurrent limit value of 1.0 A. It then uses the Sensor MOSFET to monitor the load for any overcurrent conditions during operation as explained in the previous paragraph.

Choosing the External Resistor R_{ILIM} Value

The user can change the current limit by adding a resistor (R_{ILIM}) between the ILIM and VIN pins, as shown in Figure 19, page 17. This way the 34653 device is adaptable to different requirements and operating environments. The overcurrent value ranges between 0.15 A and 1.25 A, with a default value of 1.0 A. Table 8 lists examples of R_{ILIM} for different values of I_{LIM} and Figure 22 shows a plot of R_{ILIM} versus I_{LIM}. It is recommended that the closest 1% standard resistor value to the actual value be chosen.

Note Accuracy requirements are application dependent.

To calculate the value of the R_{ILIM} resistor we use the following equations:

$$I_{LIM}(A) = 129 / [R_{ILIM}(k\Omega) + 1.4\ k\Omega]$$

$$R_{ILIM}(k\Omega) = [129 / I_{LIM}(A)] - 1.4\ k\Omega$$

Table 8. R_{ILIM} Values for Some Desired I_{LIM} Values

I_{LIM}(A)	R_{ILIM}(kΩ)
0.15	859.71
0.2	644.43
0.3	429.15
0.4	321.52
0.5	256.93
0.6	213.88
0.7	183.12
0.8	160.06
0.9	142.12
1.0	127.77
1.1	116.02
1.2	106.24
1.25	101.93

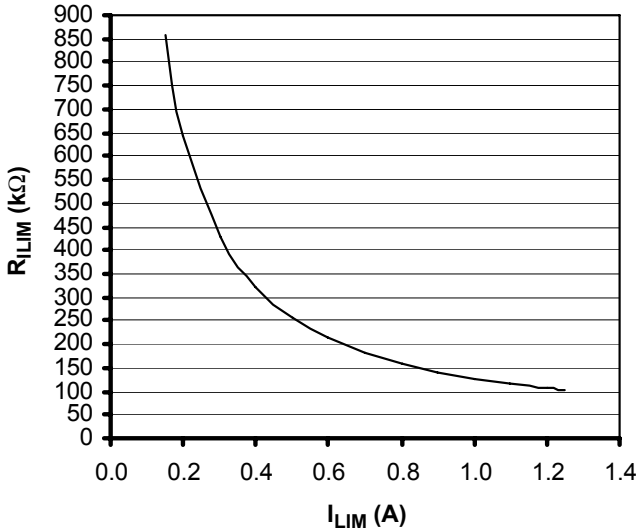

Figure 22. External Resistor (R_{ILIM}) Value Versus Current Limit Value (I_{LIM})

SHORT CIRCUIT DETECTION

If the current going through the load becomes >5.0 A, the Power MOSFET is discharged very fast (in less than 10 μs) to try to regulate the current, and the 34653 is in the overcurrent mode for 3.0 ms. Then it follows the pattern outlined in the Overcurrent Limit paragraph above.

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POWER MOSFET ENERGY CAPABILITY

Figure 23 shows a projected energy capability of the device's internal Power MOSFET under a drain-to-source voltage of 82 V and an ambient temperature of 90°C. It is compared to the energy levels required for the capacitive loads of 100 µF, 200 µF, and 400 µF at 80 V for the discharge periods of 16 ms, 32 ms, and 64 ms, respectively. It is clear that the Power MOSFET well exceeds the required energy capability for all three cases with a sufficient margin. For example, the 400 µF capacitor load with a 64 ms discharge time requires an energy capability of about 1540 mJ, which is well below the Power MOSFET capability of about 3500 mJ. As a result to this analysis the 33652 is expected to exceedingly meet all the energy capability requirements for the possible capacitive loads.

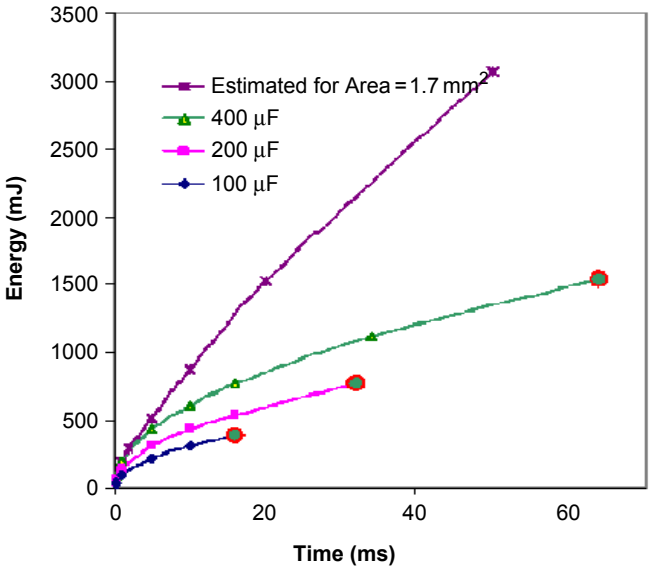

Figure 23. Projected Energy Capability of the Power MOSFET Compared to the Required Energy Levels of Some Capacitive Loads

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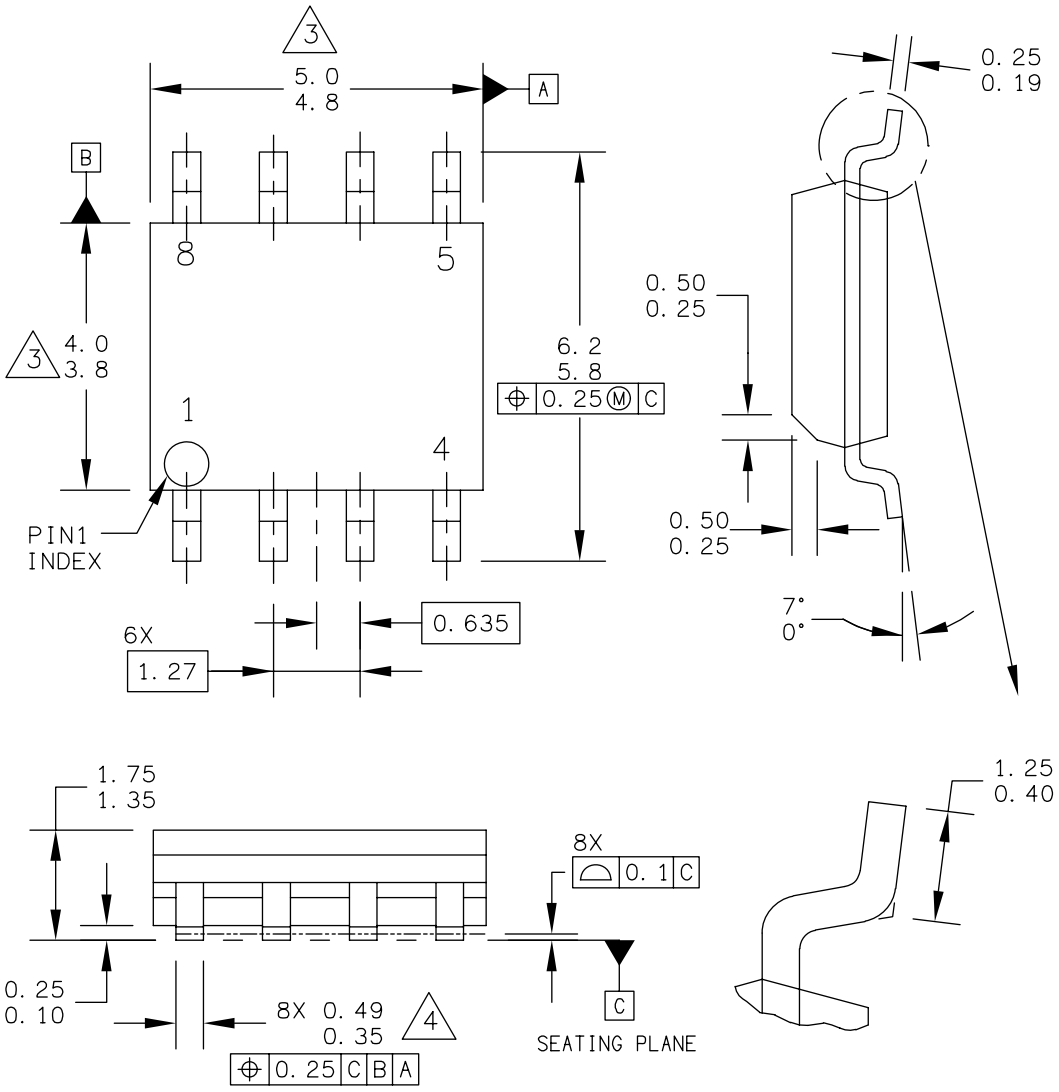
PACKAGING

PACKAGE DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and perform a keyword search on the “98A” drawing number below.



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	CASE NUMBER: 751-07	07 APR 2005
	STANDARD: JEDEC MS-012AA	

EF SUFFIX (Pb-Free)
8-PIN SOIC NARROW BODY
PLASTIC PACKAGE
98ASB42564B
ISSUE U

34653

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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
6.0	2/2006	• Changed Document Order No.
7.0	8/2006	• Corrected PIN CONNECTIONS on page 3 • Updated document to the prevailing Freescale form and style • Updated PACKAGE DIMENSIONS on page 22
8.0	2/2007	• Added Part Number MCZ34653EF/R2 to Ordering Information • Added RoHS logo • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from MAXIMUM RATINGS on page 4. • Added note Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics. on page 4.

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