# Z6132 4K x 8 Quasi-Static RAM

Zilog

## Product Specification

March 1981



**Description**

The Zilog Z6132 is a +5 V intelligent MOS dynamic RAM organized as 4096 words by eight bits. Although it uses single-transistor dynamic storage cells, the Z6132 effectively functions as a static RAM because it performs and controls its own refresh. This eliminates the need for external refresh circuitry and combines the convenience of a static RAM with the high density and low power consumption normally associated with a dynamic RAM.

The Z6132 is particularly suited for microprocessor and minicomputer applications where its byte-wide organization, transparent self-refresh and single supply voltage reduce the parts count and simplify the design.

The Z6132 uses high-performance depletion-load double-poly n-channel silicon-gate MOS technology with a mixture of static and dynamic circuitry that provides a small memory cell, fast access and low power consumption. The Z6132 has separate pins for addresses and bidirectional data I/O to provide maximum flexibility in its application.

The circuit is packaged in an industry-standard 28-pin DIP and pin compatible with the proposed JEDEC standard.

The Z6132 conforms with the Z-Bus specification used by the new generation of Zilog microprocessors, the Z8 and Z8000.

**Features**

- Byte-wide organization: 4096 words by eight bits
- Access and cycle times guaranteed over voltage and temperature range:

| Part Number | Access Time | Cycle Time |
|---|---|---|
| Z6132-3 | 200 ns | 350 ns |
| Z6132-4 | 250 ns | 375 ns |
| Z6132-5 | 300 ns | 425 ns |
| Z6132-6 | 350 ns | 450 ns |

- All inputs and outputs are TTL compatible
- Low power consumption: 250 mW active, 125 mW stand-by.
- Industry-standard 28-pin DIP with JEDEC-recommended pinout
- Automatic self-refresh scheme with slow-and fast-cycle modes.
- On-chip substrate bias generator.
- Interfaces readily to Z8 and Z8000.

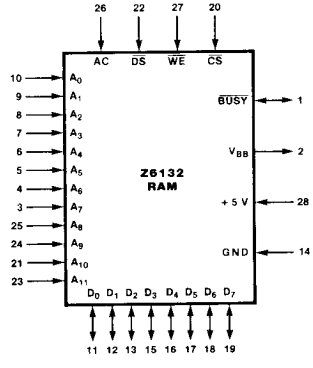


**Figure 1. Logic Symbol**

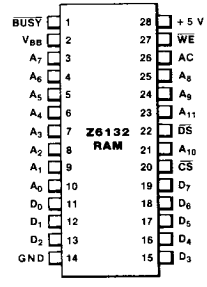


**Figure 2. Pin Assignments**

**Pin Names**

| | |
|---|---|
| $A_0$-$A_{11}$ | Address inputs |
| $D_0$-$D_7$ | Data Inputs/Outputs (3-state) |
| AC | Address Clock input (rising edge) |
| $\overline{DS}$ | Data Strobe input (active Low) |
| $\overline{WE}$ | Write Enable input (active Low) |
| $\overline{CS}$ | Chip Select input (active Low) |
| $\overline{BUSY}$ | Busy output (active Low; open drain) and Refresh Mode Control input |
| $V_{BB}$ | Negative Substrate Bias output |
| $V_{CC}$ | +5 V supply connection |
| $V_{SS}$ | 0 V = Ground connection |

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**Functional Description**

The Z6132 4K x 8 quasi-static RAM is organized as two separate blocks, each having two sets of 64 rows on either side of the 128 sense amplifiers (Figure 3). Both blocks have separate and independent row address buffers and decoders, but they share the column decoder and the internal 8-bit wide data path. The two sets of row address decoders are addressed either by the address inputs $A_1$–$A_7$ or by the internal 7-bit refresh counter. The least significant address input ($A_0$) selects one of the two blocks for external access. While the selected block performs a read or write operation, the other memory block uses the refresh counter address to refresh one row. Details of the self-refresh mechanism are explained later.

A memory cycle starts when the rising edge of Address Clock (AC) clocks in Chip Select ($\overline{CS}$), $A_0$, and Write Enable ($\overline{WE}$). If the chip is not selected ($\overline{CS}$ = High), all other inputs are ignored for the rest of the cycle (that is, until the next rising edge of AC). Both memory blocks are self refreshed by the 7-bit refresh counter. If the chip is selected ($\overline{CS}$ = Low), the 12 address bits and the Write Enable bit are clocked into their registers. $A_0$ determines which block is addressed by $A_1$–$A_{11}$; the other block is refreshed by the 7-bit refresh counter.

The Chip Select and Address inputs must be valid only during a short hold time after the rising edge of AC. This allows address/data multiplexing, because data I/O is controlled by a separate control input Data Strobe ($\overline{DS}$).

**Read Cycle**

A read cycle is initiated by the rising edge of Address Clock (AC) while Chip Select ($\overline{CS}$) is Low and Write Enable ($\overline{WE}$) High. A Low level on the Data Strobe ($\overline{DS}$) input activates the Data outputs after a specified delay from the rising edge of AC as well as the falling edge of $\overline{DS}$, whichever comes later. During a read operation, $\overline{DS}$ is nothing but a static Output Enable signal.

**Write Cycle**

A write cycle is initiated by the rising edge of Address Clock (AC) while Chip Select ($\overline{CS}$) is Low and Write Enable ($\overline{WE}$) is Low.

The $\overline{WE}$ input is checked again at the beginning (falling edge) of Data Strobe ($\overline{DS}$). If $\overline{WE}$ is still Low, this falling edge of $\overline{DS}$ edge-triggers the data on the $D_0$–$D_7$ inputs into the addressed memory location. Data must be valid only during a short hold time after the falling edge of $\overline{DS}$.

**Write Inhibit Cycle**

After a write cycle has been initiated, the actual write operation can still be aborted by pulling $\overline{WE}$ High again before the falling edge of $\overline{DS}$. This write inhibit cycle is a special feature that permits starting a write cycle early at AC time, but still allows the option of inhibiting the write operation later at $\overline{DS}$ time.

**Note:** *Whenever a write cycle has been initiated, it must be accompanied by a High-to-Low transition on the Data Strobe input.*

**Maximum Cycle Time**

The maximum read or write cycle time requirements (15,000 and 800 ns) do not apply to any individual cycle. They are specified to guarantee a complete refresh in a 2 ms period.

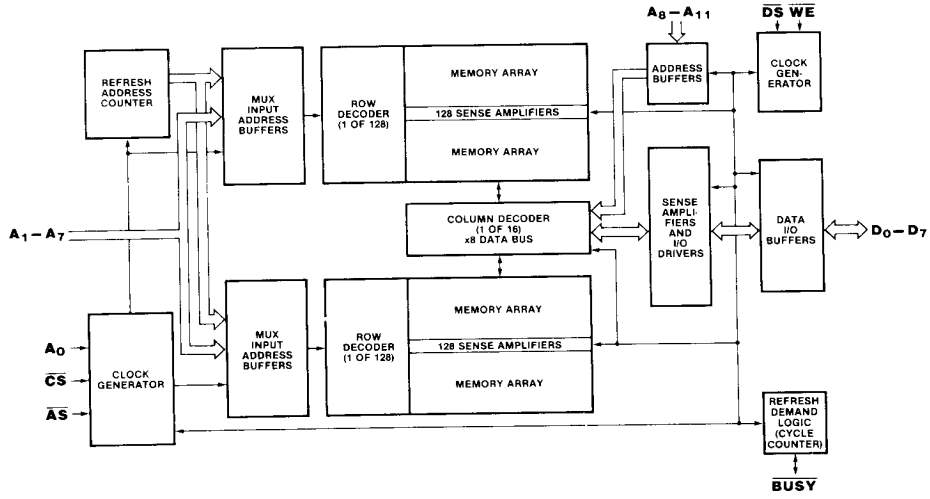



**Figure 3. Z6132 Block Diagram**

**Self-Refresh Operation**

The Z6132 stores data in single-transistor dynamic cells that must be refreshed at least every 2 ms. Each of the two memory blocks contains 16,384 cells and requires 128 refresh cycles to completely refresh the array.

The Z6132 operates in one of two user-selectable self-refresh modes, each satisfying the refresh time requirements. On the basis of the available memory cycle time, the user can decide to use either the Long Cycle-Time Refresh Mode or the Short Cycle-Time Refresh Mode.

**Long Cycle-Time Refresh Mode**

This is the simplest self-refresh mode, and is selected by permanently grounding the $\overline{BUSY}$ output pin. Every memory cycle in this mode consists of a memory operation followed by a refresh operation on both blocks, after which the refresh counter is incremented. Internally, the complete cycle consists of a 4-phase sequence: 1. Memory read, write, or write inhibit. 2. Precharge. 3. Refresh. 4. Precharge. These internal operations are automatic and transparent to the user. When the chip is not selected ($\overline{CS}$ = High when AC goes High), the first two phases are omitted.

There are two important requirements: the memory cycle time must always be longer than the TC (Min) value specified for $\overline{BUSY}$ = Low and there must be at least 128 Address Clocks in any 2 ms period.

The Long Cycle-Time Refresh mode is the one most practical for microprocessor applications, where the cycle time usually exceeds 700 ns.

**Short Cycle-Time Refresh Mode**

This is a more sophisticated self-refresh mode that allows operation at any cycle time down to the specified minimum value.

The user selects this mode by pulling the $\overline{BUSY}$ output pin High through a pull-up resistor (typically 1 kΩ) to $V_{CC}$. The $\overline{BUSY}$ outputs of several Z6132 chips can be or-tied together.

In this mode, the Z6132 always performs a refresh operation on the memory block that is not being addressed from the outside. The refresh counter is incremented whenever it is meaningful, as explained in the following text.

**Deselect Self-Refresh.** If the chip is deselected ($\overline{CS}$ = High when AC goes High), both blocks are refreshed and the refresh counter is incremented after every cycle.

**Odd/Even Self-Refresh.** If the chip is selected ($\overline{CS}$ = Low when AC goes High), the refresh counter refreshes the block that is not addressed by $A_0$. The refresh counter is incremented after an even and an odd address have occured. This self-refresh scheme takes advantage of the inherent sequential nature of most memory addressing.

**Cycle-Count Self-Refresh.** Normally the deselect and odd/even self-refresh schemes step through 128 refresh addresses in less than 2 ms. To guarantee proper refresh operation even in the exceptional case when the memory is continually selected and addressed by a long string of all even or all odd addresses, a built-in cycle counter activates the $\overline{BUSY}$ output and requests one longer memory cycle to append a refresh operation. This internal cycle counter is reset whenever the refresh counter is incremented. The cycle counter then counts memory cycles and activates the $\overline{BUSY}$ output when it reaches a count of 17.

$\overline{BUSY}$ is fed into the $\overline{WAIT}$ input of most microprocessors. $\overline{BUSY}$ is a request to the CPU for a longer memory cycle and is kept Low until the refresh cycle has started. $\overline{BUSY}$ only becomes active when the Z6132 has been selected and addressed with all odd or all even addresses for 17 consecutive Address Strobes.

**Mixed Cycle Time Refresh Mode**

External logic can be used to select between Long and Short Cycle Time Refresh modes by controlling the $\overline{BUSY}$ pin as an input. The Timing Diagram (parameters 25 through 27) shows when the internal logic interrogates the $\overline{BUSY}$ input.

When $\overline{BUSY}$ is Low the cycle must be long, both blocks are refreshed and the refresh counter is incremented every cycle.

When $\overline{BUSY}$ is High, the cycle can be short and the refresh operation is performed as described under Short Cycle Time Refresh Mode.

The external logic must guarantee proper refresh timing. If the Z6132 received a sequence of 17 consecutive all odd or all even addresses while it was continuously selected and $\overline{BUSY}$ was held High, the $\overline{BUSY}$ output will go Low as described before.

A current limiting resistor of ~ 1kΩ should be inserted if the $\overline{BUSY}$ pin is driven by TTL logic.

External logic, as shown in Figure 4 can detect the fact that the memory requires a long cycle time and can pull the CPU $\overline{WAIT}$ input Low.

*Note that the cycle time in most microprocessor applications is so long that the simple Long Cycle Time Refresh Mode is sufficient.*

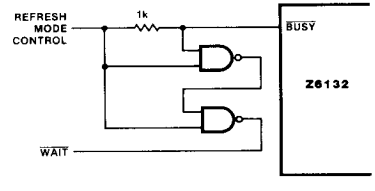
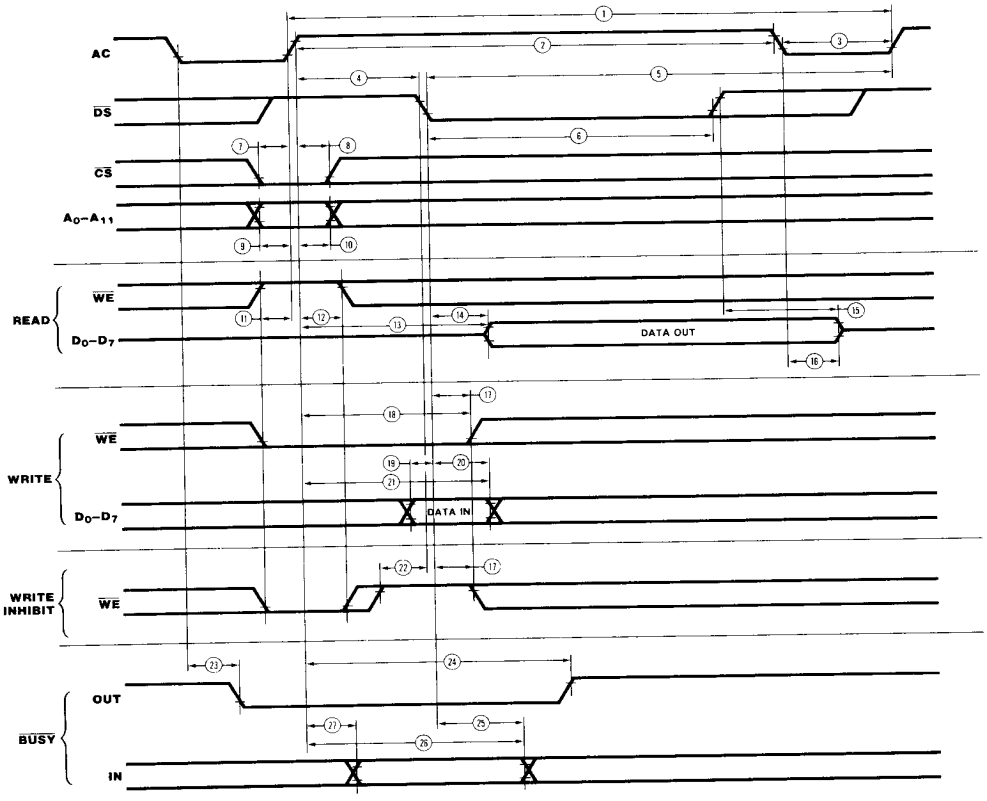



**Figure 4. External $\overline{WAIT}$ Generation**

## AC Electrical Characteristics



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| No. | Symbol | Parameter | Z6132-3[7] Min (ns) | Z6132-3[7] Max (ns) | Z6132-4 Min (ns) | Z6132-4 Max (ns) | Z6132-5 Min (ns) | Z6132-5 Max (ns) | Z6132-6 Min (ns) | Z6132-6 Max (ns) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | TC | Read or Write Cycle Time | 650 | 15000 | 700 | 15000 | 725 | 15000 | 750 | 15000 | 1 |
| | | | 350 | 800 | 375 | 800 | 425 | 800 | 450 | 800 | 2 |
| 2 | TwACh | AC Width (High) | 480 | | 510 | | 550 | | 610 | | 1 |
| | | | 230 | | 260 | | 280 | | 310 | | 2 |
| 3 | TwACl | AC Width (Low) | 40 | | 50 | | 60 | | 60 | | |
| 4 | TdAC(DS) | AC ↑ to $\overline{DS}$ ↓ | 10 | | 10 | | 10 | | 10 | | |
| 5 | TdDS(AC) | $\overline{DS}$ ↓ to AC ↑ | 550 | | 580 | | 610 | | 640 | | 1 |
| | | | 250 | | 275 | | 310 | | 340 | | 2 |
| 6 | TwDS | $\overline{DS}$ Width (Low) | 120 | | 140 | | 160 | | 180 | | |
| 7 | TsCS(AC) | $\overline{CS}$ Setup Time to AC ↑ | 0 | | 0 | | 0 | | 0 | | |
| 8 | ThCS(AS) | $\overline{CS}$ Hold Time to AC ↑ | 40 | | 45 | | 50 | | 55 | | |
| 9 | TsA(AC) | Address Setup Time to AC ↑ | 0 | | 0 | | 0 | | 0 | | |
| 10 | ThA(AC) | Address Hold Time to AC ↑ | 40 | | 45 | | 50 | | 55 | | |
| 11 | TsW(AC) | $\overline{WE}$ Setup Time to AC ↑ | -10 | | -15 | | -20 | | -25 | | |
| 12 | ThW(AC) | $\overline{WE}$ Hold Time to AC ↑ | 60 | | 70 | | 80 | | 80 | | |
| 13 | TdAC(DO) | AC ↑ to Data Out | | 200 | | 250 | | 300 | | 350 | 3 |
| 14 | TdDS(DO) | $\overline{DS}$ ↓ to Data Out | | 70 | | 80 | | 90 | | 100 | 3 |
| 15 | TdDS(DOz) | $\overline{DS}$ ↑ to Data Out Float | 30 | 70 | 35 | 80 | 40 | 90 | 45 | 100 | 4 |
| 16 | TdAC(DOz) | AC ↓ to Data Out Float | 30 | 70 | 35 | 80 | 40 | 90 | 45 | 100 | 4 |
| 17 | ThW(DS) | $\overline{WE}$ Hold Time to $\overline{DS}$ ↓ | 60 | | 70 | | 80 | | 90 | | 3 |
| 18 | TsW(AC) | $\overline{WE}$ Hold Time to AC ↑ | 120 | | 130 | | 140 | | 150 | | 3 |
| 19 | TsDI(DS) | Data In Setup Time to $\overline{DS}$ ↓ | 0 | | 0 | | 0 | | 0 | | |
| 20 | ThDI(AC) | Data In Hold Time to $\overline{DS}$ ↓ | 45 | | 50 | | 60 | | 70 | | 3 |
| 21 | ThDI(AC) | Data In Hold Time to AC ↑ | 120 | | 130 | | 140 | | 150 | | 3 |
| 22 | TsWh(DS) | $\overline{WE}$ High Setup Time to $\overline{DS}$ ↓ | 10 | | 10 | | 10 | | 10 | | |
| 23 | TdAC(Bl) | AC ↓ to $\overline{BUSY}$ Out ↓ | | 80 | | 90 | | 100 | | 110 | |
| 24 | TdAC(Bh) | AC ↑ to $\overline{BUSY}$ Out ↑ | | 400 | | 450 | | 500 | | 550 | 5 |
| | | | | 80 | | 90 | | 100 | | 110 | 6 |
| 25 | ThB(DS) | $\overline{BUSY}$ In Hold Time to $\overline{DS}$ ↓ | 70 | | 80 | | 90 | | 100 | | 3 |
| 26 | ThB(AC) | $\overline{BUSY}$ In Hold Time to AC ↑ | 150 | | 160 | | 170 | | 180 | | 3 |
| 27 | TsB(AC) | $\overline{BUSY}$ In Setup Time to AC ↑ | -40 | | -50 | | -60 | | -70 | | |

NOTES:
1. $\overline{BUSY}$ = Low.
2. $\overline{BUSY}$ = High.
3. Whichever is later.
4. Whichever is earlier.
5. Selected.
6. Deselected.
7. Available second half of 1981.



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**Substrate Bias Generator**

The Z6132 contains an on-chip negative substrate-bias generator, which is a simple dc-to-dc converter that generates a substrate-bias voltage of –2.5 to –3 V. This reduces parasitic junction capacitances and thus increases circuit speed. The substrate bias output $V_{BB}$ should be decoupled externally with an $\approx 0.1\ \mu F$ ceramic capacitor to $V_{SS}$ (ground).

**Power-Up**

After applying $V_{CC}$, it is necessary to wait 20 ms to charge the substrate bias decoupling capacitor. Moreover, the 6132 requires sixteen selected or deselected memory cycles before proper operation is attained.

**Absolute Maximum Ratings**

Voltages on all pins (except $V_{BB}$) with respect to GND . . . . . –0.5 V to +7.0 V

Operating Ambient Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Standard Test Conditions**

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the refer-ence pin. Standard conditions are as follows:

- $+4.75\ V \leq V_{CC} \leq +5.25\ V$
- $V_{SS} = GND = 0\ V$
- $0°C \leq T_A \leq +70°C$

**DC Electrical Characteristics**

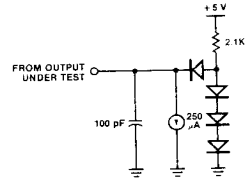
| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.2 | 7.0 | V | |
| $V_{IL}$ | Input Low Voltage | –0.5 | 0.8 | V | |
| $V_{OH}$ | Output High Voltage | 2.4 | | V | $I_{OH} = 250\ \mu A$ (except $\overline{BUSY}$) |
| $V_{OL}$ | Output Low Voltage | | 0.4 | V | $I_{OL} = +3.5$ mA for $D_0$-$D_7$ |
| | | | 0.4 | V | $I_{OL} = +5$ mA for $\overline{BUSY}$ |
| $I_{IL}$ | Input Leakage | | ±10 | μA | $0.4 \leq V_{IN} \leq +2.4\ V$ |
| $I_{OL}$ | Output Leakage | | ±10 | μA | $0.4 \leq V_{OUT} \leq +2.4\ V$ |
| $I_{CC}$ | $V_{CC}$ Supply Current | | 30 | mA | Standby, AC = Static |
| | | | 45 | mA | Fast Cycle Operation, TC = 400 ns |

**Capacitance**

Capacitance of input or output pins, except $\overline{BUSY}$: 5 pF (max)

Capacitance of $\overline{BUSY}$ input/output: 10 pF (max)

All ac parameters assume a load capacitance of 100 pF maximum.



**Interfacing the Z6132 to a Z8000**

The Z8001 or Z8002 CPU addresses memory as bytes, but can access either 8-bit bytes or 16-bit words. When writing a byte, $A_0$ selects the byte within a word; in all other cases the Z8000 always accesses a word, and $A_0$ is ignored. (When reading a byte, the memory reads a word and the CPU selects the appropriate byte internally.)

The odd- and even-byte memory banks use separate Chip Select decoders. The LS157 multiplexer is used as a function generator and activates either the odd bank, the even bank or both, as determined by $A_0$, Read/Write (R/$\overline{W}$) and Byte/Word (B/$\overline{W}$).

Address labels $A_0$-$A_{11}$ and Data labels $D_0$-$D_7$ are used only to illustrate this example. Obviously, all address pins as well as all Data pins can be arranged arbitrarily to accommodate the PC board layout. $A_0$ must, however, always be connected to $AD_1$ to enhance the self-refresh operation.

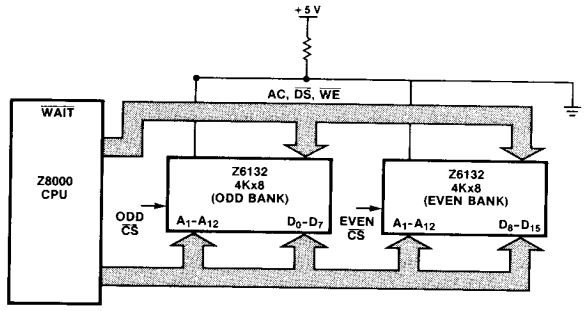



**Figure 5. Block Diagram**

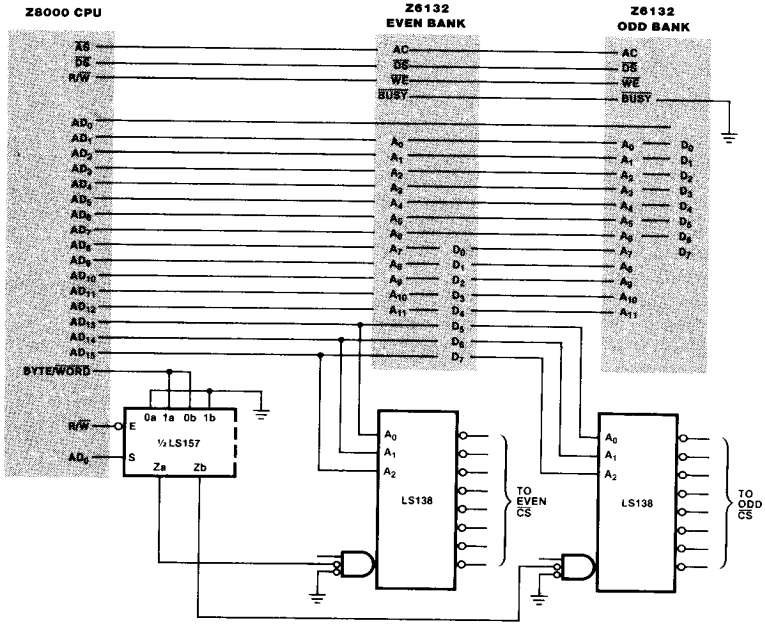



**Figure 6. Connection Diagram**

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## Interfacing the Z6132 to a Z-80

When interfacing the Z80 CPU to the Z6132, the complexity of the required logic depends somewhat on the speed at which the CPU is operating and the speed selection of the Z6132. For the interface example shown, the assumptions are that the Z80 CPU is operating at 4 MHz and the Z6132 has a 300 ns access time (i.e., a Z6132-5). Note that the Z6132 is used in the Short Cycle Time Refresh mode.

The $\overline{MREQ}$ and $\overline{M1}$ lines from the Z80 CPU are used to generate the Address Clock (AC) to the Z6132. The $\overline{M1}$ line is latched with the Z80 CPU Clock (CLK) so that the memory transaction is started as early as possible during opcode fetch cycles. This is done to provide the required access time for the Z6132 during Z80 opcode fetch cycles, which are one-half clock cycle shorter than data memory cycles.

The D-type flip-flop is used to "remove" the short cycle from the $\overline{MREQ}$ signal during Z80 CPU-initiated memory refresh cycles. If this were not done, an AC pulse would be generated that would not meet the AC width specification of the Z6132-5.

Memory select can be accomplished with a single address line (A12). If more than one Z6132 is used in a system, an address decoder (such as the 74LS138 shown) can be used to drive the $\overline{CS}$ line on the Z6132. The $\overline{CS}$ line is sampled with the Low-to-High transition of AC, so there will not be a problem with erroneous chip selects in the absence of a valid AC strobe.

During the write cycles, the $\overline{WE}$ line is sampled by the $\overline{DS}$ line. During the read cycles, the Low-to-High transition of AC is the critical sample time for the $\overline{WE}$ line, and $\overline{DS}$ becomes an output enable control. Therefore, $\overline{RD}$ and $\overline{WR}$ from the Z80 are OR'ed to generate $\overline{DS}$ to the Z6132, and $\overline{RD}$ and $\overline{M1}$ are OR'ed to generate $\overline{WE}$.

Normally, $\overline{WE}$ can be driven through an inverter by $\overline{RD}$ only. Due to the shortened Z80 cycle, however, AC is generated as early as possible during opcode fetches. Consequently, $\overline{WE}$ must be generated early by OR'ing $\overline{RD}$ and $\overline{M1}$.

The logic shown allows the Z6132 to be used for program or data memory and to work with 4 MHz clocks. Since all internal timing, including refresh, is derived from the rising edge of AC, it is necessary that AC be supplied at all times. The CPU does not have to access the Z6132 in order to do this because any $\overline{MREQ}$ signal will activate AC. In the unlikely event that only even or only odd addresses are presented to the Z6132 for more than 17 AC strobes, the Z6132 will do an internal refresh on the next AC. If the CPU tries to access the Z6132 during this time, the CPU is placed in the Wait mode. The BUSY line on the Z6132 is activated until the internal refresh operation is completed.

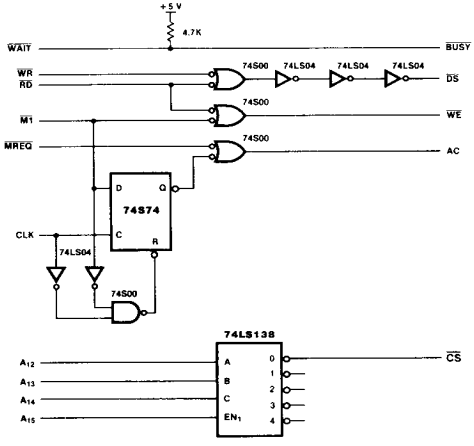


**Figure 7. Z-80 Connection Diagram**

## Interfacing the Z6132 to a Z8

The Z6132 interfaces directly with the single chip Z8 microcomputer. Port 1 provides the 8-bit multiplexed Address/Data bus, and the more significant address bits are provided by Port 0.

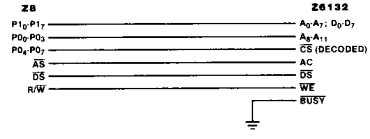


**Figure 8. Z8 Connection Diagram**

## Ordering Information

| Product Number | Package/ Temp | Speed | Description | Product Number | Package/ Temp | Speed | Description |
|---|---|---|---|---|---|---|---|
| Z6132-3 | CS,PS,DS | 200 ns | Z6132-3 4096x8-Bit Quasi-Static RAM | Z6132-5 | CS,PS,DS | 300 ns | Z6132-5 4096x8-Bit Quasi-Static RAM |
| Z6132-4 | CS,PS,DS | 250 ns | Z6132-4 4096x8-Bit Quasi-Static RAM | Z6132-6 | CS,PS,DS | 350 ns | Z6132-6 4096x8-Bit Quasi-Static RAM |

NOTES: C = Ceramic, D = Cerdip, P = Plastic; S = 0°C to +70°C.



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