



Evaluation Board for the AD7400A and AD7401A

EVAL-AD7400A/AD7401A

FEATURES

Full-featured evaluation board for the AD7400A and AD7401A
EVAL-CED1Z compatible
Standalone capability
On-board analog buffering
Various linking options
PC software for control and data analysis when using the
EVAL-CED1Z

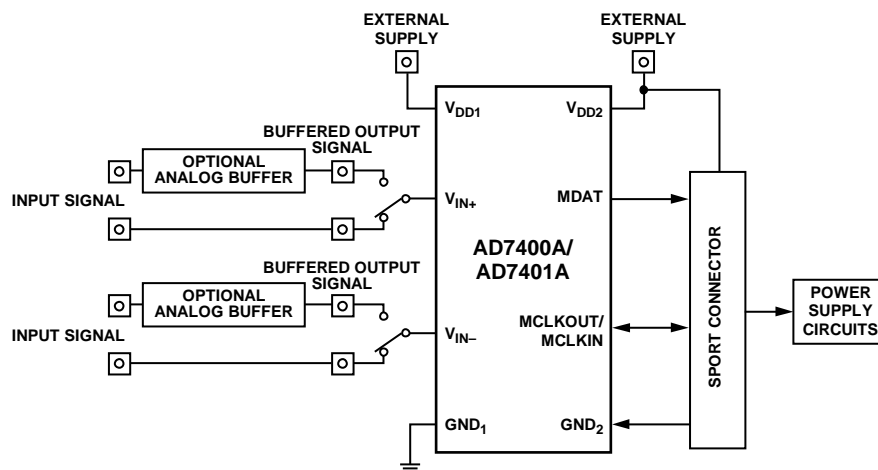
GENERAL DESCRIPTION

This data sheet describes the evaluation board for the [AD7400A](#) and [AD7401A](#). The AD7400A and AD7401A are second-order, sigma-delta ($\Sigma\Delta$) modulators that convert an analog input signal into a high speed, 1-bit data stream with on-chip digital isolation based on the Analog Devices Inc., *iCoupler*® technology. The AD7400A and AD7401A operate from a 5 V power supply and accept a differential input signal of ± 200 mV (± 320 mV

full scale). The analog input is continuously sampled by the analog modulator, eliminating the need for external sample-and-hold circuitry. The input information is contained in the output stream as a density of ones with a data rate of 10 MHz. The original information can be reconstructed with an appropriate digital filter. The serial I/O can use a 5 V or a 3 V supply (V_{DD2}). Full details on the AD7400A and AD7401A are available in the AD7400A and AD7401A data sheets, which are available from Analog Devices and should be consulted in conjunction with this data sheet when using the evaluation board.

On-board components include two [AD797](#) analog op amps for buffering the differential analog input to the AD7400A and AD7401A. Various link options are explained in the Link Options section. Interface to this board using a standard 2-row 34-pin SPORT connector. This SPORT connector is compatible with the EVAL-CED1Z, which is available from Analog Devices. External sockets are also provided for signals.

FUNCTIONAL BLOCK DIAGRAM



Rev. 0

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Fax: 781.461.3113
www.analog.com
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REVISION HISTORY

11/08—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

When using this evaluation board with the EVAL-CED1Z, the V_{DD1} and V_{DD2} supplies (that is, the isolated and nonisolated supplies) must be provided by an external source via the J1 and J4 connectors, respectively. The isolated supply, V_{DD1} , can be supplied with a voltage from 4.5 V to 5.25 V while V_{DD2} must be supplied with a 3.3 V supply when used in conjunction with the EVAL-CED1Z. This is because the EVAL-CED1Z operates with a 3.3 V logic level. When using the board as a standalone unit, external supplies must be provided for V_{DD1} , V_{DD2} , and the op amp supplies. This evaluation board has the following power supply inputs: V_{DD1} (+5 V), V_{DD2} (+3 V to +5 V), (–5 V), AGND, and DGND. The (–5 V) supply is only required if the external [AD797](#) op amps are used to buffer the analog inputs to the [AD7400A](#) or [AD7401A](#).

The supplies are decoupled to the relevant ground plane with 10 μ F tantalum and 0.1 μ F multilayer ceramic capacitors at the point where they enter the board.

The EVAL-AD7400A/AD7401A has split ground planes, that is, both the isolated and nonisolated side of the device have completely separate ground planes to preserve the isolation. The board is split beneath the AD7400A or AD7401A package so that signals on one side of the AD7400A or AD7401A are completely isolated from signals on the other side. The EVAL-AD7400A boards contains the AD7400A in the 8-lead surface mount PDIP packages with gull wing leads, and the EVAL-AD7401A board contains the AD7401A in a 16-lead SOIC package.

LINK OPTIONS

There are seven link options and two solder links that must be set correctly to select the appropriate operating setup before using the evaluation board. The functions of the options are outlined in Table 1.

Table 1. Link Option Functions

Link No.	Function
J7	<p>This link selects the destination for the MCLKOUT output on the AD7400A and the source of the MCLKIN input on the AD7401A.</p> <p>In Position A, the MCLKOUT signal on the AD7400A goes to the SPORT connector on the EVAL-CED1Z board. The MCLKIN signal on the AD7401A is supplied via the SPORT connector by the EVAL-CED1Z board.</p> <p>In Position B, the MCLKOUT signal on the AD7400A goes to the J5 SMB socket. The MCLKIN input on the AD7401A must be supplied by an external source via the J5 SMB socket.</p>
J8	<p>This link option selects the destination of the MDAT output signal from the AD7400A or AD7401A.</p> <p>In Position A, the MDAT signal goes to the SPORT connector on the EVAL-CED1Z board.</p> <p>In Position B, the MDAT signal goes to the J6 SMB socket.</p>
J9	<p>This link option selects the source of the V_{DD2} supply (the nonisolated supply) for the AD7400A or AD7401A.</p> <p>In Position A, V_{DD2} must be supplied from an external source via the J4-1 connector.</p> <p>In Position B, the V_{DD2} input on the AD7400A or AD7401A is connected to the 5 V supply from the EVAL-CED1Z. This connection should not be used because the EVAL-CED1Z operates with a 3.3 V logic level and therefore V_{DD2} should be supplied by 3.3 V from an external source.</p> <p>In Position C, the V_{DD2} input on the AD7400A or AD7401A is connected to the 2.5 V supply from the EVAL-CED1Z. This connection should not be used because the EVAL-CED1Z operates with a 3.3 V logic level and therefore V_{DD2} should be supplied by 3.3 V from an external source.</p>
J10	<p>This link option selects the source of the V_{IN+} analog input to the AD7400A or AD7401A.</p> <p>In Position A, the V_{IN+} analog input to the AD7400A or AD7401A is buffered by the AD797 (U2). This link option should be used in conjunction with J11, which should be placed in Position A.</p> <p>In Position B, the V_{IN+} analog input to the AD7400A or AD7401A is not buffered by the AD797 (U2). This link option should be used in conjunction with J11, which should be placed in Position B.</p> <p>In Position C, the V_{IN+} analog input to the AD7400A or AD7401A is tied directly to GND₁.</p>
J11	<p>This link selects the AD797 (U2) to buffer the analog input from J2 SMB.</p> <p>In Position A, the analog input signal supplied to the J2 SMB connector is fed directly to the AD797 for buffering. This link option should be used in conjunction with J10, which should be placed in Position A.</p> <p>In Position B, the analog input signal supplied to the J2 SMB connector is fed directly to the V_{IN+} input of the AD7400A or AD7401A, therefore it is not buffered. This link option should be used in conjunction with J10, which should be placed in Position B.</p>

EVAL-AD7400A/AD7401A

Link No.	Function
J13	This link selects the AD797 (U3) to buffer the analog input from the J3 SMB. In Position A, the analog input signal supplied to the J3 SMB connector is fed directly to the AD797 (U3) for buffering. This link option should be used in conjunction with J14, which should be placed in Position A. In Position B, the analog input signal supplied to the J3 SMB connector is fed directly to the V_{IN+} input of the AD7400A and AD7401A, therefore it is not buffered. This link option should be used in conjunction with J14, which should be placed in Position B.
J14	This link option selects the source of the V_{IN-} analog input to the AD7400A or AD7401A. In Position A, the V_{IN-} analog input to the AD7400A or AD7401A is buffered by the AD797 (U3). This link option should be used in conjunction with J13, which should be placed in Position A. In Position B, the V_{IN-} analog input to the AD7400A or AD7401A is not buffered by the AD797 (U3). This link option should be used in conjunction with J13, which should be placed in Position B. In Position C, the V_{IN-} analog input to the AD7400A or AD7401A is tied directly to GND_1 .
MCLKOUT/MCLKIN	This is a solder link that selects the destination of MCLKOUT for the AD7400A and the source of MCLKIN for the AD7401A. In Position A, the MCLKOUT/MCLKIN pin of the AD7400A or AD7401A is tied directly to GND_2 . In Position B, the MCLKOUT/MCLKIN pin of the AD7400A or AD7401A is connected directly to J7, that is, the signal is received/supplied by either the EVAL-CED1Z or an external source via the J5 SMB socket.
MDAT	This is a solder link that selects the destination of the MDAT for the AD7400A or AD7401A. In Position A, the MDAT pin of the AD7400A or AD7401A is tied directly to GND_2 . In Position B, the MDAT pin of the AD7400A or AD7401A is connected directly to J8, that is, the signal is received by either the EVAL-CED1Z or an external source via the J6 SMB socket.

Table 2. Link Positions on the Packaged EVAL-AD7400A/AD7401A

Link No.	Position	Function
J7	A	The MCLKOUT signal from the AD7400A is supplied to the EVAL-CED1Z. The MCLKIN signal from the AD7401A is supplied by the EVAL-CED1Z.
J8	A	The MDAT signal from the AD7400A or AD7401A is supplied directly to the EVAL-CED1Z.
J9	A	The V_{DD2} supply (the nonisolated supply) for the AD7400A or AD7401A is supplied by a 3.3 V supply from an external source via the J4 connector.
J10	B	The V_{IN+} analog input to the AD7400A or AD7401A is not buffered by the AD797 (U2). This link option should be used in conjunction with J11, which should be placed in Position B.
J11	B	The analog input signal supplied to the J2 SMB is fed directly to the V_{IN+} input of the AD7400A or AD7401A, thus it is not buffered. This link option should be used in conjunction with J10, which should be placed in Position B.
J13	B	The analog input signal supplied to the J3 SMB is fed directly to the V_{IN-} input of the AD7400A or AD7401A, thus it is not buffered.
J14	C	The V_{IN-} analog input to the AD7400A or AD7401A is tied directly to AGND.
MCLKOUT/MCLKIN	B	The MCLKOUT/MCLKIN pin of the AD7400A or AD7401A is connected directly to J7.
MDAT	B	The MDAT pin of the AD7400A or AD7401A is connected directly to J8.

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board. It is necessary to ensure that all links are positioned correctly for the chosen operating mode. There are two different modes in which to operate the evaluation board: operate the board with the EVAL-CED1Z or use the board as a standalone board.

Table 2 shows the position in which all the links are set when the evaluation board is packaged. When the board is shipped, it is assumed that the user will be operating with the EVAL-CED1Z board. The links are set so that the control signals are supplied by the EVAL-CED1Z. The V_{DD1} supply, which is the

supply for the isolated side of the device, must be supplied by an external source via the J1-1 connector. The V_{DD2} supply, which is the supply for the nonisolated side of the device, must be supplied by 3.3 V from an external source via the J4 connector. The board is configured to enable the user to supply a single-ended input signal to the V_{IN+} terminal of the ADC while the V_{IN-} terminal of the ADC is connected to GND. The J10, J11, J13, and J14 links can be modified to enable a differential signal to be applied to the AD7400A or AD7401A inputs if required. The EVAL-AD7400A/AD7401A is configured to accept analog input signals directly from the user's source. Alternatively, the AD797 op amps (U2, U3) can be used to buffer the analog input signals if required.

INTERFACING THE EVALUATION BOARD TO THE EVAL-CED1Z

Interface the EVAL-CED1Z board to the evaluation board via a SPORT connector, J12. This standard 2-row, 0.1" connector is used to connect the EVAL-AD7400A/AD7401A board to the

EVAL-CED1Z controller board. Table 3 gives a description of the pins and the pin designations on the SPORT connector used to interface between the EVAL-CED1Z board and the EVAL-AD7400A/AD7401A.

Table 3. SPORT Connector Pin Functions

Pin	Connection	Description
1	+5VD_Edge	5 V digital supply.
2	+7V	7 V analog supply.
3	DGND	Digital ground. These lines are connected to the digital ground plane on the evaluation board.
4	NC	No connect. Do not use this pin.
5	$\overline{\text{RESET}}$	Reset.
6	SPORT_TSCLK0/SPI_SEL5	SPORT 0 transmit serial clock. SPI Peripheral Chip Select 5.
7	SPORT_RFS0/SPI_SEL3	SPORT 0 receive frame sync. SPI Peripheral Chip Select 3.
8	SPORT_DROPRI/SPI_SEL4	SPORT 0 Data Receive Primary. SPI Peripheral Chip Select 4. This input is connected to the MDAT pin of the AD7400A or AD7401A.
9	DGND	Digital ground.
10	SPORT_DR0SEC	Sport 0 data receive secondary; parallel.
11	SPORT_TFS0/SPI_SEL6	Sport 0 transmit frame sync. SPI Peripheral Chip Select 6.
12	SPORT_DT0SEC	Sport 0 data transmit secondary.
13	+2.5VD/3.3V_EDGE	2.5 V/3.3 V digital supply.
14	SPORT_DT0PRI/SPI_SEL7	Sport 0 data transmit primary. SPI Peripheral Chip Select 7.
15	+3.3VD_EDGE	2.5 V/3.3 V digital supply.
16	SPORT_RSCLK0/SPI_SEL2	SPORT 0 receive serial clock. SPI Peripheral Chip Select 2. This continuous clock is connected to the MCLKOUT pin of the AD7400A via J7.
17	$\overline{\text{SPI_SS}}$	SPT slave select.
18	SPI_MOSI	SPI master out, slave in data line.
19	SPI_SEL1	SPI Peripheral Chip Select 1.
20	SPI_MISO	SPI master in, slave out data line.
21	SPI_SEL2	SPI Peripheral Chip Select 2.
22	SPI_CLK	SPI clock.
23	SPI_SEL3	SPI Peripheral Chip Select 3.
24	TWI_SDA	2-wire interface serial data.
25	SPI_SEL4	SPI Peripheral Chip Select 4.
26	TWI_SCL	2-wire interface serial clock.
27	SPI_SEL5	SPI Peripheral Chip Select 5.
28	RXINT/GPIO2/PPI_FS3	Receive data interrupt. General-Purpose I/O Bit 2. Parallel Peripheral Interface Frame Sync 3.
29	SPI_SEL6	SPI Peripheral Chip Select 6.
30	GPIO3/TMR1/PPI_FS1	General-Purpose I/O Bit 3. Timer 1. Parallel Peripheral Interface Frame Sync 1.
31	SPI_SEL7	SPI Peripheral Chip Select 7.
32	TMR0/PPI_FS2	Timer 0. Parallel Peripheral Interface Frame Sync 2.
33	DGND	Digital ground.
32	DGND	Digital ground.

EVAL-AD7400A/AD7401A

SOCKETS

There are 4 SMB input sockets relevant to the operation of the AD7400A or AD7401A on this evaluation board. All of these sockets are used for applying an externally generated signal to the evaluation board. When operating the board with the EVAL-CED1Z, the only external sockets necessary are those used to supply the differential input signals to the analog inputs of the ADC (that is, J2 (V_{IN+}), J3 (V_{IN-})). All of the other sockets are optional and if they are not used, their signals are supplied by the EVAL-CED1Z. Most of these sockets are used when operating the board as a standalone unit, as all the signals required are supplied from external sources. The functions of these sockets are outlined in Table 4.

The V_{DD1} supply, which is the supply for the isolated side of the device, must be supplied by an external source via the J1-1 connector. The V_{DD2} supply must be supplied by 3.3 V from an external source via the J4 connector.

Table 4. Socket Functions

Socket	Function
J2 (V_{IN+})	Subminiature BNC socket for a unipolar differential input that is applied directly to the V_{IN+} pin of the AD7400A or AD7401A.
J3 (V_{IN-})	Subminiature BNC socket for a unipolar differential input that is applied directly to the V_{IN-} pin of the AD7400A or AD7401A.
J5 (MCLKOUT/MCLKIN)	Subminiature BNC socket for the MCLKOUT output on the AD7400A or subminiature BNC socket for the MCLKIN input to the AD7401A.
J6 (MDAT)	Subminiature BNC socket for the MDAT output.

CONNECTORS

There are three connectors on the EVAL-AD7400A/AD7401A as outlined in Table 5.

Table 5. Connector Functions

Connector	Function
J1-1	External V_{DD1} power connector.
J1-2	External GND_1 power connector.
J1-3	External -5 V power connector.
J4-1	External V_{DD2} power connector.
J4-2	GND_2 power connector.
J12	SPORT connector for the digital interface and power supply connections.

TEST POINTS

There are numerous test points on the EVAL-AD7400A/AD7401A. The test points enable the user to have easy access to these signals for probing, evaluation, and debugging.

OPERATING WITH THE EVAL-CED1Z

The evaluation board can be operated in standalone mode or operated in conjunction with the EVAL-CED1Z. This evaluation board controller is available from Analog Devices under the order entry EVAL-CED1Z.

When interfacing the EVAL-AD7400A/AD7401A directly to the EVAL-CED1Z, the control signals to operate the EVAL-AD7400A/AD7401A are provided by the EVAL-CED1Z. The device supplies (V_{DD1} , V_{DD2} , and -5 V) need to be supplied by an external source via the J1 and J4 connectors. If the AD797 op amps are not being used, then the -5 V is not required.

The AD7400A and AD7401A are isolated Σ - Δ modulators that convert an analog input signal into a high speed (10 MHz typical for AD7400A and 20 MHz for the AD7401A), single-bit data stream. The time average of the single-bit data from the modulator is directly proportional to the input signal. To generate an output digital word similar to a conventional ADC, the 1 bit output data stream from the AD7400A or AD7401A needs to be processed by a digital filter. A sinc3 filter is recommended for use with a decimation rate of 256, this results in a 16-bit word with a throughput rate of 39 kHz, assuming a 10 MHz clock frequency. The sinc3 filter has been implemented in the FPGA on the EVAL-CED1Z and hence the performance results displayed by the software are generated using this filter with a decimation rate of 256.

For the AD7401A the MCLKIN is supplied by the EVAL-CED1Z. The MCLK frequency is set at 16 MHz. This gives a throughput rate of 62.5 kSPS for a decimation rate of 256. The software allows the user to change the throughput rate by effectively modifying the decimation rate.

Software to communicate with the EVAL-CED1Z and the AD7400A or AD7401A is provided with the EVAL-AD7400A/AD7401A package.

The SPORT connector on the EVAL-AD7400A/AD7401A plugs directly into the SPORT connector on the EVAL-CED1Z board. The EVAL-CED1Z board is powered from a 7 V, 15 W power supply which accepts input voltages from 100 V to 240 V ac and contains the relevant adaptors for worldwide use. The power supply is provided with the EVAL-CED1Z.

Connection between the EVAL-CED1Z and the USB port of a PC is via a standard USB 2.0 connection cable that is provided as part of the EVAL-CED1Z package.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-AD7400A/AD7401A evaluation kit includes self-installing software on CD, for controlling and evaluating the performance of the [AD7400A](#) or [AD7401A](#) when it is operated with the EVAL-CED1Z. The software is compatible with Windows® 2000/XP. If the setup file does not run automatically, **setup.exe** can be run from the CD.

When the CD is inserted into the PC, an installation program automatically begins. This program installs the evaluation software. The user interface on the PC is a dedicated program written especially for the AD7400A or AD7401A when operating with the EVAL-CED1Z.

Note that the software should be installed before the USB cable is connected between the EVAL-CED1Z and the PC. This ensures that the appropriate USB driver files have been properly installed before the EVAL-CED1Z is connected to the PC.

When the software is run for the first time with EVAL-CED1Z connected to the PC, the PC automatically finds the new device and identifies it. Follow the on-screen instructions that appear. This installs the drivers for the EVAL-CED1Z on the PC. If an error appears on screen when the software is first opened, then the PC does not recognize the USB device. Correct this error with the following steps:

1. Click the **My Computer** icon, then select **Properties**. When the **System Properties** window opens, select the **Hardware** tab.
2. Click **Device Manager** in the **Hardware Tab** of the **System Properties** window.
3. Examine the devices listed under the **Universal Serial Bus Controller** heading.
4. If an unknown device is listed, right click this option and select **Update Driver**.
5. The **New Hardware Wizard** runs twice. Under **ADI Development Tools** the hardware is listed as **ADI Converter Evaluation and Development Board (WF)**.
6. Reboot your PC.

SETTING UP THE EVAL-CED1Z

This section describes how the evaluation board, the EVAL-CED1Z, and the software should be setup to begin using the complete system.

1. Install the EVAL-AD7400A/AD7401A software.
2. Connect the EVAL-CED1Z board and the evaluation board via the SPORT connector. Apply power to the EVAL-CED1Z via the 7 V, 15 W power supply provided. At this stage, the green LED labeled **Power**, on the EVAL-CED1Z should be lit indicating that the EVAL-CED1Z is receiving power.
3. The USB cable can then be connected between the PC and the EVAL-CED1Z. A green LED positioned beside the USB connector on the EVAL-CED1Z board lights up indicating that the USB connection has been established.
4. The EVAL-AD7400A/AD7401A is detected. Proceed through any dialog boxes that may appear (use the recommended options) to finalize the installation.
5. Start the EVAL-AD7400A/AD7401A software. The FPGA on the EVAL-CED1Z is automatically programmed when the software is opened. The two red LEDs (D14 and D15) on the EVAL-CED1Z now light up. This indicates that the EVAL-CED1Z is functional and ready to receive instructions.

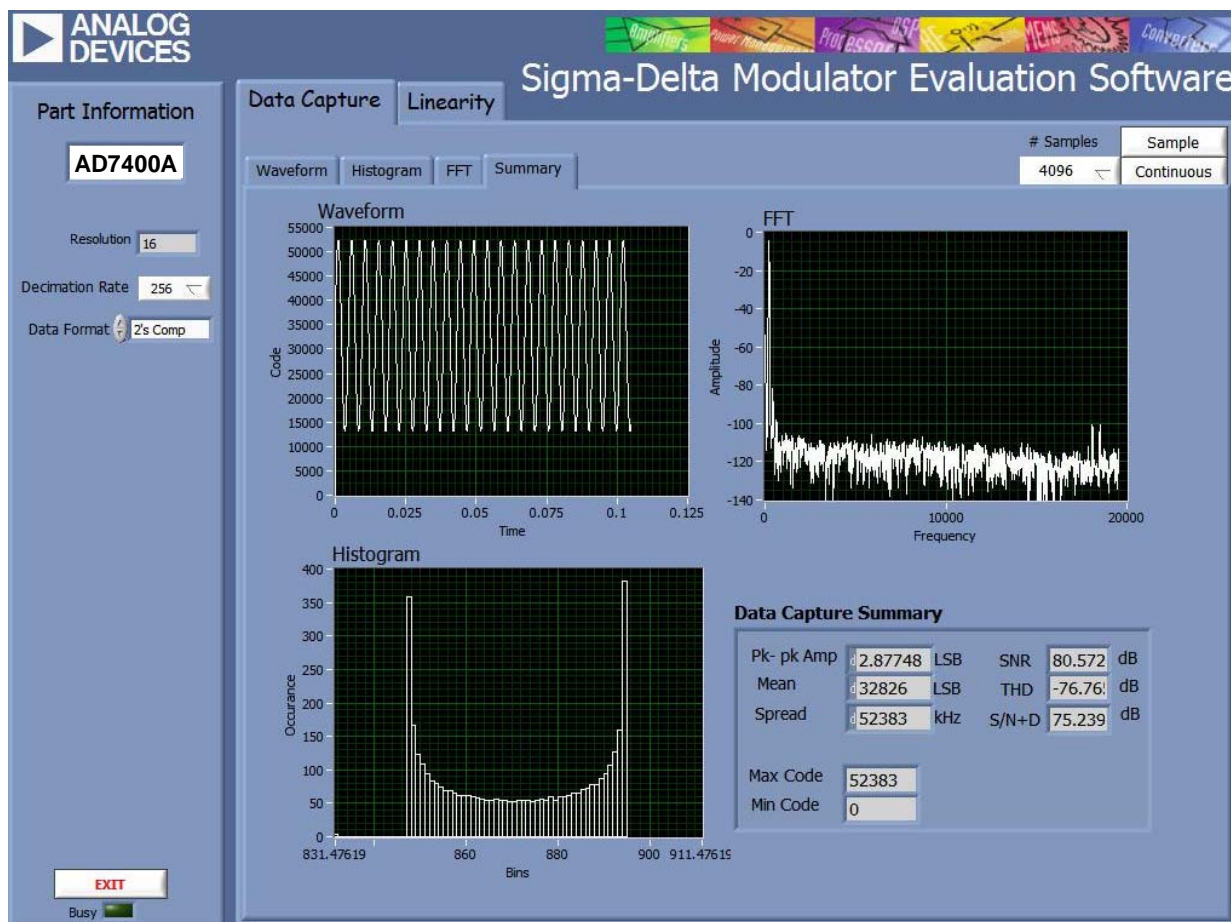


Figure 2. AD7400A Summary Window

SOFTWARE OPERATION

With the hardware set up, you can now use the software to control the EVAL-CED1Z and the EVAL-AD7400A/AD7401A. To launch the software from the **Analog Devices** menu, click the **AD7400A/AD7401A** submenu, then click the **AD7400A/AD7401A** icon. Figure 2 displays the main window that is opened. If an error message appears, click **OK** and restart the application after checking the connection between the adapter board and the USB port on the PC. Also check that the USB device is identified by the **Device Manager** as detailed in the Installing the Software section.

The software that controls the EVAL-CED1Z and, therefore, the EVAL-AD7400A/AD7401A, has two main windows. Figure 2 shows the window that appears when the software is run. The main function of this window is to allow you to read a predetermined number of samples from the evaluation board and display them in both the time and frequency domain. The screen can be divided into three main sections: **Part Information**, **Data Capture**, and **Linearity**. The top portion of the screen contains the menu bar, including the **Part Information** tab on the left hand side of the screen and a **Data Capture** tab in the center, which consists of a number of subtabs: **Waveform**, **Histogram**, **FFT**, and **Summary**.

The **Linearity** tab is also located in the center and enables you to generate a linearity plot for the device.

USING THE SOFTWARE

Menu Bar

The menu bar consists of the following menus: **File**, **Edit**, **Operate**, **Tools**, **Window**, and **Help**.

Part Information Tab

The **Part Information** tab allows you to select a variety of configurations, such as **Resolution**, **Decimation Rate**, and **Data Format**.

- **Resolution:** The software automatically sets the resolution to 16 bits for the AD7400A or AD7401A.
- **Decimation Rate:** The default decimation rate for the sinc3 filter is 256. A variety of different decimation rates can be selected from the pull-down menu.
- **Data Format:** The data format is set to binary by default.

The **Part Information** tab also includes a **Busy** status indicator which lights up when the evaluation board is busy. There is also an **Exit** button that allows you to quit the program.

Data Capture Tab

On the **Data Capture** tab, you can select the number of samples to be captured from the drop-down menu. The default number of samples is 8192; you are free to change this as required. The desired display option is selected by clicking the **Waveform**, **Histogram**, and **FFT** tab.

Waveform Tab

The **Waveform** tab displays a digital storage oscilloscope (DSO) that allows you to display a waveform. When samples are uploaded from the EVAL-CED1Z, they are displayed here. The samples are displayed as integer code values.

At the bottom left of the graph are the zoom options. These allow you to zoom in and out to get a closer look at a sample, if required. The **Waveform Analysis** section, located beneath the waveform graph, contains information about the samples taken, for example, minimum/maximum position or velocity, the spread, the standard deviation, and the mean.

Histogram Tab

The **Histogram** tab displays a histogram of the captured ADC codes. It can be used to give an indication of the performance of the ADC in response to dc inputs. The **Histogram Analysis** section contains information about the samples taken, for example maximum and minimum codes captured.

FFT Tab

The **FFT** tab displays a fast Fourier transform (FFT) plot. The FFT is typically used for examining the performance of the ADC in the frequency domain. The **Spectrum Analysis** section contains information about the samples taken, for example, ac specifications.

Linearity Tab

On the **Linearity** tab, you can select the number of hits per code to be captured for the linearity analysis. The desired display option is selected by clicking the **Histogram**, **INL**, **DNL**, or **Summary** tab buttons. To initiate the data collection, select the **Get Linearity Data** button. The data collection and analysis takes a few seconds to complete. The greater the number of hits per code selected the longer the analysis takes.

Histogram Tab

The **Histogram** tab displays a histogram of the captured ADC codes. It can be used to give an indication of the performance of the ADC in response to dc inputs. The **Histogram Analysis** section contains information about the samples taken, for example maximum and minimum codes captured.

INL Tab

The **INL** tab displays an INL plot for the [AD7400A](#) or [AD7401A](#). This plot can be used to examine the dc performance of the ADC. The **Linearity Analysis** section contains information on the maximum and minimum INL error and the code at which this error occurred. It also shows the total number of hits per code and the number of samples taken.

DNL Tab

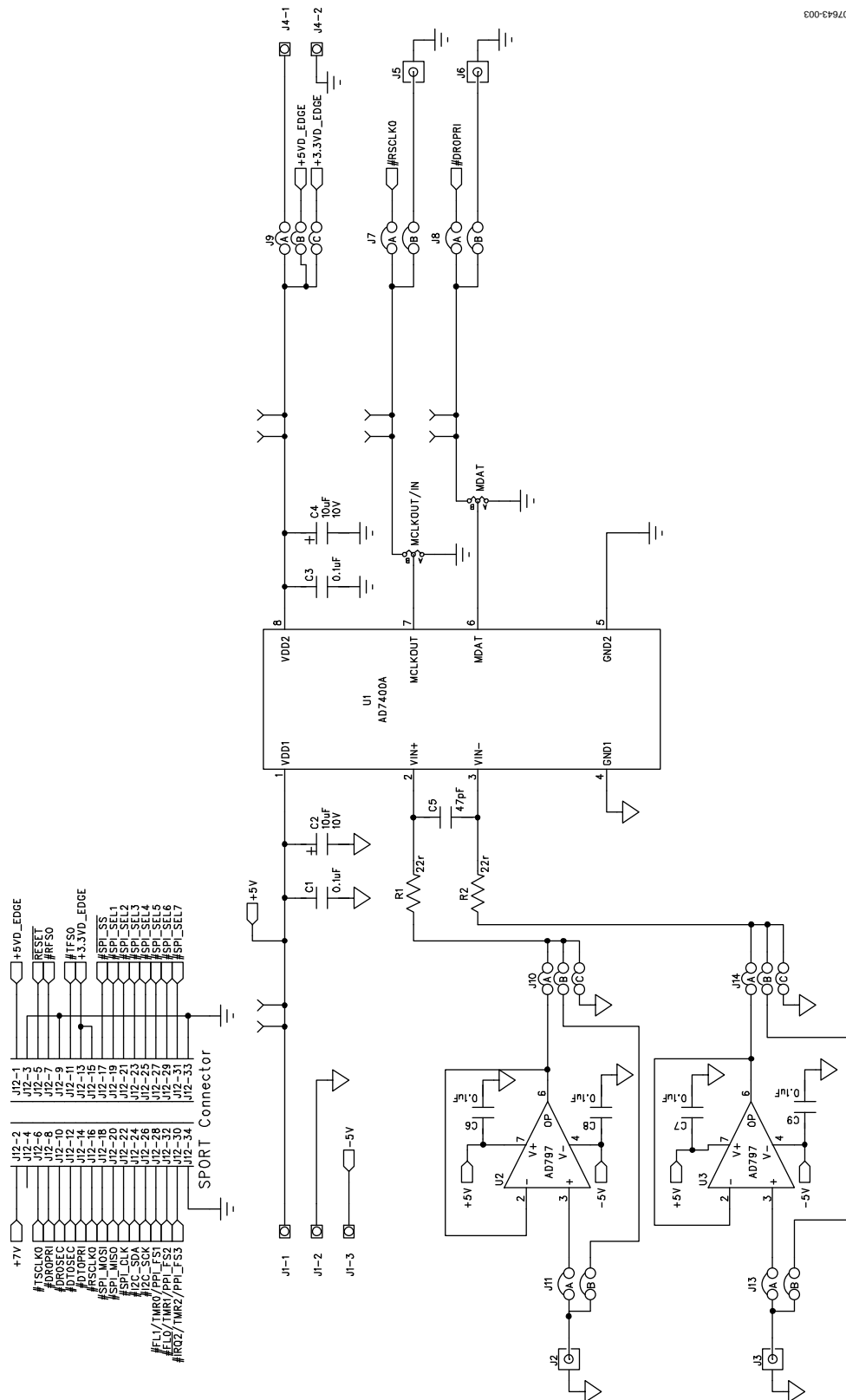
The **DNL** tab displays a DNL plot for the AD7400A or AD7401A. This plot can be used to examine the dc performance of the ADC in conjunction with the INL plot. The **Linearity Analysis** section contains information on the maximum and minimum DNL error and the code at which this error occurred.

TAKING SAMPLES

To initiate a conversion and capture the sample data, click the **Sample** button or the **Continuous** button. Both the **Sample** and the **Continuous** buttons are located on the top right hand corner of the **Data Capture** tab. When you click the **Sample** button, the software instructs the EVAL-CED1Z to take the required number of samples at the required frequency from the evaluation board. The EVAL-AD7400A/AD7401A runs with sampling speeds less than or equal to 39 kSPS. This sampling rate can be altered by changing the decimation rate selected for the filter. You can choose the decimation rate and the number of samples to be taken.

The samples taken are then uploaded and displayed. An FFT and/or histogram can be calculated and displayed. If you click the **Continuous** button, the software repeats the process indefinitely until you click **Stop**. (The **Continuous** button switches to **Stop** when selected).

EVAL-AD7400A and EVAL-AD7401A schematics, silkscreen, and layout diagrams can be found in Figure 3 to Figure 10.



07643-004

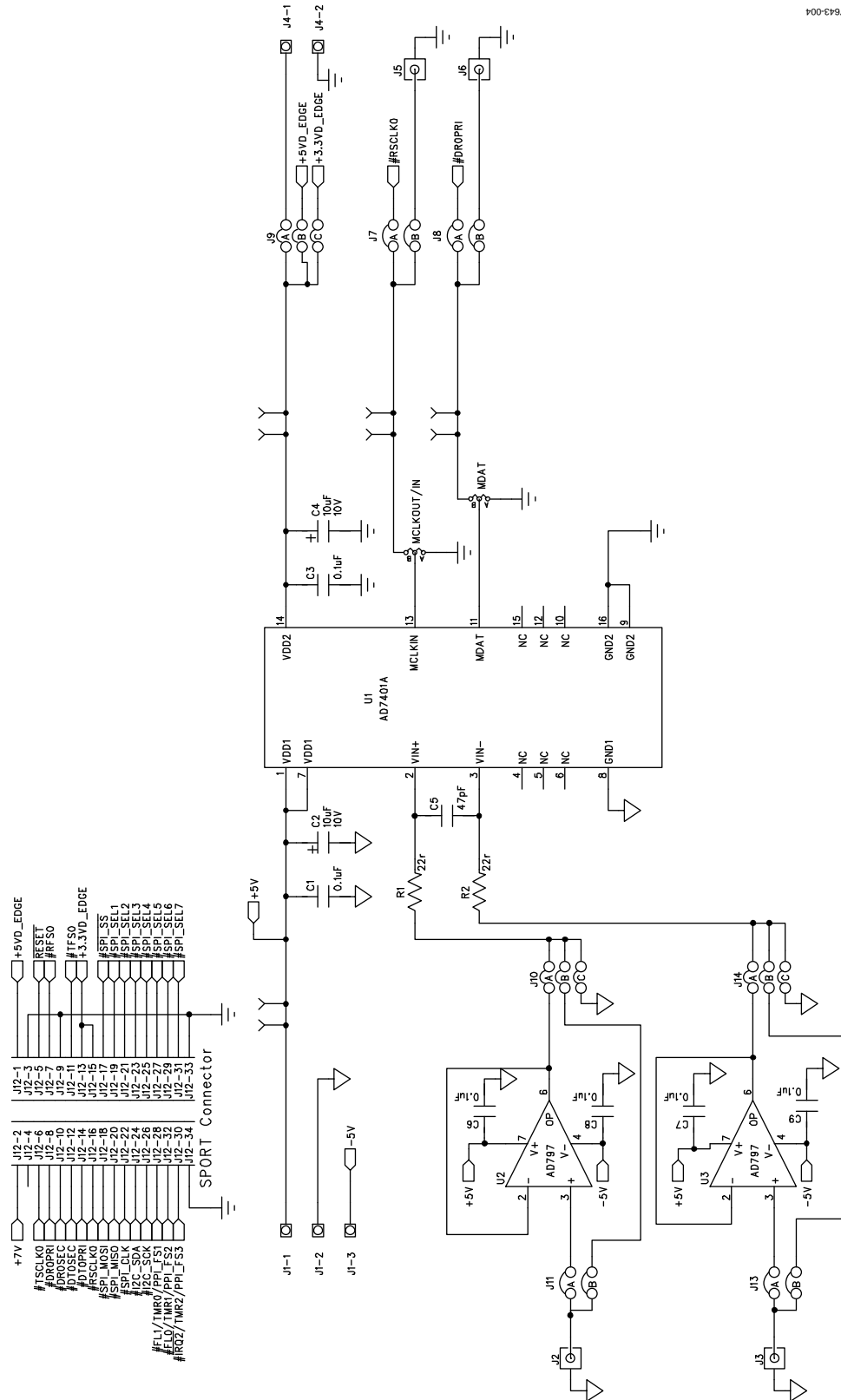


Figure 4. AD7401A Evaluation Board Circuit Diagram, 16-Lead SOIC Package

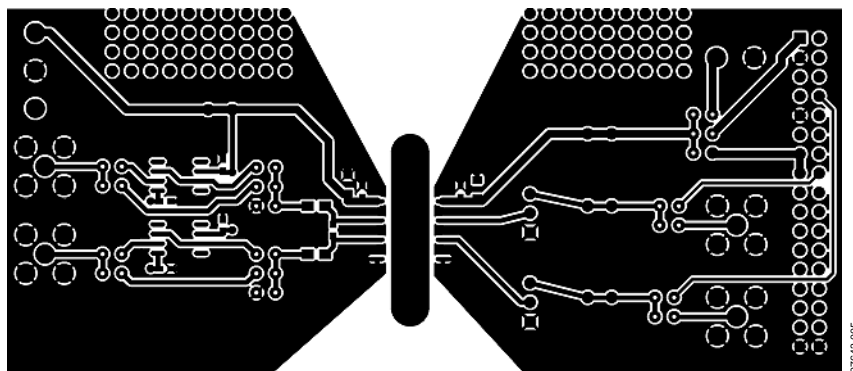


Figure 5. Component Side Artwork for the EVAL-AD7400A, 8-Lead Surface-Mount PDIP Packages with Gull Wing Leads

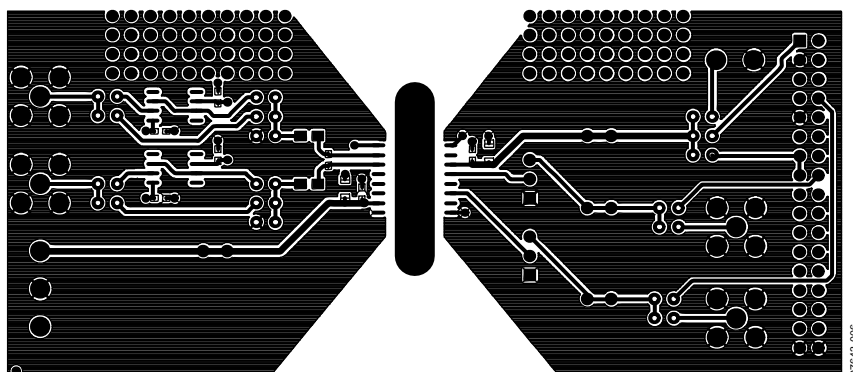


Figure 6. Component Side Artwork for the EVAL-AD7401A, 16-Lead SOIC Package

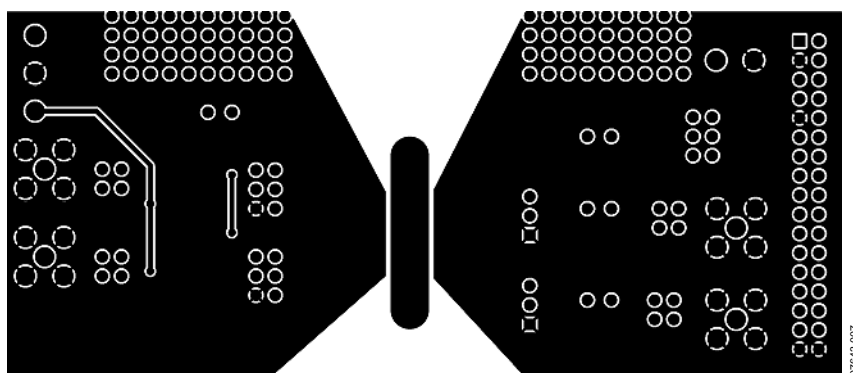


Figure 7. Solder Side Artwork for the EVAL-AD7400A, 8-Lead Surface-Mount PDIP Packages with Gull Wing Leads

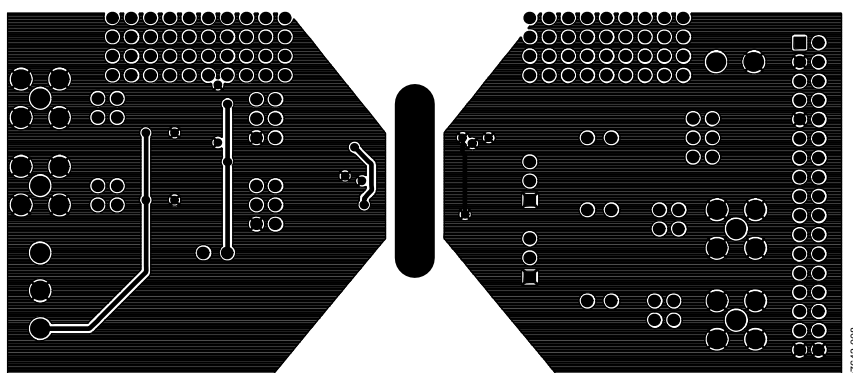


Figure 8. Solder Side Artwork for the EVAL-AD7401A, 16-Lead SOIC Package

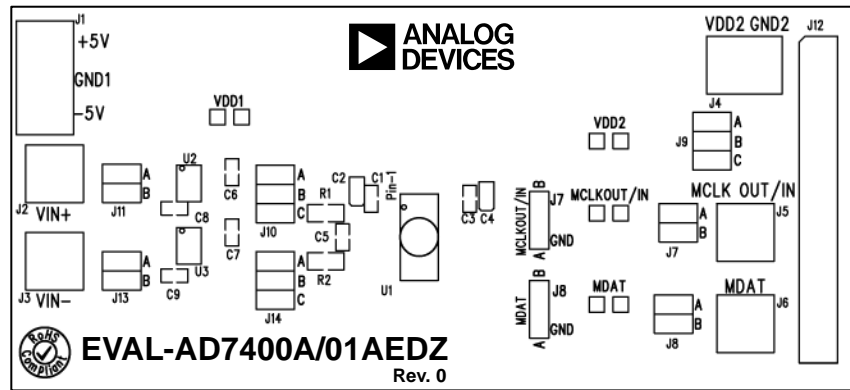


Figure 9. Silkscreen for the EVAL-AD7400A, 8-Lead Surface-Mount PDIP Packages with Gull Wing Leads

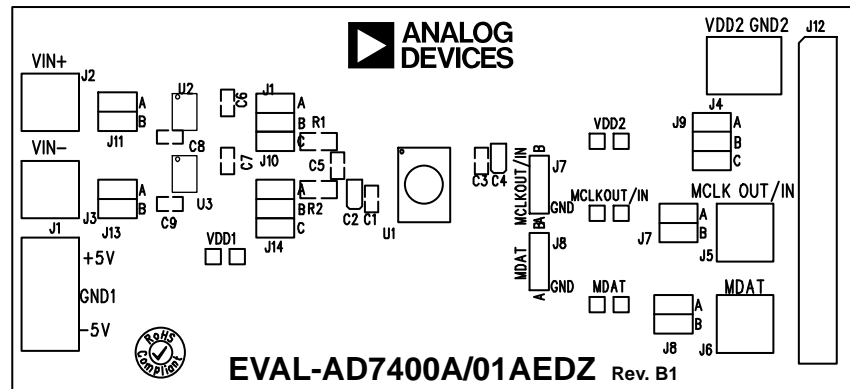


Figure 10. Silkscreen for the EVAL-AD7401A, 16-Lead SOIC Package

EVAL-AD7400A/AD7401A

ORDERING INFORMATION

BILL OF MATERIALS

Table 6.

Qty	Reference Designator	Description	Supplier/Number ¹
6	C1, C3, C6, C7, C8, C9	0.1 μ F capacitor	FEC 9406140
2	C2, C4	10 μ F capacitor	FEC 197130
1	C5	47 pF capacitor	FEC 498567
2	R1, R2	22 Ω resistor	FEC 1099789
1	U1	ADC (AD7400A or AD7401A)	Analog Devices AD7400YRWZ or AD7401YRWZ
2	U2, U3	Op amp, AD797ARZ	Analog Devices AD797ARZ
1	J1	Terminal block, connector\power 3-way	FEC 9632980
4	J2, J3, J5, J6	SMB connector	FEC 419 4512
1	J4	Terminal block, connector\power	FEC 151789
4	J7, J8, J11, J13	Jumper 2	FEC 1022244
3	J9, J10, J14	Jumper 3	FEC 1022244
1	J12	Header 34	Digi-Key S7085-ND

¹ FEC = Farnell Electronics, Inc.

ORDERING GUIDE

Model	Description
EVAL-AD7400AEDZ ¹	Evaluation Board for AD7400A
EVAL-AD7401AEDZ ¹	Evaluation Board for AD7401A
EVAL-CED1Z ¹	Converter Evaluation and Development Board

¹ Z = RoHS Compliant Part.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES

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