HEF4007UB

Dual complementary pair and inverter

Rev. 5 — 8 August 2024 | Product data sheet

1. General description

The HEF4007UB is a dual complementary pair and inverter. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD}.

2. Features and benefits

- Wide supply voltage range from 3.0 to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4007UBT	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

4. Functional diagram

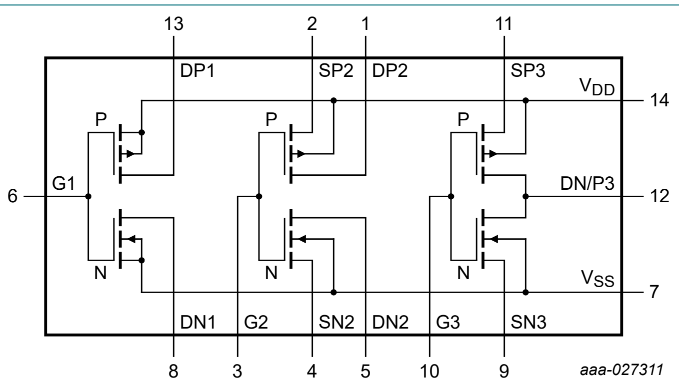

Fig. 1. Logic diagram

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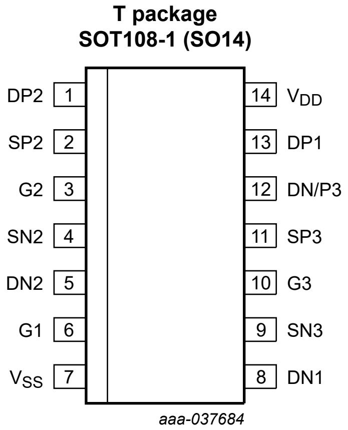
5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DP1, DP2	13, 1	drain connections from the 1st and 2nd p-channel transistors
SP2, SP3	2, 11	source connections to 2nd and 3rd p-channel transistors
G1, G2, G3	6, 3, 10	gate connections to n-channel and p-channel of the three transistor pairs
SN2, SN3	4, 9	source connections to the 2nd and 3rd n-channel transistors
DN1, DN2	8, 5	drain connection from the 1st and 2nd n-channel transistors
DN/P3	12	common connection to the 3rd p-channel and n-channel transistor drains
V_{SS}	7	ground (0 V)
V_{DD}	14	supply voltage

6. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current		-	±10	mA
V_I	input voltage		-0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current		-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

7. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	μs/V
		V_{DD} = 10 V	-	-	0.5	μs/V
		V_{DD} = 15 V	-	-	0.08	μs/V

8. Static characteristics

Table 5. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_O = 0.5 V or 4.5 V; $\|I_O\|$ < 1 μA	5 V	4	-	4	-	4	-	V
		V_O = 1.0 V or 9.0 V; $\|I_O\|$ < 1 μA	10 V	8	-	8	-	8	-	V
		V_O = 1.5 V or 13.5 V; $\|I_O\|$ < 1 μA	15 V	12.5	-	12.5	-	12.5	-	V
V_{IL}	LOW-level input voltage	V_O = 0.5 V or 4.5 V; $\|I_O\|$ < 1 μA	5 V	-	1	-	1	-	1	V
		V_O = 1.0 V or 9.0 V; $\|I_O\|$ < 1 μA	10 V	-	2	-	2	-	2	V
		V_O = 1.5 V or 13.5 V; $\|I_O\|$ < 1 μA	15 V	-	2.5	-	2.5	-	2.5	V

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ µA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ µA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output (source)current	V_O = 2.5 V; V_I = 0 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V_O = 4.6 V; V_I = 0 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V_O = 9.5 V; V_I = 0 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V_O = 13.5 V; V_I = 0 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output (sink)current	V_O = 0.4 V; V_I = 5 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V; V_I = 10 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V; V_I = 15 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current	V_I = 0 V to 15 V	15 V	-	±0.3	-	±0.3	-	±1.0	µA
I_{DD}	supply current	all valid input combinations; $V_I = V_{SS}$ or V_{DD}; I_O = 0 A	5 V	-	1.0	-	1.0	-	7.5	µA
			10 V	-	2.0	-	2.0	-	15.0	µA
			15 V	-	4.0	-	4.0	-	30.0	µA

9. Dynamic characteristics

Table 6. Dynamic characteristics

T_{amb} = 25 °C; for waveforms see Fig. 2; for test circuit see Fig. 3; unless otherwise specified.

Symbol	Parameter	Conditions	Extrapolation formula [1]	V_{DD}	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	Gn to Dn or DP	13 + 0.55 × C_L	5 V	-	40	80	ns
			9 + 0.23 × C_L	10 V	-	20	40	ns
			7 + 0.16 × C_L	15 V	-	15	30	ns
t_{PLH}	LOW to HIGH propagation delay	Gn to Dn or DP	13 + 0.55 × C_L	5 V	-	40	75	ns
			9 + 0.23 × C_L	10 V	-	20	40	ns
			7 + 0.16 × C_L	15 V	-	15	30	ns
t_t	output transition time [2]		10 + 1.0 × C_L	5 V	-	60	120	ns
			9 + 0.42 × C_L	10 V	-	30	60	ns
			6 + 0.28 × C_L	15 V	-	20	40	ns

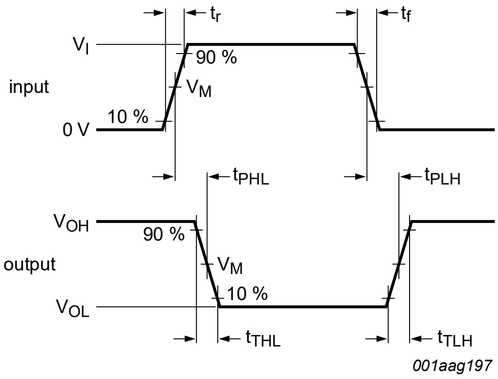
[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).
[2] t_t is the same as t_{THL} and t_{TLH}.

Table 7. Dynamic power dissipation

V_{SS} = 0 V; $t_r = t_f \leq$ 20 ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula	Where
P_D	dynamic power dissipation	5 V	$P_D = 4500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}{}^2$ (µW)	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.
		10 V	$P_D = 20000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}{}^2$ (µW)	
		15 V	$P_D = 50000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}{}^2$ (µW)	

9.1. Waveforms and test circuit



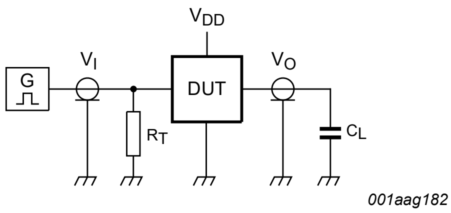
Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 2. Propagation delay, output transition time

Table 8. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	0.5 × V_{DD}	0.5 × V_{DD}



Test data is given in Table 9.

Definitions test circuit:

C_L = load capacitance including jig and probe capacitance;

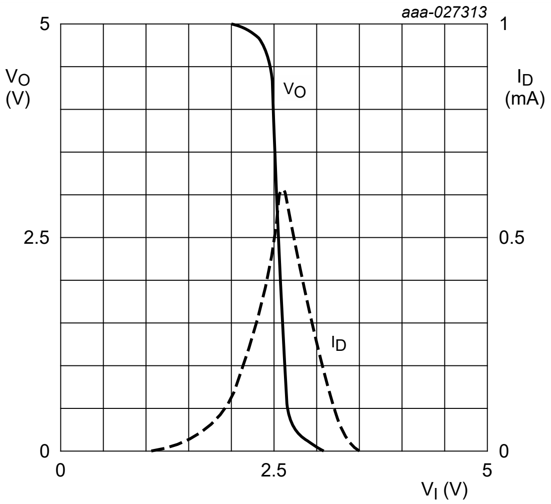
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 3. Test circuit for measuring switching times

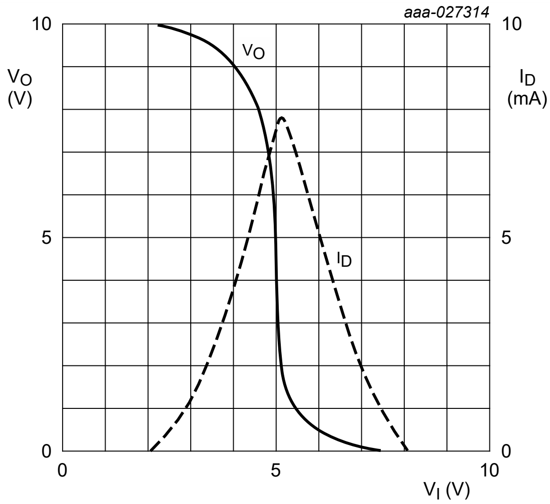
Table 9. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

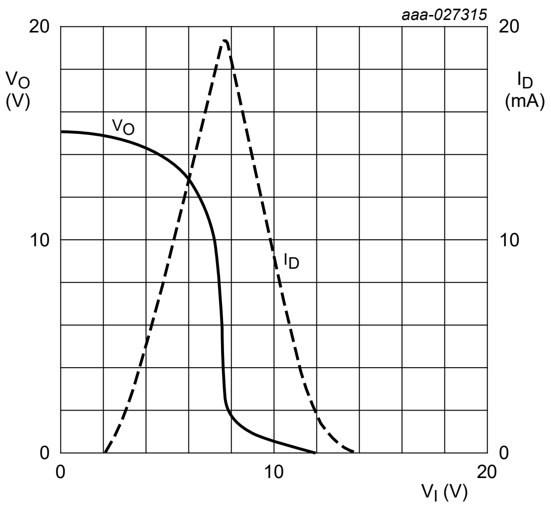
9.2. Characteristics



a. V_{DD} = 5 V; T_{amb} = 25 °C



b. V_{DD} = 10 V; T_{amb} = 25 °C



c. V_{DD} = 15 V; T_{amb} = 25 °C

Fig. 4. Typical drain current I_D and output voltage V_O as functions of input voltage

10. Application information

Some examples of applications for the HEF4007UB are:

- High input impedance amplifiers
- Linear amplifiers
- (Crystal) oscillators
- High-current sink and source drivers
- High impedance buffers

Note:

Rules for maintaining electrical isolation between transistors and monolithic substrate:

- The V_{DD} supply pin (Pin 14) must be maintained at the most positive (or equally positive) potential with respect to any other pin of the HEF4007UB.
- The V_{SS} ground pin (Pin 7) must be maintained at the most positive (or equally positive) potential with respect to any other pin of the HEF4007UB.

Violation of these rules will result in improper transistor operation and/or possible permanent damage to the HEF4007UB.

Fig. 5 and Fig. 6 show voltage gain and supply current. Fig. 7 shows the test set-up and an example of an analog amplifier using one HEF4007UB.

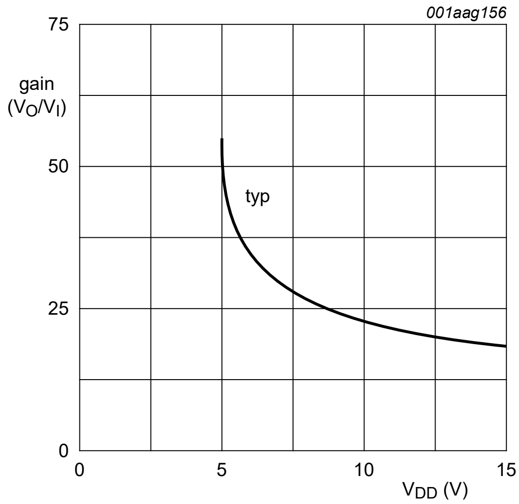


Fig. 5. Typical voltage gain as a function of supply voltage

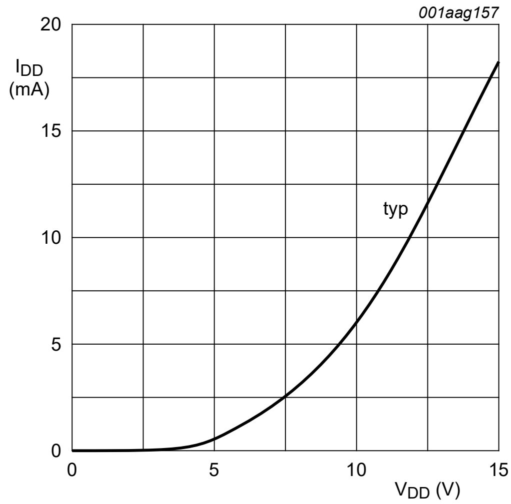


Fig. 6. Typical supply current as a function of supply voltage

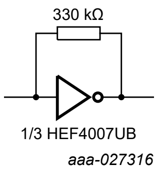
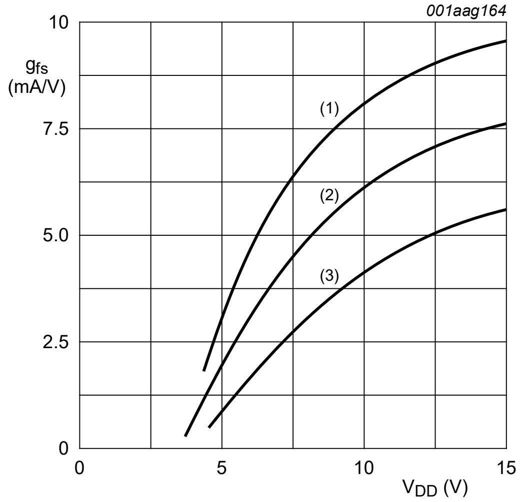


Fig. 7. Test set-up

Fig. 8 shows typical forward transconductance and Fig. 9 shows the test set-up.

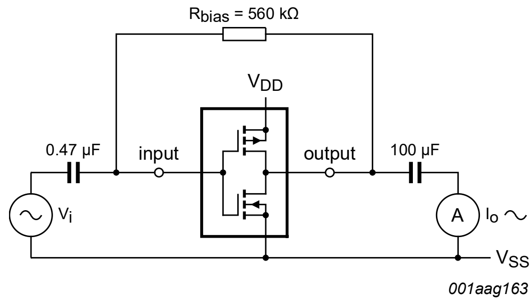


(1) Average +2σ; where: 'σ' is the standard deviation.

(2) Average.

(3) Average -2σ; where: 'σ' is the standard deviation.

Fig. 8. Typical forward transconductance as a function of supply voltage at T_{amb} = 25 °C



$g_{fs} = \frac{dI_O}{dV_i}$ at V_O is constant.

f_i = 1 kHz

Fig. 9. Test set-up

Fig. 10, Fig. 11, Fig. 12 and Fig. 13 show some applications in which the HEF4007UB is used.

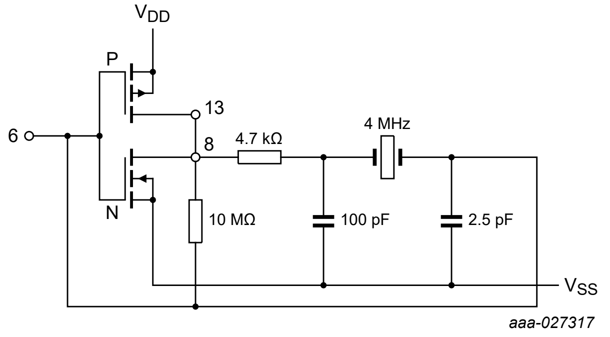


Fig. 10. 4 MHz crystal oscillator

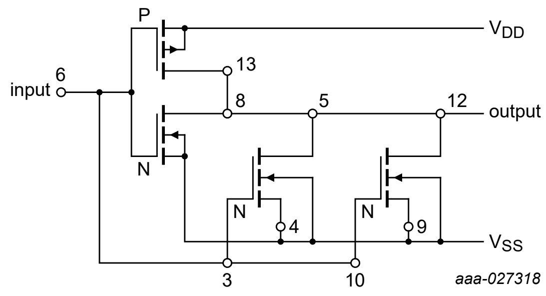


Fig. 11. High current sink driver

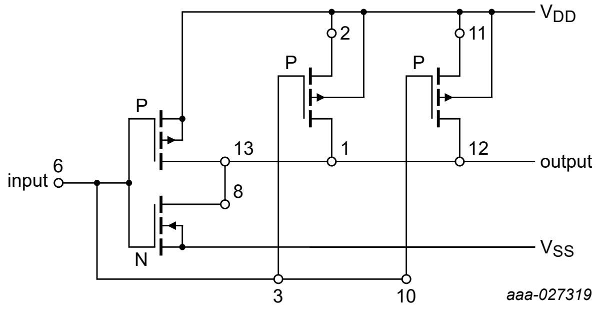


Fig. 12. High current source driver

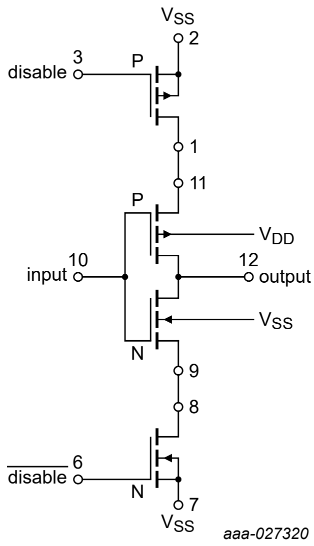


Fig. 13. High impedance buffer

Table 10. Function table

For Fig. 13. High impedance buffer

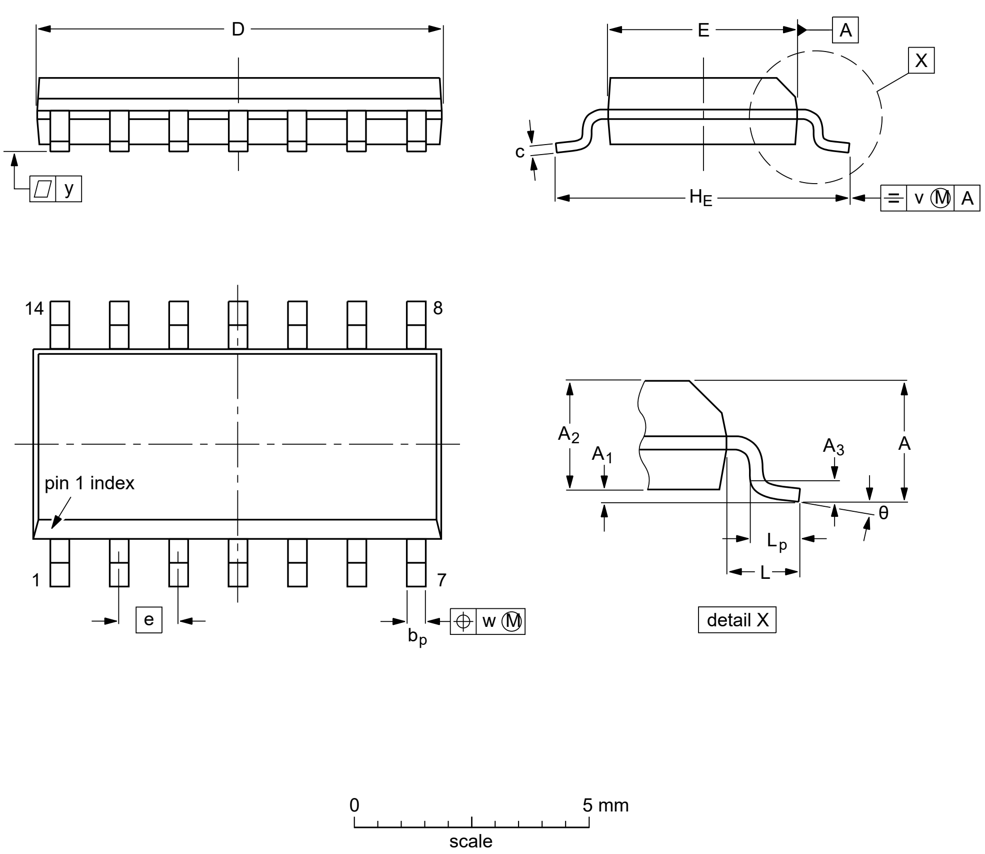
H = HIGH state (the more positive voltage); L = LOW state (the less positive voltage);

X = state is immaterial; Z = HIGH-impedance OFF-state

Input	Disable	Output
H	L	L
L	L	H
X	H	Z

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	8.75	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	8.55	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.344	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.337	0.15		0.228		0.016				0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot108-1_po

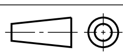
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 14. Package outline SOT108-1 (SO14)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4007UB v.5	20240808	Product data sheet	-	HEF4007UB v.4
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 14: Aligned SO package outline drawing to JEDEC MS-012 • Section 1 and Section 2 updated. • Section 6: Derating values for P_{tot} total power dissipation removed.			
HEF4007UB v.4	20170831	Product data sheet	-	HEF4007UB v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number HEF4007UBP and HEF4007UBD removed.			
HEF4007UB v.3	19951201	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 8 August 2024