STL23NS3LLH7

N-channel 30 V, 0.0027 Ω typ., 23 A STripFET™ H7 Power MOSFET plus monolithic Schottky in a PowerFLAT™ 3.3 x 3.3

Datasheet - production data

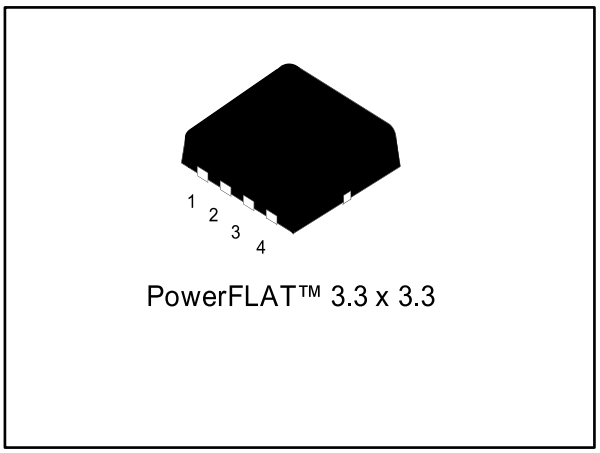
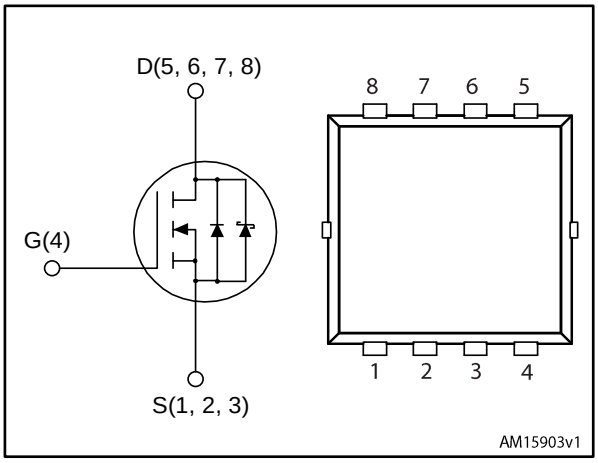


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STL23NS3LLH7	30 V	0.0037 Ω	23 A

- Very low on-resistance
- Very low Q_g
- High avalanche ruggedness
- Embedded Schottky diode

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes the STripFET H7 technology with a trench gate structure combined with extremely low on-resistance. The device also offers ultra-low capacitances for higher switching frequency operations.

Table 1: Device summary

Order code	Marking	Package	Packing
STL23NS3LLH7	23NS3	PowerFLAT™ 3.3 x 3.3	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_{pcb} = 25 °C	23	A
I_D (1)	Drain current (continuous) at T_{pcb} = 100 °C	14.3	A
I_{DM} (1)(2)	Drain current (pulsed)	92	A
I_D (3)	Drain current (continuous) at Tc = 25 °C	92	A
I_D (3)	Drain current (continuous) at Tc = 100 °C	57.5	A
I_{DM} (2)(3)	Drain current (pulsed)	368	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	50	W
P_{TOT} (3)	Total dissipation at T_{pcb} = 25 °C	2.9	W
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Operating junction temperature		

Notes:

(1)This value is rated according to $R_{thj\text{-}c}$.

(2)Pulse width limited by safe operating area.

(3)This value is rated according to $R_{thj\text{-}pcb}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	42.8	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.5	°C/W

Notes:

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V V_{DS} = 24 V			500	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 20 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	1.2		2.3	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 11.5 A		0.0027	0.0037	Ω
		V_{GS} = 4.5 V, I_D = 11.5 A		0.004	0.005	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 15 V, f = 1 MHz, V_{GS} = 0 V	-	2100	-	pF
C_{oss}	Output capacitance		-	850	-	pF
C_{rss}	Reverse transfer capacitance		-	60	-	pF
Q_g	Total gate charge	V_{DD} = 10 V, I_D = 23 A, V_{GS} = 4.5 V (see *Figure 13: "Gate charge test circuit"*)	-	13.7	-	nC
Q_{gs}	Gate-source charge		-	7.5	-	nC
Q_{gd}	Gate-drain charge		-	3.3	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 11.5 A, R_G = 3 Ω, V_{GS} = 4.5 V	-	10	-	ns
t_r	Rise time		-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	22	-	ns
t_f	Fall time		-	7.5	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 2 A, V_{GS} = 0	-	0.4	0.7	V
t_{rr}	Reverse recovery time	I_{SD} = 2 A, di/dt = 100 A/µs V_{GS} = 0 V	-	31.2		ns
Q_{rr}	Reverse recovery charge		-	18.7		nC
I_{RRM}	Reverse recovery current		-	1.2		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

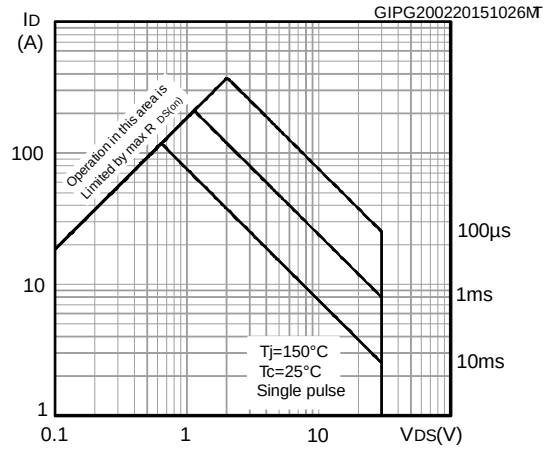


Figure 3: Thermal impedance

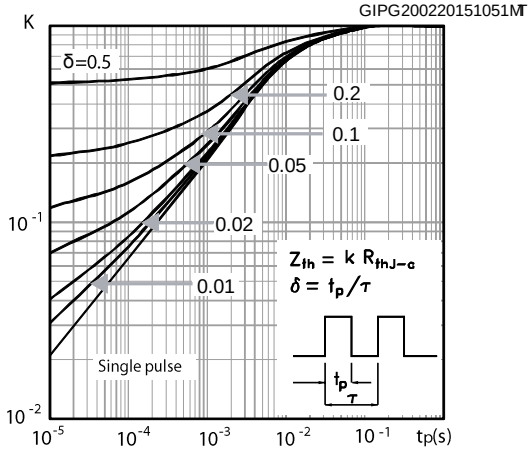


Figure 4: Output characteristics

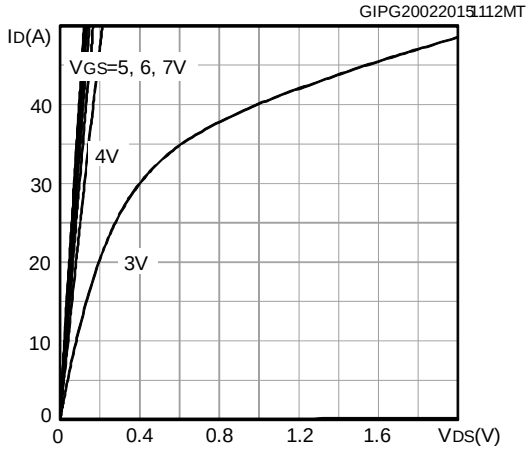


Figure 5: Transfer characteristics

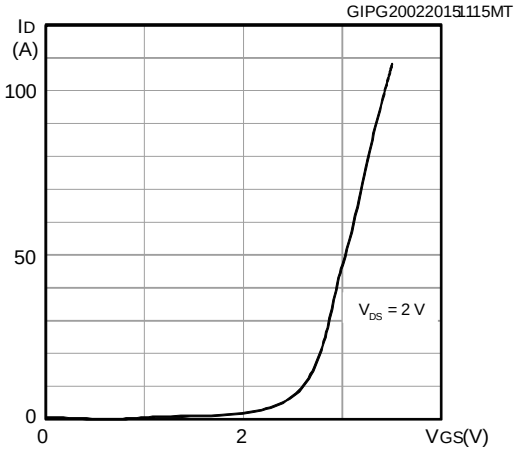


Figure 6: Gate charge vs gate-source voltage

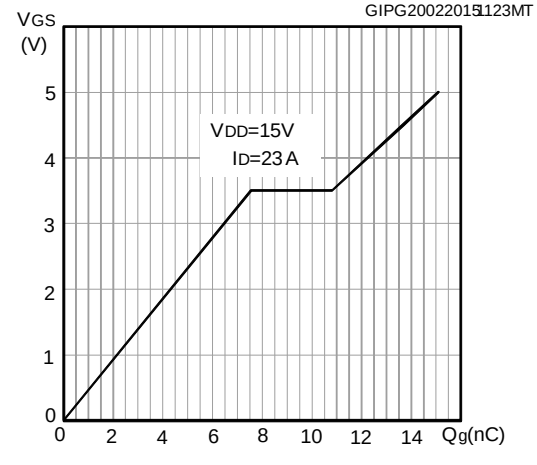


Figure 7: Static drain-source on-resistance

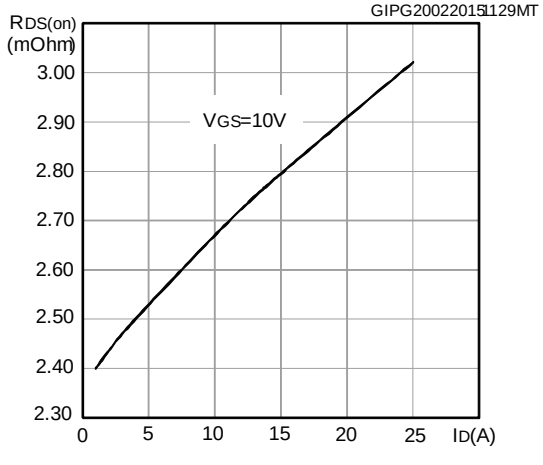


Figure 8: Capacitance variations

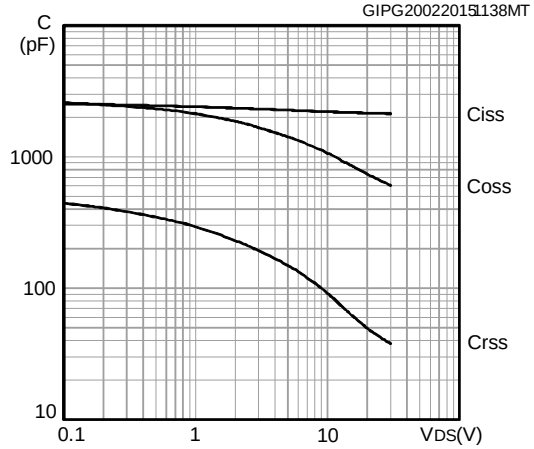


Figure 9: Normalized on-resistance vs temperature

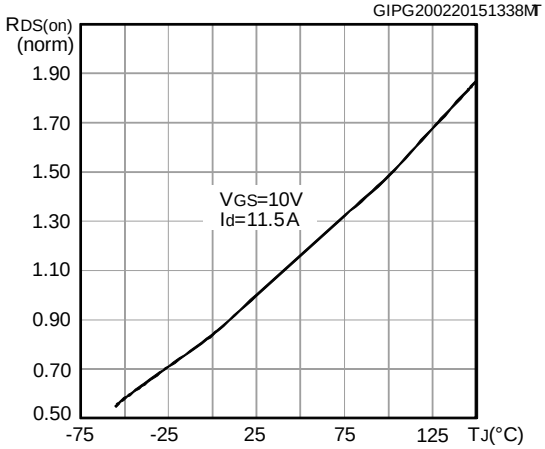


Figure 10: Normalized $V_{(BR)DSS}$ vs temperature

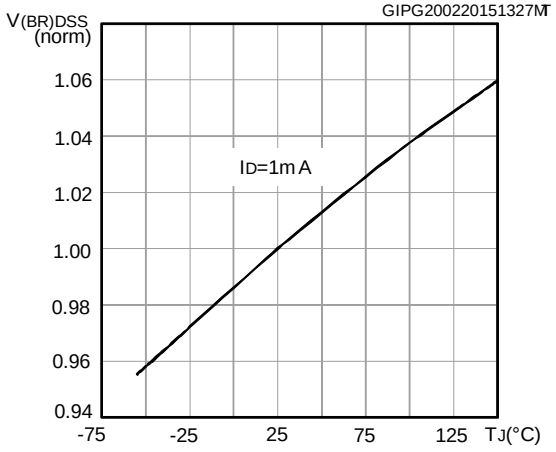
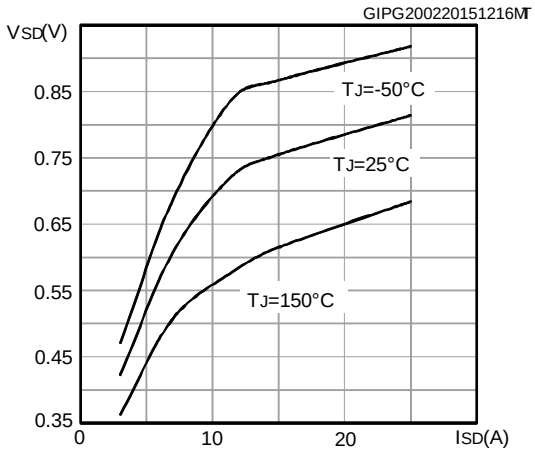


Figure 11: Source-drain diode forward characteristics



3 Test circuits

Figure 12: Switching times test circuit for resistive load

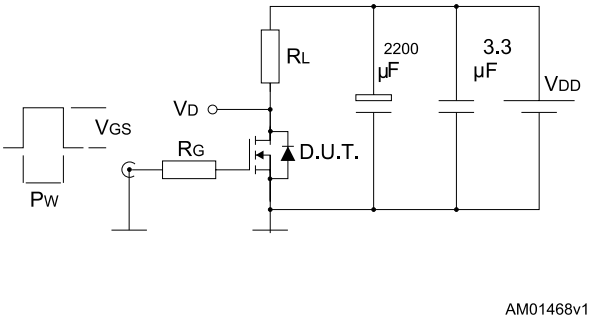


Figure 13: Gate charge test circuit

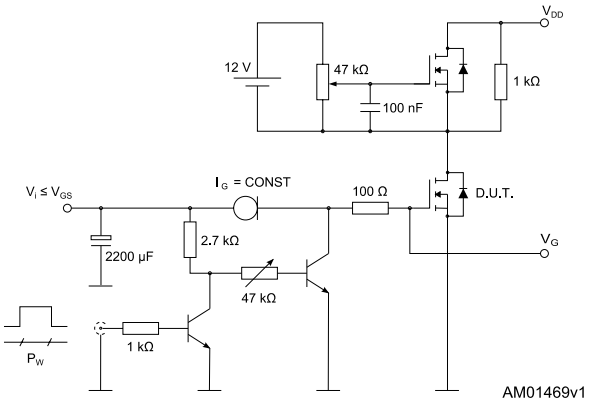


Figure 14: Test circuit for inductive load switching and diode recovery times

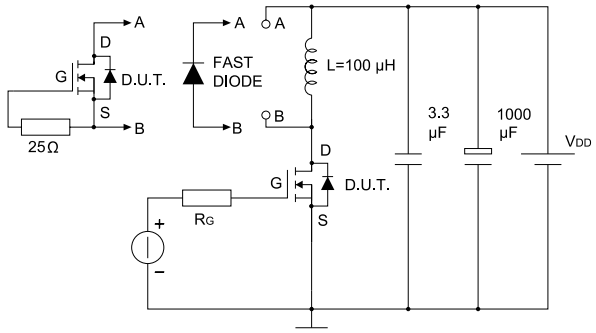


Figure 15: Unclamped inductive load test circuit

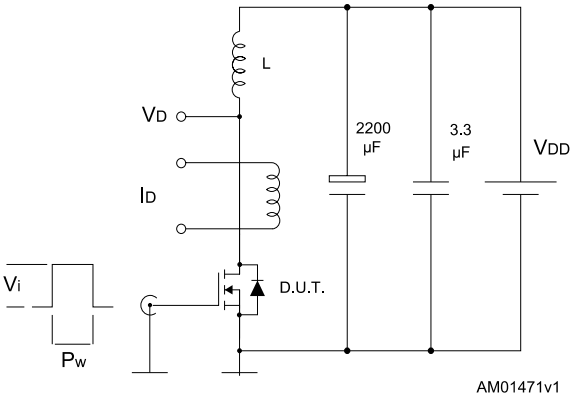


Figure 16: Unclamped inductive waveform

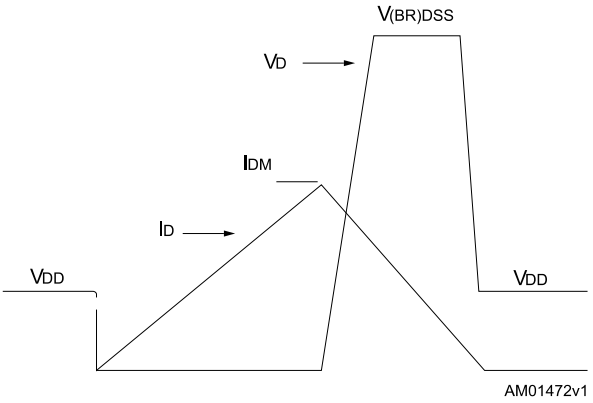
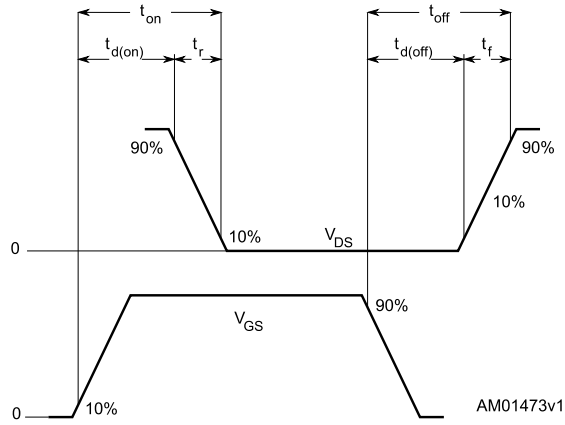


Figure 17: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFlat 3.3 x 3.3 package information

Figure 18: PowerFLAT™ 3.3 x 3.3 package outline

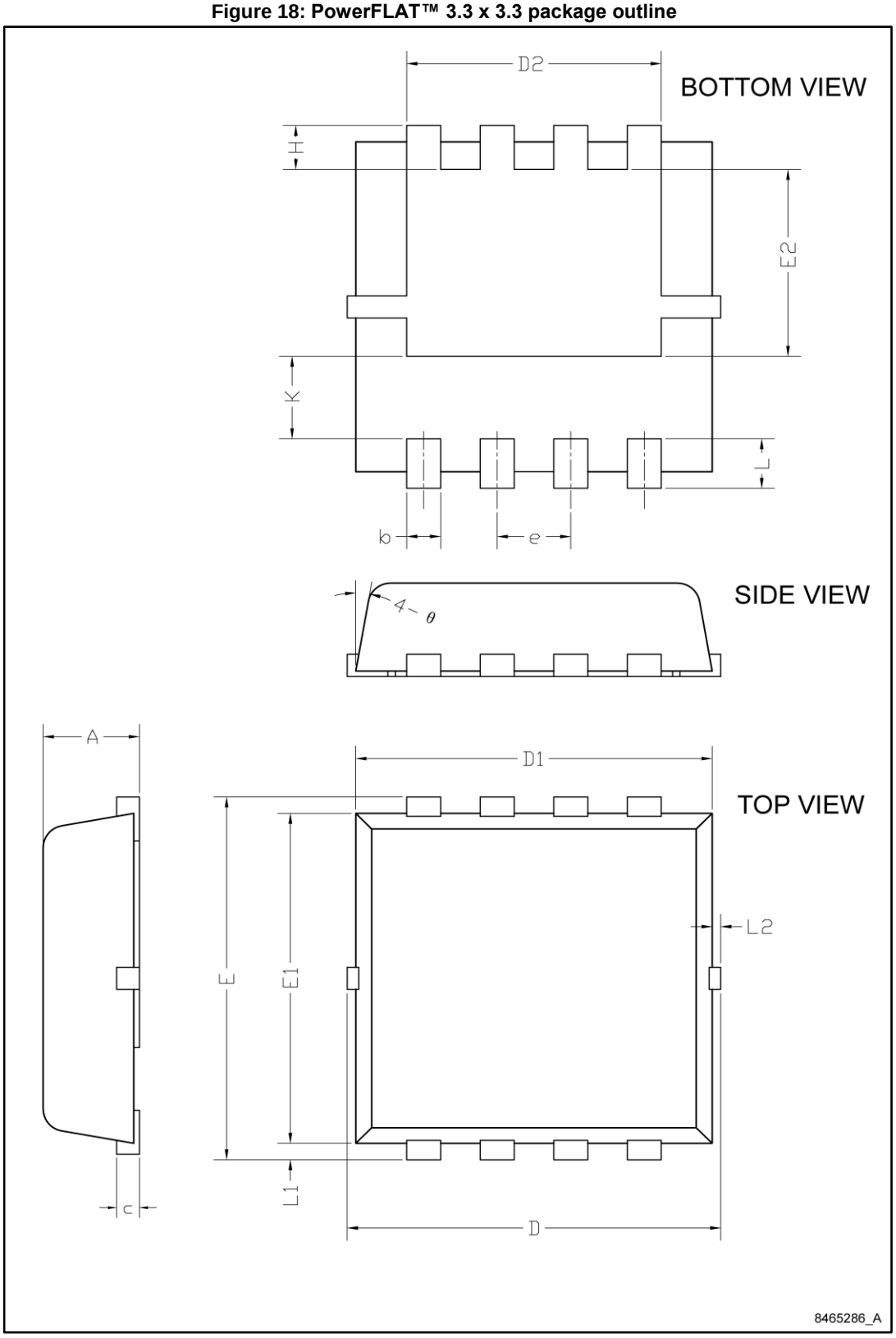
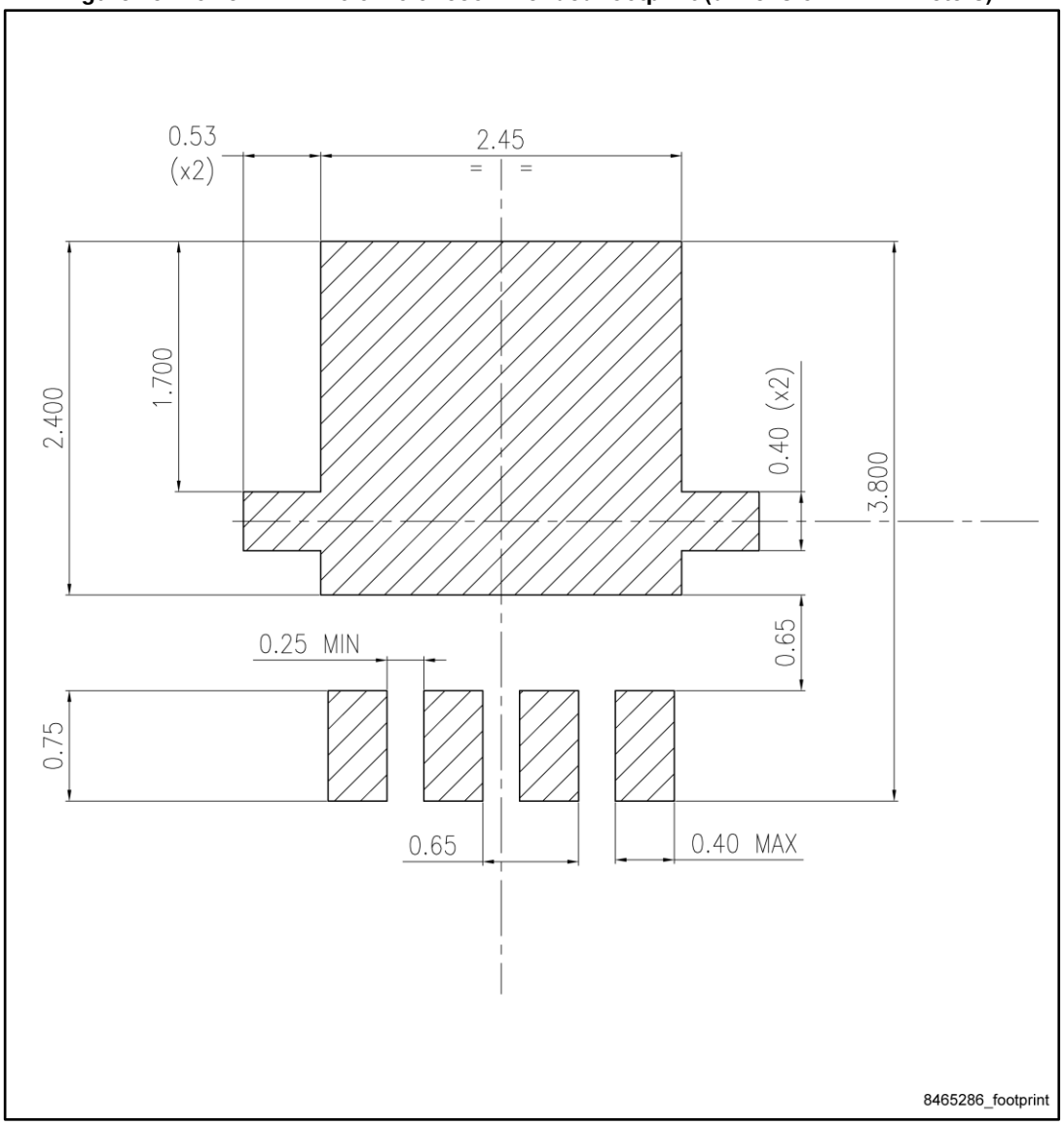


Table 8: PowerFLAT™ 3.3 x 3.3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
θ	8°	10°	12°

Figure 19: PowerFLAT™ 3.3 x 3.3 recommended footprint (dimension in millimeters)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
31-Jul-2013	1	First release.
27-Mar-2015	2	Updated title and features in cover page. Updated *Table 2: "Absolute maximum ratings"*, *Table 4: "On /off states"* and *Table 7: "Source drain diode"*. Added *Section 2.1: "Electrical characteristics (curves)"*. Minor text changes.
07-May-2015	3	Document status promoted from preliminary data to production data. Minor text changes.

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