600 MHz, 32 × 16 Buffered Analog Crosspoint Switch

AD8104/AD8105

FEATURES

- High channel count, 32 × 16 high speed, nonblocking switch array
- Differential or single-ended operation
- Differential G = +1 (AD8104) or G = +2 (AD8105)
- Pin compatible with AD8117/AD8118, 32 × 32 switch arrays
- Flexible power supplies
  - Single +5 V supply, or dual ±2.5 V supplies
- Serial or parallel programming of switch array
- High impedance output disable allows connection of multiple devices with minimal loading on output bus
- Excellent video performance
  - >50 MHz 0.1 dB gain flatness
  - 0.05% differential gain error (R_L = 150 Ω)
  - 0.05° phase error (R_L = 150 Ω)
- Excellent ac performance
  - Bandwidth: 600 MHz
  - Slew rate: 1800 V/μs
  - Settling time: 2.5 ns to 1%
- Low power of 1.7 W
- Low all hostile crosstalk
  - < −70 dB at 5 MHz
  - < −40 dB at 600 MHz
- Reset pin allows disabling of all outputs (connected through a capacitor to ground provides power-on reset capability)
- 304-ball BGA package (31 mm × 31 mm)

APPLICATIONS

- Routing of high speed signals including
  - RGB and component video routing
  - KVM
  - Compressed video (MPEG, wavelet)
  - Data communications

FUNCTIONAL BLOCK DIAGRAM

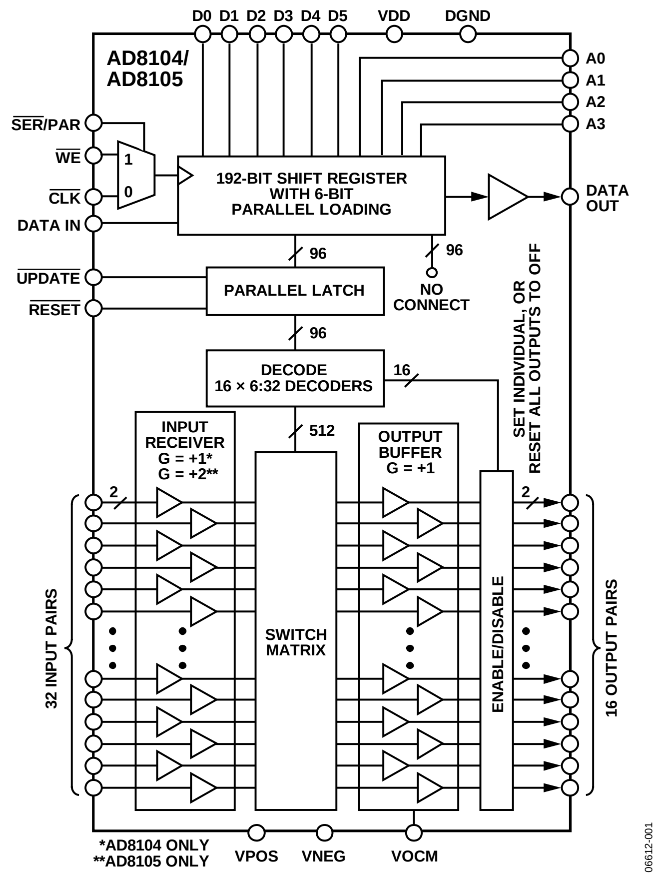

Figure 1.

GENERAL DESCRIPTION

The AD8104/AD8105 are high speed, 32 × 16 analog crosspoint switch matrices. They offer 600 MHz bandwidth and slew rate of 1800 V/μs for high resolution computer graphics (RGB) signal switching. With less than −70 dB of crosstalk and −90 dB isolation (at 5 MHz), the AD8104/AD8105 are useful in many high speed applications. The 0.1 dB flatness, which is greater than 50 MHz, makes the AD8104/AD8105 ideal for composite video switching.

The AD8104/AD8105 include 16 independent output buffers that can be placed into a high impedance state for paralleling crosspoint outputs so that off-channels present minimal loading to an output bus. The AD8104 has a differential gain of +1, while the AD8105 has a differential gain of +2 for ease of use in back-terminated load applications. They operate as fully differential devices or can be configured for single-ended operation. Either a single +5 V supply or dual ±2.5 V supplies can be used, while consuming only 340 mA of idle current with all outputs enabled. The channel switching is performed via a double-buffered, serial digital control (which can accommodate daisy-chaining of several devices), or via a parallel control, allowing updating of an individual output without reprogramming the entire array.

The AD8104/AD8105 are packaged in a 304-ball BGA package and are available over the extended industrial temperature range of −40°C to +85°C.

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6/07—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±2.5 V at T_A = 25°C, $R_{L,\ diff}$ = 200 Ω, V_{OCM} = 0 V, differential I/O mode, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	AD8104/AD8105 Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	200 mV p-p, typical channel		600		MHz
	2 V p-p, typical channel		420/525		MHz
Gain Flatness	0.1 dB, 200 mV p-p		100/50		MHz
	0.1 dB, 2 V p-p		70/50		MHz
Propagation Delay	2 V p-p		1.3		ns
Settling Time	1%, 2 V step		2.5		ns
Slew Rate	2 V step, peak		1800		V/µs
	2 V step, 10% to 90%		1500		V/µs
NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC or PAL, R_L = 150 Ω		0.05		%
Differential Phase Error	NTSC or PAL, R_L = 150 Ω		0.05		Degrees
Crosstalk, All Hostile	f = 5 MHz		−80/−70		dB
	f = 10 MHz		−72/−68		dB
	f = 100 MHz		−48/−50		dB
	f = 600 MHz		−40/−50		dB
Off Isolation, Input to Output	f = 5 MHz, one channel		−92		dB
Input Voltage Noise	0.1 MHz to 50 MHz		45/53		nV/√Hz
DC PERFORMANCE					
Voltage Gain	Differential		+1/+2		V/V
Gain Error			±1		%
	No load		±1	±3	%
Gain Matching	Channel-to-channel		±1		%
Differential Offset			±5	±25	mV
Common-Mode Offset			±25	±90	mV
OUTPUT CHARACTERISTICS					
Output Impedance	DC, enabled		0.1		Ω
	Disabled, differential		30		kΩ
Output Disable Capacitance	Disabled		4		pF
Output Leakage Current	Disabled		1		µA
Output Voltage Range	No load	2.8	3.8		V p-p
V_{OCM} Input Range	$V_{OUT,\ diff}$ = 2 V p-p	−0.5		+0.8	V
	$V_{OUT,\ diff}$ = 2.8 V p-p	−0.25		+0.6	V
Output Swing Limit	Single-ended output	−1.3		+1.3	V
Output Current	Maximum operating signal		30		mA
INPUT CHARACTERISTICS					
Input Voltage Range	Common mode, $V_{IN,\ diff}$ = 2 V p-p	−2		+2	V
	Differential		2/1		V
Common-Mode Rejection Ratio	f = 10 MHz		48		dB
Input Capacitance	Any switch configuration		2		pF
Input Resistance	Differential		5		kΩ
Input Offset Current			1		µA
V_{OCM} Input Bias Current			64		µA
V_{OCM} Input Impedance			4		kΩ

Parameter	Test Conditions/Comments	AD8104/AD8105 Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS					
Enable On Time	50% update to 1% settling		100		ns
Switching Time, 2 V Step	50% update to 1% settling		100		ns
Switching Transient (Glitch)	Differential		40		mV p-p
POWER SUPPLIES					
Supply Current	VPOS, outputs enabled, no load		340	420	mA
	VPOS, outputs disabled		210	240	mA
	VNEG, outputs enabled, no load		340	420	mA
	VNEG, outputs disabled		210	240	mA
	VDD, outputs enabled, no load			1.2	mA
Supply Voltage Range			4.5 to 5.5		V
PSRR	VNEG, VPOS, f = 1 MHz		85		dB
	VOCM, f = 1 MHz		75		dB
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (still air)		−40 to +85		°C
θ_{JA}	Operating (still air)		14		°C/W
θ_{JC}	Operating (still air)		1		°C/W

TIMING CHARACTERISTICS (SERIAL MODE)

Specifications subject to change without notice.

Table 2.

Parameter	Symbol	Limit Min	Limit Typ	Limit Max	Unit
Serial Data Setup Time	t_1	40			ns
$\overline{\text{CLK}}$ Pulse Width	t_2	50			ns
Serial Data Hold Time	t_3	50			ns
$\overline{\text{CLK}}$ Pulse Separation	t_4	150			ns
$\overline{\text{CLK}}$ to $\overline{\text{UPDATE}}$ Delay	t_5	10			ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	90			ns
$\overline{\text{CLK}}$ to DATA OUT Valid	t_7	120			ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off			100		ns
$\overline{\text{RESET}}$ Pulse Width		60			ns
$\overline{\text{RESET}}$ Time			200		ns

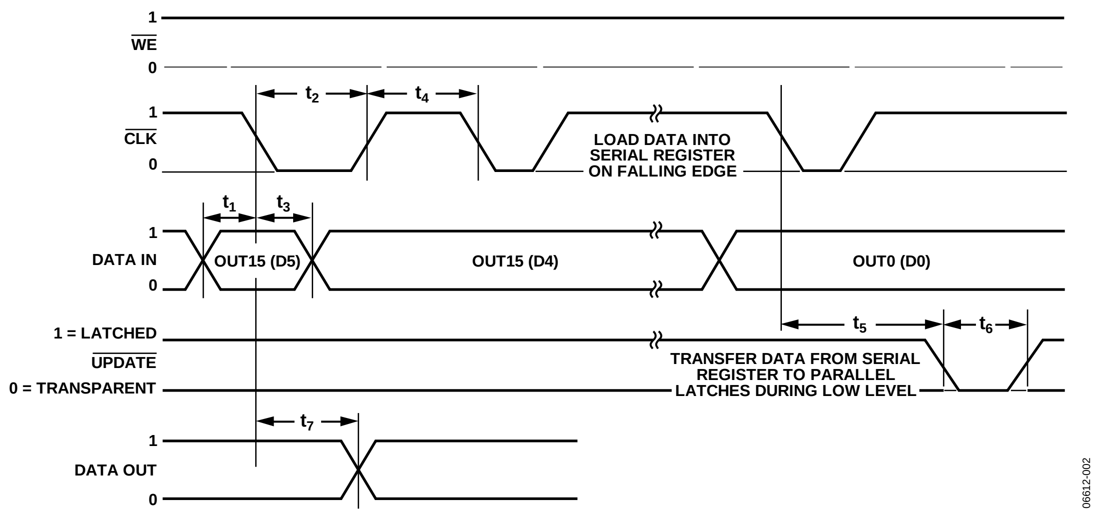

Figure 2. Timing Diagram, Serial Mode

Table 3. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, $\overline{\text{CLK}}$, DATA IN, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, $\overline{\text{CLK}}$, DATA IN, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	$\overline{\text{RESET}}$[1], $\overline{\text{SER}}$/PAR, $\overline{\text{CLK}}$, DATA IN, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$[1], $\overline{\text{SER}}$/PAR, $\overline{\text{CLK}}$, DATA IN, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.6 V max	VDD − 0.3 V min	DGND + 0.5 V max	1 μA max	−1 μA min	−1 mA max	1 mA min

[1] See Figure 15.

TIMING CHARACTERISTICS (PARALLEL MODE)

Specifications subject to change without notice.

Table 4.

Parameter	Symbol	Limit			Unit
		Min	**Typ**	**Max**	
Parallel Data Setup Time	t_1	80			ns
$\overline{\text{WE}}$ Pulse Width	t_2	110			ns
Parallel Data Hold Time	t_3	150			ns
$\overline{\text{WE}}$ Pulse Separation	t_4	90			ns
$\overline{\text{WE}}$ to $\overline{\text{UPDATE}}$ Delay	t_5	10			ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	90			ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off			100		ns
$\overline{\text{RESET}}$ Pulse Width		60			ns
$\overline{\text{RESET}}$ Time			200		ns

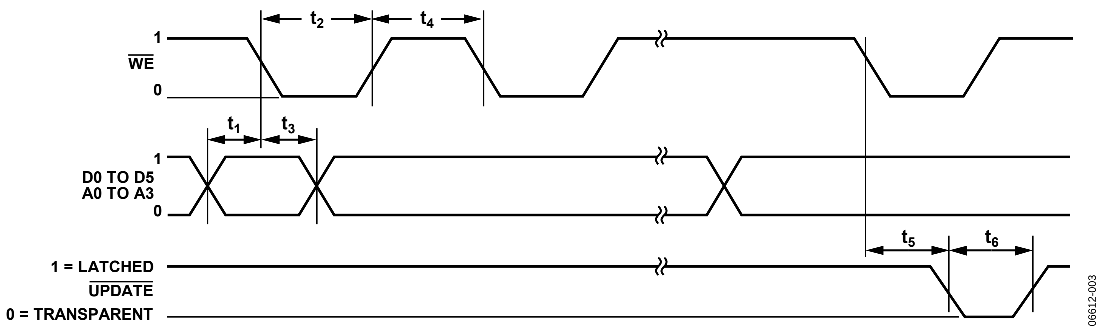

Figure 3. Timing Diagram, Parallel Mode

Table 5. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, $\overline{\text{WE}}$, D0, D1, D2, D3, D4, D5, A0, A1, A2, A3, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, $\overline{\text{WE}}$, D0, D1, D2, D3, D4, D5, A0, A1, A2, A3, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	$\overline{\text{RESET}}$[1], $\overline{\text{SER}}$/PAR, $\overline{\text{WE}}$, D0, D1, D2, D3, D4, D5, A0, A1, A2, A3, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$[1], $\overline{\text{SER}}$/PAR, $\overline{\text{WE}}$, D0, D1, D2, D3, D4, D5, A0, A1, A2, A3, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.6 V max	Disabled	Disabled	1 μA max	−1 μA min	Disabled	Disabled

[1] See Figure 15.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Supply Voltage (VPOS – VNEG)	6 V
Digital Supply Voltage (VDD – DGND)	6 V
Ground Potential Difference (VNEG – DGND)	+0.5 V to −2.5 V
Maximum Potential Difference (VDD – VNEG)	8 V
Common-Mode Analog Input Voltage	VNEG to VPOS
Differential Analog Input Voltage	±2 V
Digital Input Voltage	VDD
Output Voltage (Disabled Analog Output)	(VPOS − 1 V) to (VNEG + 1 V)
Output Short-Circuit Duration	Momentary
Output Short-Circuit Current	80 mA
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	θ_{JB}	ψ_{JT}	ψ_{JB}	Unit
304-Ball BGA	14	1	6.5	0.6	5.7	°C/W

POWER DISSIPATION

The AD8104/AD8105 are operated with ±2.5 V or +5 V supplies and can drive loads down to 100 Ω, resulting in a large range of possible power dissipations. For this reason, extra care must be taken derating the operating conditions based on ambient temperature.

Packaged in a 304-ball BGA, the AD8104/AD8105 junction-to-ambient thermal impedance (θ_{JA}) is 14°C/W. For long-term reliability, the maximum allowed junction temperature of the die should not exceed 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. The following curve shows the range of allowed internal die power dissipations that meet these conditions over the −40°C to +85°C ambient temperature range. When using Table 6, do not include external load power in the maximum power calculation, but do include load current dropped on the die output transistors.

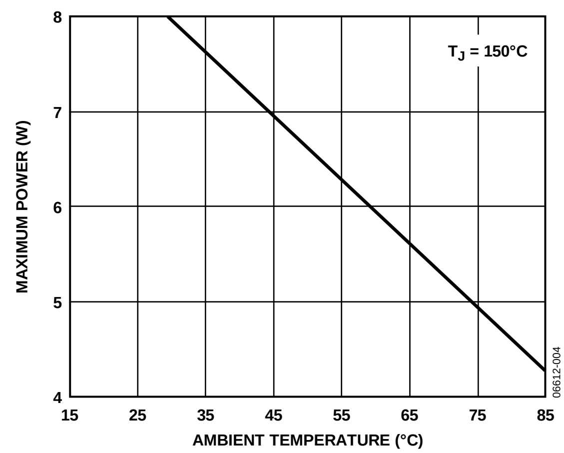

Figure 4. Maximum Die Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VPOS	VPOS	VPOS	VPOS	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VPOS	VPOS	VPOS	A
B	VPOS	VPOS	VPOS	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VPOS	VPOS	VPOS	VPOS	B
C	VPOS	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VPOS	C
D	IN16	VPOS	VPOS	VNEG	VOCM	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VOCM	VNEG	VPOS	IP0	VPOS	D
E	IP16	IN17	VNEG	VOCM																VOCM	VNEG	IN0	IP1	E
F	IN18	IP17	VNEG	VDD																VDD	VNEG	IP2	IN1	F
G	IP18	IN19	VNEG	DGND																DGND	VNEG	IN2	IP3	G
H	IN20	IP19	VNEG	$\overline{\text{RESET}}$																DATA OUT	VNEG	IP4	IN3	H
J	IP20	IN21	VNEG	$\overline{\text{UPDATE}}$																$\overline{\text{CLK}}$	VNEG	IN4	IP5	J
K	IN22	IP21	VNEG	$\overline{\text{WE}}$																DATA IN	VNEG	IP6	IN5	K
L	IP22	IN23	VPOS	D5																$\overline{\text{SER}}$/PAR	VPOS	IN6	IP7	L
M	IN24	IP23	VPOS	D4																DGND	VPOS	IP8	IN7	M
N	IP24	IN25	VPOS	D3																A3	VPOS	IN8	IP9	N
P	IN26	IP25	VNEG	D2																A2	VNEG	IP10	IN9	P
R	IP26	IN27	VNEG	D1																A1	VNEG	IN10	IP11	R
T	IN28	IP27	VNEG	D0																A0	VNEG	IP12	IN11	T
U	IP28	IN29	VNEG	VDD																VDD	VNEG	IN12	IP13	U
V	IN30	IP29	VNEG	DGND																DGND	VNEG	IP14	IN13	V
W	IP30	IN31	VNEG	VOCM																VOCM	VNEG	IN14	IP15	W
Y	VPOS	IP31	VPOS	VNEG	VOCM	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VOCM	VNEG	VPOS	VPOS	IN15	Y
AA	VPOS	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VPOS	AA
AB	VPOS	VPOS	VPOS	VPOS	ON14	OP14	ON12	OP12	ON10	OP10	ON8	OP8	ON6	OP6	ON4	OP4	ON2	OP2	ON0	OP0	VPOS	VPOS	VPOS	AB
AC	VPOS	VPOS	VPOS	ON15	OP15	ON13	OP13	ON11	OP11	ON9	OP9	ON7	OP7	ON5	OP5	ON3	OP3	ON1	OP1	VPOS	VPOS	VPOS	VPOS	AC
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

AD8104/AD8105

BOTTOM VIEW
(Not to Scale)

06612-005

Figure 5. 304-Ball BGA Pin Configuration (Bottom View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	VPOS	VPOS	VPOS	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VPOS	VPOS	VPOS	VPOS	A
B	VPOS	VPOS	VPOS	VPOS	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VPOS	VPOS	VPOS	B
C	VPOS	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VPOS	C
D	VPOS	IP0	VPOS	VNEG	VOCM	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VOCM	VNEG	VPOS	VPOS	IN16	D
E	IP1	IN0	VNEG	VOCM																VOCM	VNEG	IN17	IP16	E
F	IN1	IP2	VNEG	VDD																VDD	VNEG	IP17	IN18	F
G	IP3	IN2	VNEG	DGND																DGND	VNEG	IN19	IP18	G
H	IN3	IP4	VNEG	DATA OUT																$\overline{\text{RESET}}$	VNEG	IP19	IN20	H
J	IP5	IN4	VNEG	$\overline{\text{CLK}}$																$\overline{\text{UPDATE}}$	VNEG	IN21	IP20	J
K	IN5	IP6	VNEG	DATA IN																$\overline{\text{WE}}$	VNEG	IP21	IN22	K
L	IP7	IN6	VPOS	$\overline{\text{SER}}$/PAR																D5	VPOS	IN23	IP22	L
M	IN7	IP8	VPOS	DGND																D4	VPOS	IP23	IN24	M
N	IP9	IN8	VPOS	A3																D3	VPOS	IN25	IP24	N
P	IN9	IP10	VNEG	A2																D2	VNEG	IP25	IN26	P
R	IP11	IN10	VNEG	A1																D1	VNEG	IN27	IP26	R
T	IN11	IP12	VNEG	A0																D0	VNEG	IP27	IN28	T
U	IP13	IN12	VNEG	VDD																VDD	VNEG	IN29	IP28	U
V	IN13	IP14	VNEG	DGND																DGND	VNEG	IP29	IN30	V
W	IP15	IN14	VNEG	VOCM																VOCM	VNEG	IN31	IP30	W
Y	IN15	VPOS	VPOS	VNEG	VOCM	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VOCM	VNEG	VPOS	IP31	VPOS	Y
AA	VPOS	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VPOS	AA
AB	VPOS	VPOS	VPOS	OP0	ON0	OP2	ON2	OP4	ON4	OP6	ON6	OP8	ON8	OP10	ON10	OP12	ON12	OP14	ON14	VPOS	VPOS	VPOS	VPOS	AB
AC	VPOS	VPOS	VPOS	VPOS	OP1	ON1	OP3	ON3	OP5	ON5	OP7	ON7	OP9	ON9	OP11	ON11	OP13	ON13	OP15	ON15	VPOS	VPOS	VPOS	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

AD8104/AD8105

TOP VIEW
(Not to Scale)

06612-006

Figure 6. 304-Ball BGA Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VPOS	Analog Positive Power Supply.
A2	VPOS	Analog Positive Power Supply.
A3	VPOS	Analog Positive Power Supply.
A4	NC	No Connect.
A5	NC	No Connect.
A6	NC	No Connect.
A7	NC	No Connect.
A8	NC	No Connect.
A9	NC	No Connect.
A10	NC	No Connect.
A11	NC	No Connect.
A12	NC	No Connect.
A13	NC	No Connect.
A14	NC	No Connect.
A15	NC	No Connect.
A16	NC	No Connect.
A17	NC	No Connect.
A18	NC	No Connect.
A19	NC	No Connect.
A20	VPOS	Analog Positive Power Supply.
A21	VPOS	Analog Positive Power Supply.
A22	VPOS	Analog Positive Power Supply.
A23	VPOS	Analog Positive Power Supply.
B1	VPOS	Analog Positive Power Supply.
B2	VPOS	Analog Positive Power Supply.
B3	VPOS	Analog Positive Power Supply.
B4	VPOS	Analog Positive Power Supply.
B5	NC	No Connect.
B6	NC	No Connect.
B7	NC	No Connect.
B8	NC	No Connect.
B9	NC	No Connect.

Pin No.	Mnemonic	Description
B10	NC	No Connect.
B11	NC	No Connect.
B12	NC	No Connect.
B13	NC	No Connect.
B14	NC	No Connect.
B15	NC	No Connect.
B16	NC	No Connect.
B17	NC	No Connect.
B18	NC	No Connect.
B19	NC	No Connect.
B20	NC	No Connect.
B21	VPOS	Analog Positive Power Supply.
B22	VPOS	Analog Positive Power Supply.
B23	VPOS	Analog Positive Power Supply.
C1	VPOS	Analog Positive Power Supply.
C2	VPOS	Analog Positive Power Supply.
C3	VPOS	Analog Positive Power Supply.
C4	VPOS	Analog Positive Power Supply.
C5	VNEG	Analog Negative Power Supply.
C6	VNEG	Analog Negative Power Supply.
C7	VNEG	Analog Negative Power Supply.
C8	VNEG	Analog Negative Power Supply.
C9	VNEG	Analog Negative Power Supply.
C10	VNEG	Analog Negative Power Supply.
C11	VPOS	Analog Positive Power Supply.
C12	VPOS	Analog Positive Power Supply.
C13	VPOS	Analog Positive Power Supply.
C14	VNEG	Analog Negative Power Supply.
C15	VNEG	Analog Negative Power Supply.
C16	VNEG	Analog Negative Power Supply.
C17	VNEG	Analog Negative Power Supply.
C18	VNEG	Analog Negative Power Supply.
C19	VNEG	Analog Negative Power Supply.
C20	VPOS	Analog Positive Power Supply.
C21	VPOS	Analog Positive Power Supply.
C22	VPOS	Analog Positive Power Supply.
C23	VPOS	Analog Positive Power Supply.
D1	VPOS	Analog Positive Power Supply.
D2	IP0	Input Number 0, Positive Phase.
D3	VPOS	Analog Positive Power Supply.
D4	VNEG	Analog Negative Power Supply.
D5	VOCM	Output Common-Mode Reference Supply.
D6	VNEG	Analog Negative Power Supply.
D7	VNEG	Analog Negative Power Supply.
D8	VNEG	Analog Negative Power Supply.
D9	VNEG	Analog Negative Power Supply.
D10	VNEG	Analog Negative Power Supply.
D11	VPOS	Analog Positive Power Supply.
D12	VPOS	Analog Positive Power Supply.
D13	VPOS	Analog Positive Power Supply.
D14	VNEG	Analog Negative Power Supply.
D15	VNEG	Analog Negative Power Supply.

Pin No.	Mnemonic	Description
D16	VNEG	Analog Negative Power Supply.
D17	VNEG	Analog Negative Power Supply.
D18	VNEG	Analog Negative Power Supply.
D19	VOCM	Output Common-Mode Reference Supply.
D20	VNEG	Analog Negative Power Supply.
D21	VPOS	Analog Positive Power Supply.
D22	VPOS	Analog Positive Power Supply.
D23	IN16	Input Number 16, Negative Phase.
E1	IP1	Input Number 1, Positive Phase.
E2	IN0	Input Number 0, Negative Phase.
E3	VNEG	Analog Negative Power Supply.
E4	VOCM	Output Common-Mode Reference Supply.
E20	VOCM	Output Common-Mode Reference Supply.
E21	VNEG	Analog Negative Power Supply.
E22	IN17	Input Number 17, Negative Phase.
E23	IP16	Input Number 16, Positive Phase.
F1	IN1	Input Number 1, Negative Phase.
F2	IP2	Input Number 2, Positive Phase.
F3	VNEG	Analog Negative Power Supply.
F4	VDD	Logic Positive Power Supply.
F20	VDD	Logic Positive Power Supply.
F21	VNEG	Analog Negative Power Supply.
F22	IP17	Input Number 17, Positive Phase.
F23	IN18	Input Number 18, Negative Phase.
G1	IP3	Input Number 3, Positive Phase.
G2	IN2	Input Number 2, Negative Phase.
G3	VNEG	Analog Negative Power Supply.
G4	DGND	Logic Negative Power Supply.
G20	DGND	Logic Negative Power Supply.
G21	VNEG	Analog Negative Power Supply.
G22	IN19	Input Number 19, Negative Phase.
G23	IP18	Input Number 18, Positive Phase.
H1	IN3	Input Number 3, Negative Phase.
H2	IP4	Input Number 4, Positive Phase.
H3	VNEG	Analog Negative Power Supply.
H4	DATA OUT	Control Pin: Serial Data Out.
H20	$\overline{\text{RESET}}$	Control Pin: Second Rank Data Reset.
H21	VNEG	Analog Negative Power Supply.
H22	IP19	Input Number 19, Positive Phase.
H23	IN20	Input Number 20, Negative Phase.
J1	IP5	Input Number 5, Positive Phase.
J2	IN4	Input Number 4, Negative Phase.
J3	VNEG	Analog Negative Power Supply.
J4	$\overline{\text{CLK}}$	Control Pin: Serial Data Clock.
J20	$\overline{\text{UPDATE}}$	Control Pin: Second Rank Write Strobe.
J21	VNEG	Analog Negative Power Supply.
J22	IN21	Input Number 21, Negative Phase.
J23	IP20	Input Number 20, Positive Phase.
K1	IN5	Input Number 5, Negative Phase.

Pin No.	Mnemonic	Description
K2	IP6	Input Number 6, Positive Phase.
K3	VNEG	Analog Negative Power Supply.
K4	DATA IN	Control Pin: Serial Data In.
K20	$\overline{\text{WE}}$	Control Pin: First Rank Write Strobe.
K21	VNEG	Analog Negative Power Supply.
K22	IP21	Input Number 21, Positive Phase.
K23	IN22	Input Number 22, Negative Phase.
L1	IP7	Input Number 7, Positive Phase.
L2	IN6	Input Number 6, Negative Phase.
L3	VPOS	Analog Positive Power Supply.
L4	$\overline{\text{SER}}$/PAR	Control Pin: Serial/Parallel Mode Select.
L20	D5	Control Pin: Input Address Bit 5.
L21	VPOS	Analog Positive Power Supply.
L22	IN23	Input Number 23, Negative Phase.
L23	IP22	Input Number 22, Positive Phase.
M1	IN7	Input Number 7, Negative Phase.
M2	IP8	Input Number 8, Positive Phase.
M3	VPOS	Analog Positive Power Supply.
M4	DGND	Logic Negative Power Supply
M20	D4	Control Pin: Input Address Bit 4.
M21	VPOS	Analog Positive Power Supply.
M22	IP23	Input Number 23, Positive Phase.
M23	IN24	Input Number 24, Negative Phase.
N1	IP9	Input Number 9, Positive Phase.
N2	IN8	Input Number 8, Negative Phase.
N3	VPOS	Analog Positive Power Supply.
N4	A3	Control Pin: Output Address Bit 3.
N20	D3	Control Pin: Input Address Bit 3.
N21	VPOS	Analog Positive Power Supply.
N22	IN25	Input Number 25, Negative Phase.
N23	IP24	Input Number 24, Positive Phase.
P1	IN9	Input Number 9, Negative Phase.
P2	IP10	Input Number 10, Positive Phase.
P3	VNEG	Analog Negative Power Supply.
P4	A2	Control Pin: Output Address Bit 2.
P20	D2	Control Pin: Input Address Bit 2.
P21	VNEG	Analog Negative Power Supply.
P22	IP25	Input Number 25, Positive Phase.
P23	IN26	Input Number 26, Negative Phase.
R1	IP11	Input Number 11, Positive Phase.
R2	IN10	Input Number 10, Negative Phase.
R3	VNEG	Analog Negative Power Supply.
R4	A1	Control Pin: Output Address Bit 1.
R20	D1	Control Pin: Input Address Bit 1.
R21	VNEG	Analog Negative Power Supply.
R22	IN27	Input Number 27, Negative Phase.
R23	IP26	Input Number 26, Positive Phase.
T1	IN11	Input Number 11, Negative Phase.
T2	IP12	Input Number 12, Positive Phase.
T3	VNEG	Analog Negative Power Supply.
T4	A0	Control Pin: Output Address Bit 0.
T20	D0	Control Pin: Input Address Bit 0.

Pin No.	Mnemonic	Description
T21	VNEG	Analog Negative Power Supply.
T22	IP27	Input Number 27, Positive Phase.
T23	IN28	Input Number 28, Negative Phase.
U1	IP13	Input Number 13, Positive Phase.
U2	IN12	Input Number 12, Negative Phase.
U3	VNEG	Analog Negative Power Supply.
U4	VDD	Logic Positive Power Supply.
U20	VDD	Logic Positive Power Supply.
U21	VNEG	Analog Negative Power Supply.
U22	IN29	Input Number 29, Negative Phase.
U23	IP28	Input Number 28, Positive Phase.
V1	IN13	Input Number 13, Negative Phase.
V2	IP14	Input Number 14, Positive Phase.
V3	VNEG	Analog Negative Power Supply.
V4	DGND	Logic Negative Power Supply.
V20	DGND	Logic Negative Power Supply.
V21	VNEG	Analog Negative Power Supply.
V22	IP29	Input Number 29, Positive Phase.
V23	IN30	Input Number 30, Negative Phase.
W1	IP15	Input Number 15, Positive Phase.
W2	IN14	Input Number 14, Negative Phase.
W3	VNEG	Analog Negative Power Supply.
W4	VOCM	Output Common-Mode Reference Supply.
W20	VOCM	Output Common-Mode Reference Supply.
W21	VNEG	Analog Negative Power Supply.
W22	IN31	Input Number 31, Negative Phase.
W23	IP30	Input Number 30, Positive Phase.
Y1	IN15	Input Number 15, Negative Phase.
Y2	VPOS	Analog Positive Power Supply.
Y3	VPOS	Analog Positive Power Supply.
Y4	VNEG	Analog Negative Power Supply.
Y5	VOCM	Output Common-Mode Reference Supply.
Y6	VNEG	Analog Negative Power Supply.
Y7	VNEG	Analog Negative Power Supply.
Y8	VNEG	Analog Negative Power Supply.
Y9	VNEG	Analog Negative Power Supply.
Y10	VNEG	Analog Negative Power Supply.
Y11	VPOS	Analog Positive Power Supply.
Y12	VPOS	Analog Positive Power Supply.
Y13	VPOS	Analog Positive Power Supply.
Y14	VNEG	Analog Negative Power Supply.
Y15	VNEG	Analog Negative Power Supply.
Y16	VNEG	Analog Negative Power Supply.
Y17	VNEG	Analog Negative Power Supply.
Y18	VNEG	Analog Negative Power Supply.
Y19	VOCM	Output Common-Mode Reference Supply.
Y20	VNEG	Analog Negative Power Supply.
Y21	VPOS	Analog Positive Power Supply.
Y22	IP31	Input Number 31, Positive Phase.

Pin No.	Mnemonic	Description
Y23	VPOS	Analog Positive Power Supply.
AA1	VPOS	Analog Positive Power Supply.
AA2	VPOS	Analog Positive Power Supply.
AA3	VPOS	Analog Positive Power Supply.
AA4	VPOS	Analog Positive Power Supply.
AA5	VNEG	Analog Negative Power Supply.
AA6	VNEG	Analog Negative Power Supply.
AA7	VNEG	Analog Negative Power Supply.
AA8	VNEG	Analog Negative Power Supply.
AA9	VNEG	Analog Negative Power Supply.
AA10	VNEG	Analog Negative Power Supply.
AA11	VPOS	Analog Positive Power Supply.
AA12	VPOS	Analog Positive Power Supply.
AA13	VPOS	Analog Positive Power Supply.
AA14	VNEG	Analog Negative Power Supply.
AA15	VNEG	Analog Negative Power Supply.
AA16	VNEG	Analog Negative Power Supply.
AA17	VNEG	Analog Negative Power Supply.
AA18	VNEG	Analog Negative Power Supply.
AA19	VNEG	Analog Negative Power Supply.
AA20	VPOS	Analog Positive Power Supply.
AA21	VPOS	Analog Positive Power Supply.
AA22	VPOS	Analog Positive Power Supply.
AA23	VPOS	Analog Positive Power Supply.
AB1	VPOS	Analog Positive Power Supply.
AB2	VPOS	Analog Positive Power Supply.
AB3	VPOS	Analog Positive Power Supply.
AB4	OP0	Output Number 0, Positive Phase.
AB5	ON0	Output Number 0, Negative Phase.
AB6	OP2	Output Number 2, Positive Phase.
AB7	ON2	Output Number 2, Negative Phase.
AB8	OP4	Output Number 4, Positive Phase.
AB9	ON4	Output Number 4, Negative Phase.
AB10	OP6	Output Number 6, Positive Phase.
AB11	ON6	Output Number 6, Negative Phase.
AB12	OP8	Output Number 8, Positive Phase.
AB13	ON8	Output Number 8, Negative Phase.
AB14	OP10	Output Number 10, Positive Phase.
AB15	ON10	Output Number 10, Negative Phase.
AB16	OP12	Output Number 12, Positive Phase.
AB17	ON12	Output Number 12, Negative Phase.
AB18	OP14	Output Number 14, Positive Phase.
AB19	ON14	Output Number 14, Negative Phase.
AB20	VPOS	Analog Positive Power Supply.
AB21	VPOS	Analog Positive Power Supply.
AB22	VPOS	Analog Positive Power Supply.
AB23	VPOS	Analog Positive Power Supply.
AC1	VPOS	Analog Positive Power Supply.
AC2	VPOS	Analog Positive Power Supply.
AC3	VPOS	Analog Positive Power Supply.
AC4	VPOS	Analog Positive Power Supply.
AC5	OP1	Output Number 1, Positive Phase.
AC6	ON1	Output Number 1, Negative Phase.
AC7	OP3	Output Number 3, Positive Phase.
AC8	ON3	Output Number 3, Negative Phase.
AC9	OP5	Output Number 5, Positive Phase.
AC10	ON5	Output Number 5, Negative Phase.
AC11	OP7	Output Number 7, Positive Phase.
AC12	ON7	Output Number 7, Negative Phase.
AC13	OP9	Output Number 9, Positive Phase.
AC14	ON9	Output Number 9, Negative Phase.
AC15	OP11	Output Number 11, Positive Phase.
AC16	ON11	Output Number 11, Negative Phase.
AC17	OP13	Output Number 13, Positive Phase.
AC18	ON13	Output Number 13, Negative Phase.
AC19	OP15	Output Number 15, Positive Phase.
AC20	ON15	Output Number 15, Negative Phase.
AC21	VPOS	Analog Positive Power Supply.
AC22	VPOS	Analog Positive Power Supply.
AC23	VPOS	Analog Positive Power Supply.

TRUTH TABLE AND LOGIC DIAGRAM

Table 9. Operation Truth Table

$\overline{\text{WE}}$	$\overline{\text{UPDATE}}$	$\overline{\text{CLK}}$	Data Input	Data Output	$\overline{\text{RESET}}$	$\overline{\text{SER}}$/PAR	Operation/Comment
X	X	X	X	X	0	X	Asynchronous reset. All outputs are disabled. Remainder of logic in 192-bit shift register is unchanged.
1	X	↓	Data$_i$[1]	Data$_{i-192}$	1	0	Serial mode. The data on the serial DATA IN line is loaded into the serial register. The first bit clocked into the serial register appears at DATA OUT 192 clock cycles later.
0	X	X	D0…D5[2] A0…A3[3]	Not applicable in parallel mode	1	1	Parallel mode. The data on parallel lines D0 to D5 are loaded into the shift register location addressed by A0 to A3.
1	0	X	X	Not applicable in parallel mode	1	X	Switch matrix update. Data in the 192-bit shift register transfers into the parallel latches that control the switch array.
1	X	X	X	X	1	1	No change in logic.

1 Data$_i$: serial data.
2 D0…D5: data bits.
3 A0…A3: address bits.

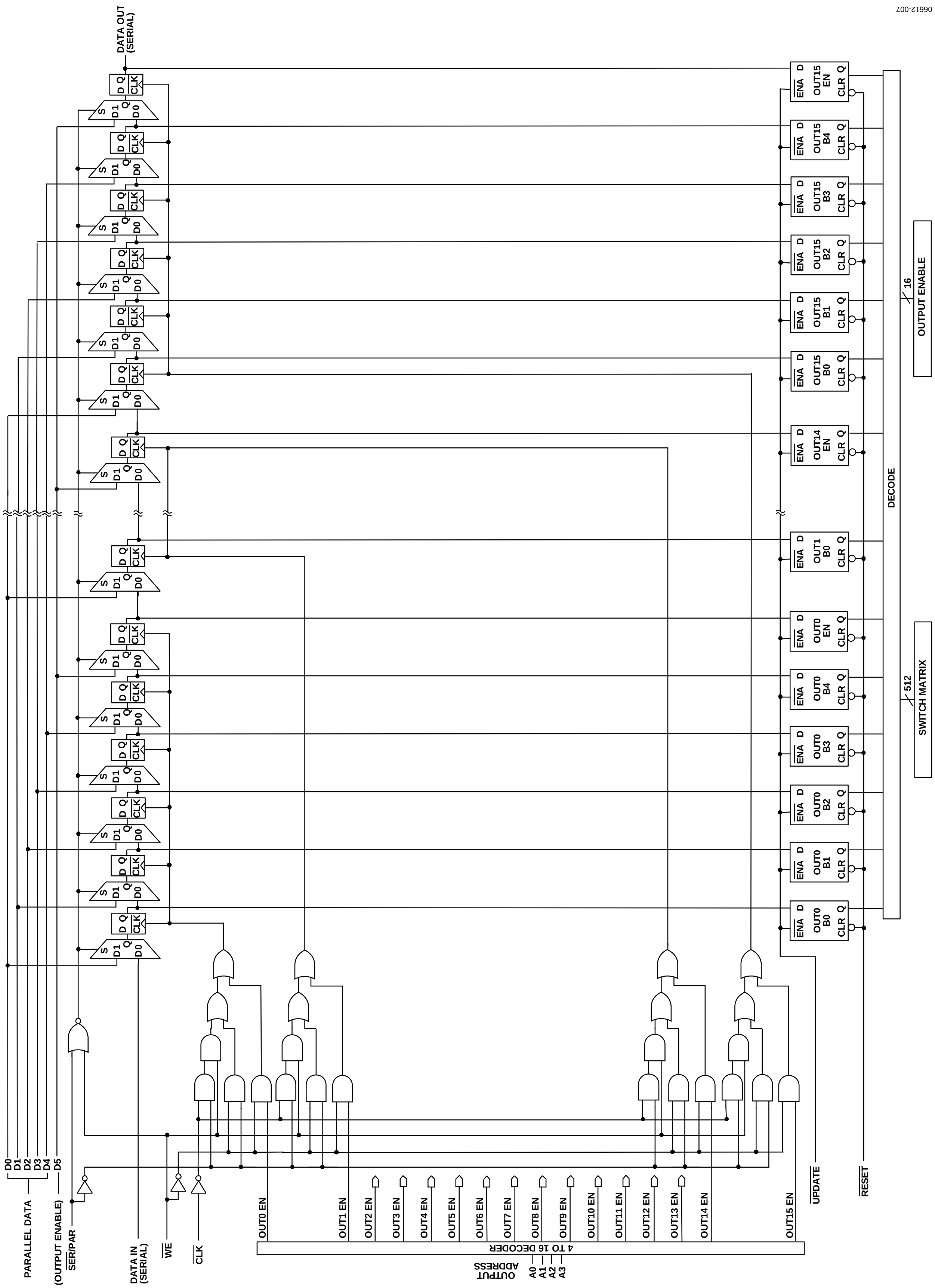

Figure 7. Logic Diagram

I/O SCHEMATICS

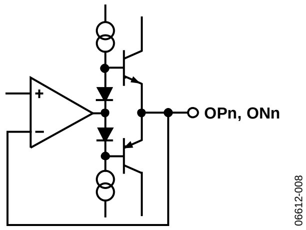

Figure 8. AD8104/AD8105 Enabled Output (see also ESD Protection Map, Figure 18)

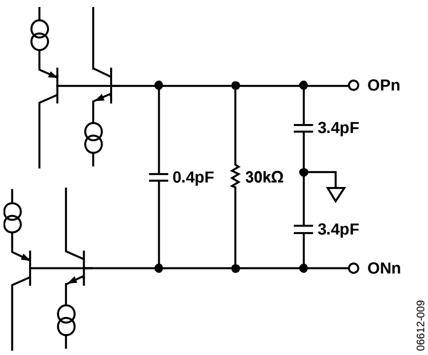

Figure 9. AD8104/AD8105 Disabled Output (see also ESD Protection Map, Figure 18)

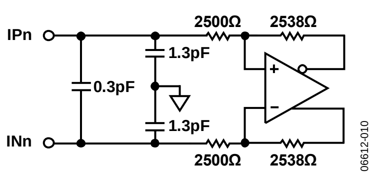

Figure 10. AD8104 Receiver (see also ESD Protection Map, Figure 18)

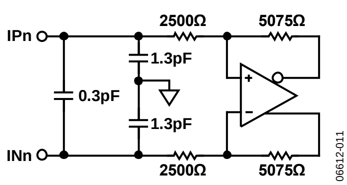

Figure 11. AD8105 Receiver (see also ESD Protection Map, Figure 18)

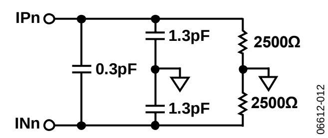

Figure 12. AD8104/AD8105 Receiver Simplified Equivalent Circuit When Driving Differentially

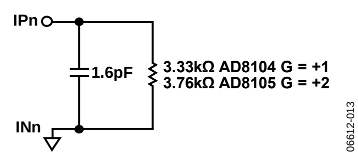

Figure 13. AD8104/AD8105 Receiver Simplified Equivalent Circuit When Driving Single-Ended

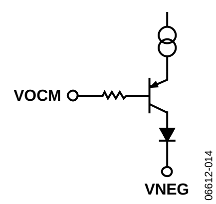

Figure 14. VOCM Input (see also ESD Protection Map, Figure 18)

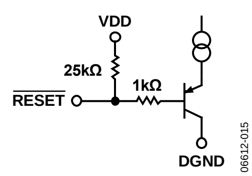

Figure 15. Reset Input (see also ESD Protection Map, Figure 18)

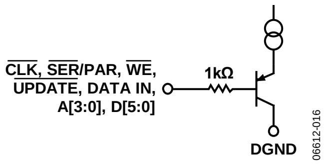

Figure 16. Logic Input (see also ESD Protection Map, Figure 18)

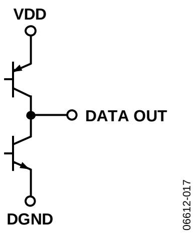

Figure 17. Logic Output (see also ESD Protection Map, Figure 18)

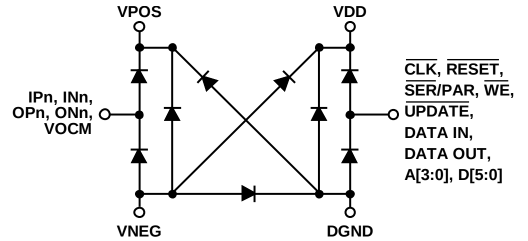

Figure 18. ESD Protection Map

TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm 2.5$ V at $T_A = 25°C$, $R_{L,\,diff} = 200\ \Omega$, $V_{OCM} = 0$ V, differential I/O mode, unless otherwise noted.

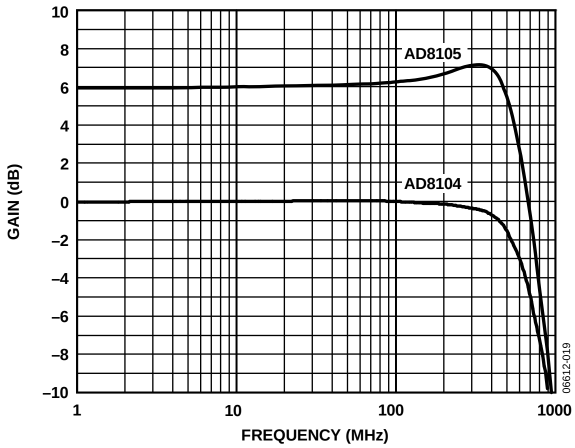

Figure 19. AD8104, AD8105 Small Signal Frequency Response, 200 mV p-p

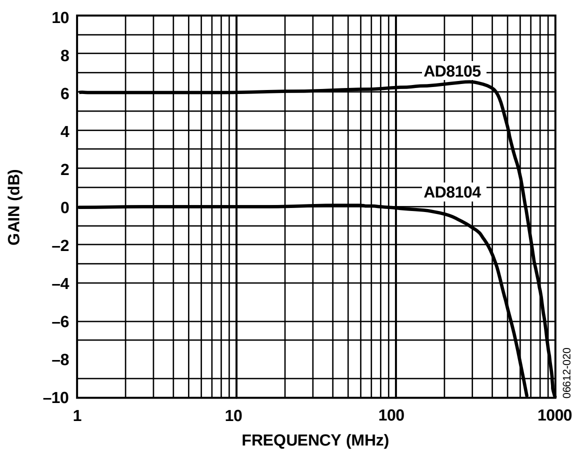

Figure 20. AD8104, AD8105 Large Signal Frequency Response, 2 V p-p

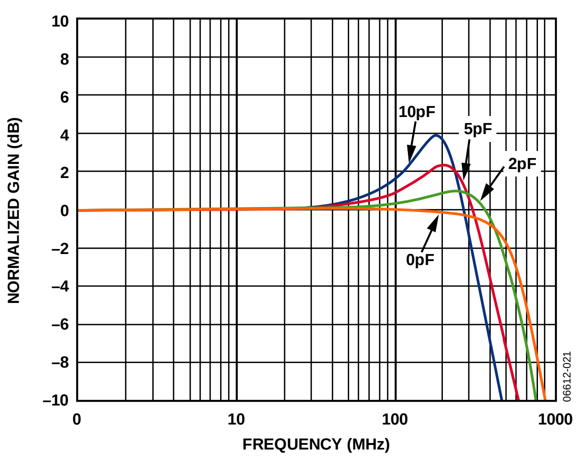

Figure 21. AD8104 Small Signal Frequency Response with Capacitive Loads, 200 mV p-p

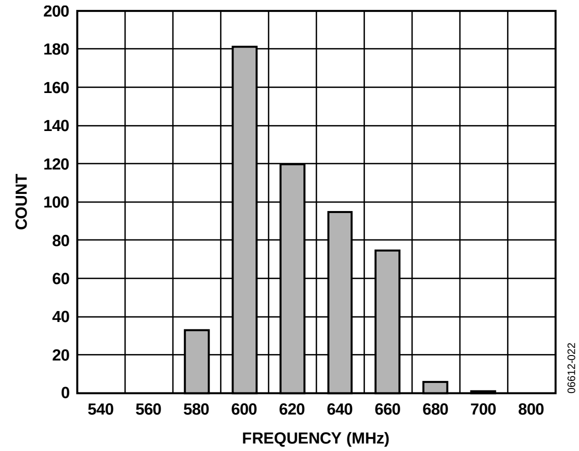

Figure 22. AD8104 −3 dB Bandwidth Histogram, One Device, All 512 Channels

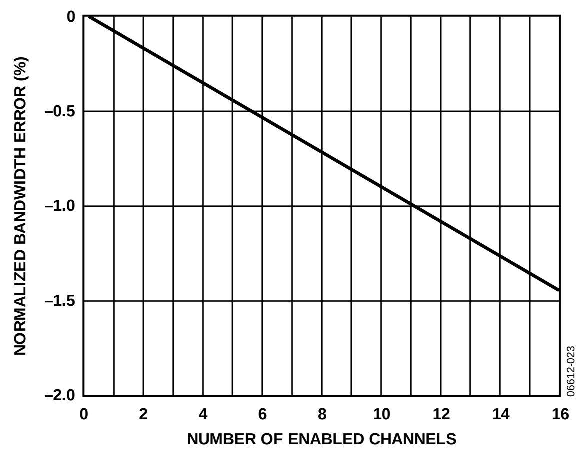

Figure 23. AD8104 Bandwidth Error vs. Enabled Channels

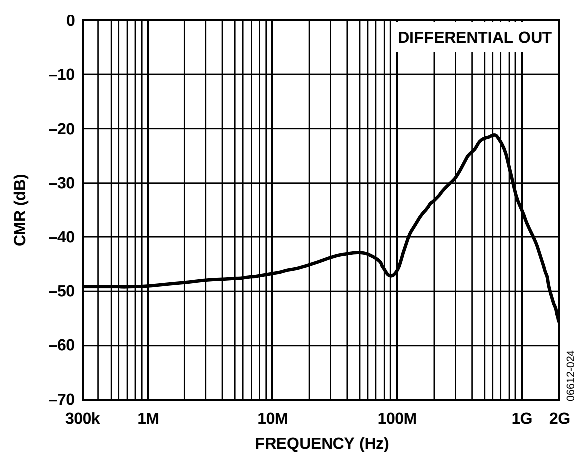

Figure 24. AD8104, AD8105 Common-Mode Rejection

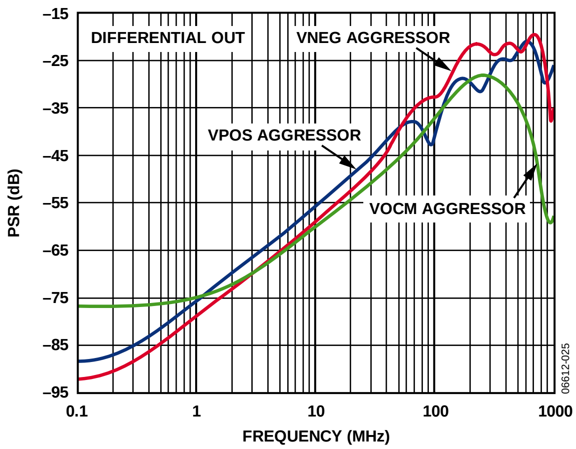

Figure 25. AD8104 Power Supply Rejection

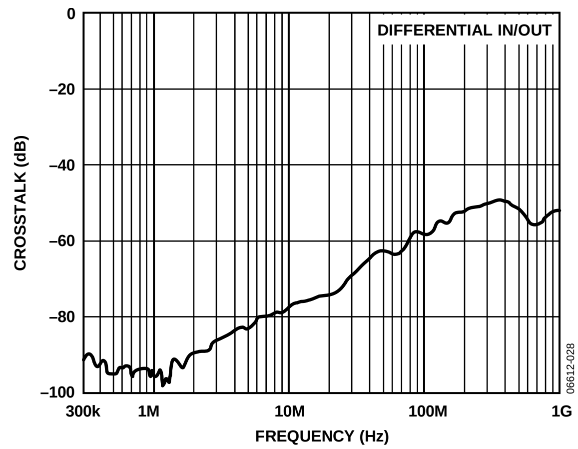

Figure 28. AD8104 Crosstalk, One Adjacent Channel

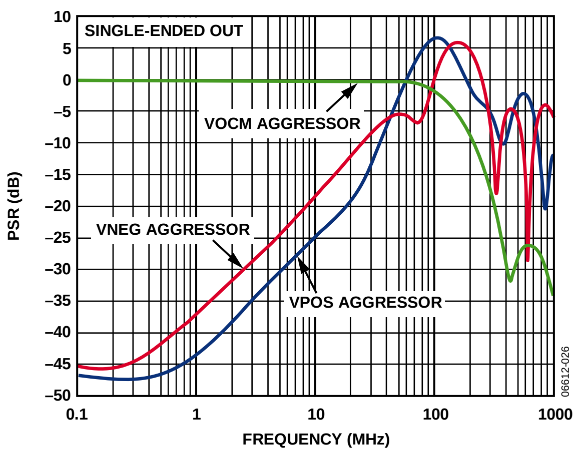

Figure 26. AD8104 Power Supply Rejection, Single-Ended

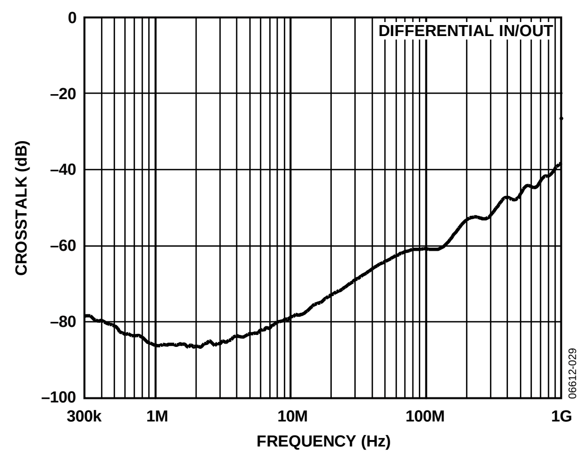

Figure 29. AD8105 Crosstalk, One Adjacent Channel

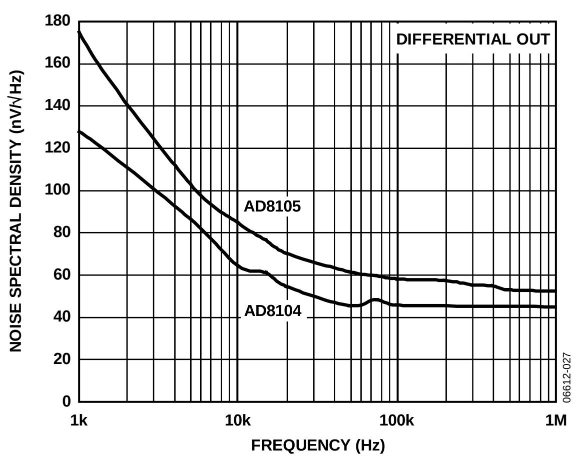

Figure 27. AD8104, AD8105 Noise Spectral Density, RTO

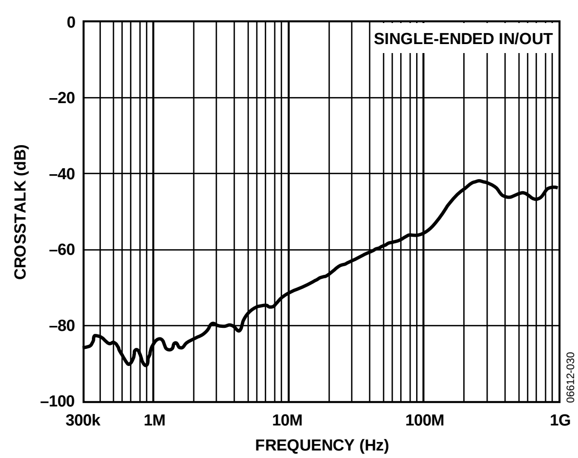

Figure 30. AD8104 Crosstalk, One Adjacent Channel, Single-Ended

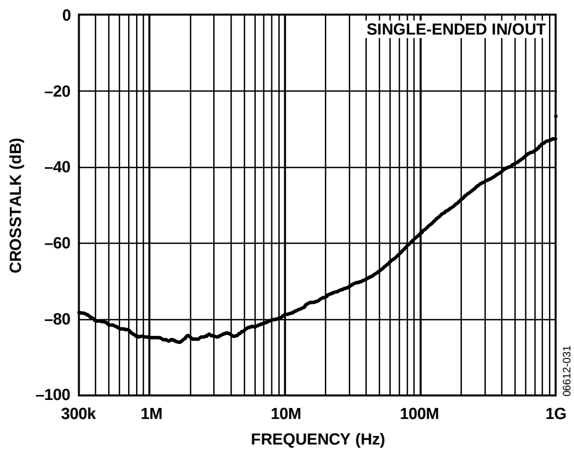

Figure 31. AD8105 Crosstalk, One Adjacent Channel, Single-Ended

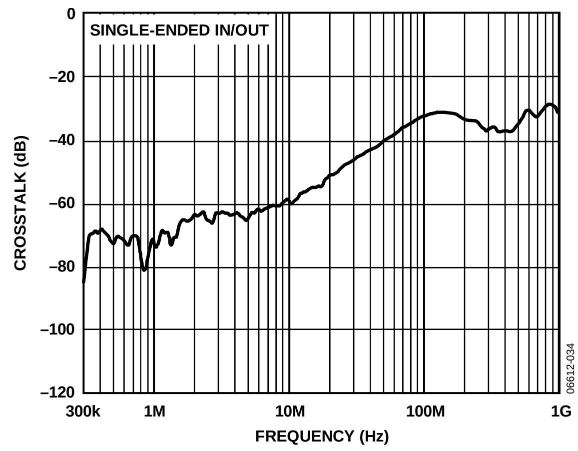

Figure 34. AD8104 Crosstalk, All Hostile, Single-Ended

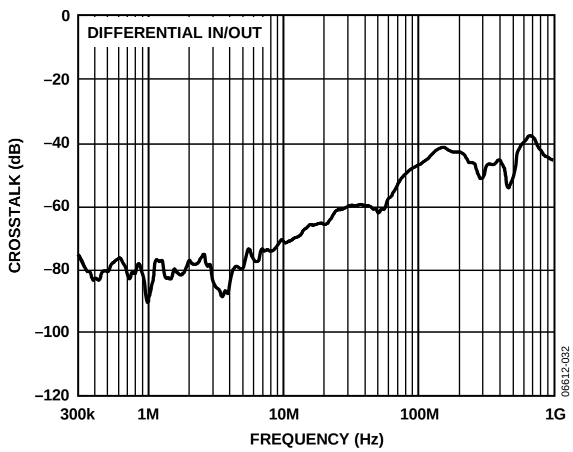

Figure 32. AD8104 Crosstalk, All Hostile

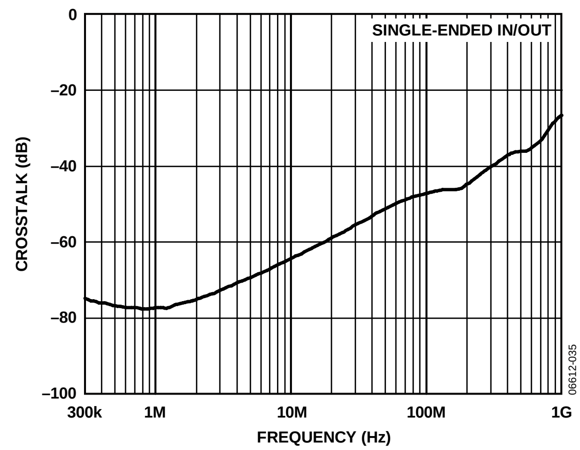

Figure 35. AD8105 Crosstalk, All Hostile, Single-Ended

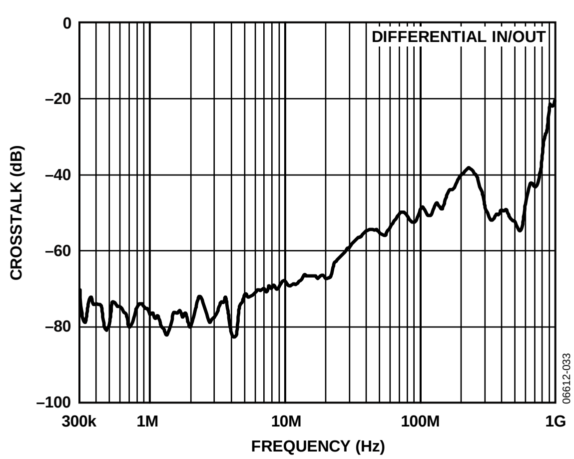

Figure 33. AD8105 Crosstalk, All Hostile

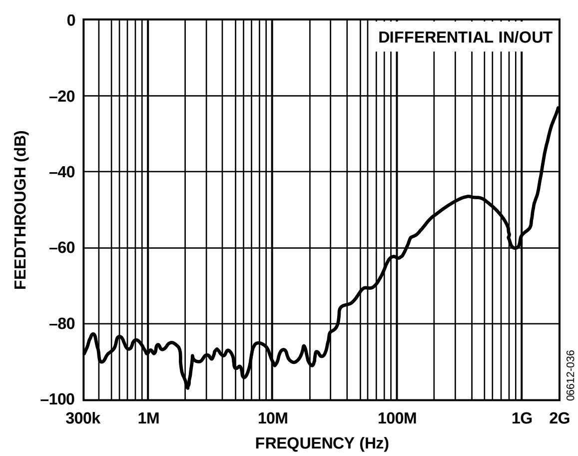

Figure 36. AD8104 Crosstalk, Off Isolation

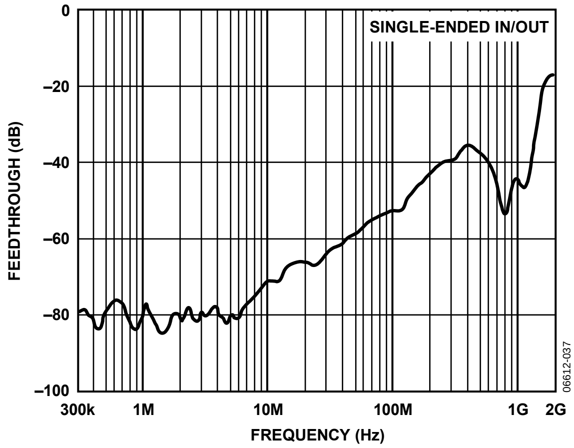

Figure 37. AD8104 Crosstalk, Off Isolation, Single-Ended

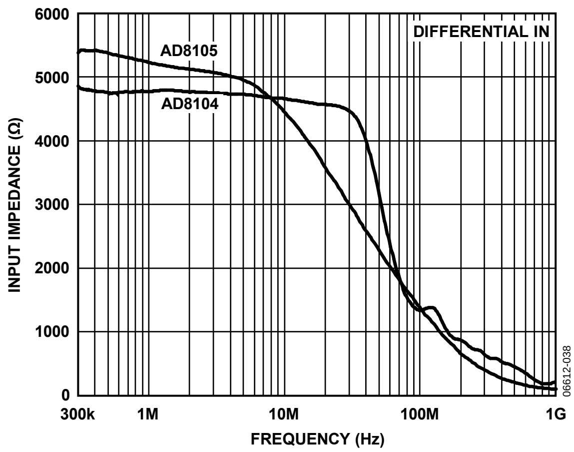

Figure 38. AD8104, AD8105 Input Impedance

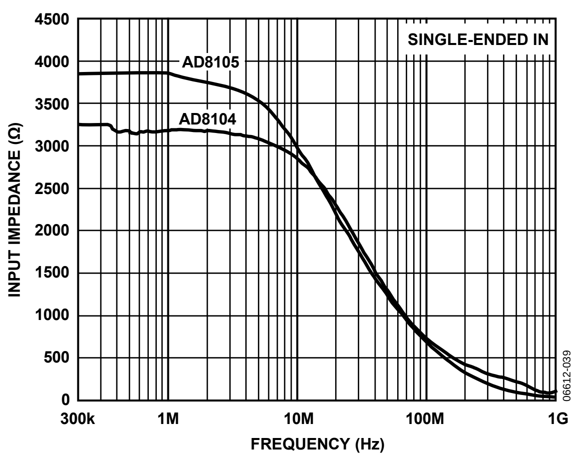

Figure 39. AD8104, AD8105 Input Impedance, Single-Ended

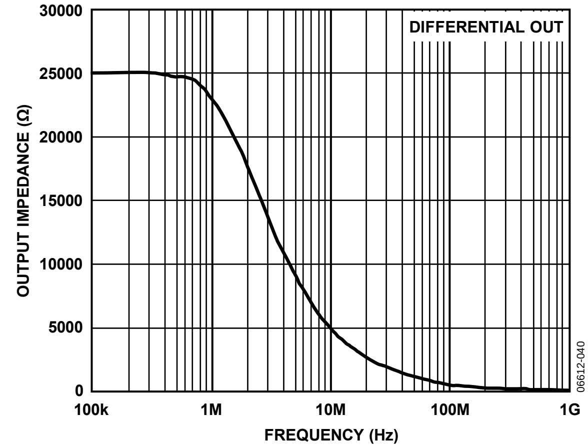

Figure 40. AD8104, AD8105 Output Impedance, Disabled

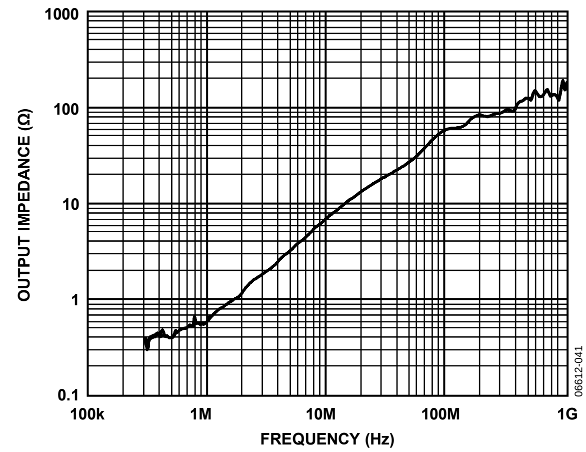

Figure 41. AD8104, AD8105 Output Impedance, Enabled

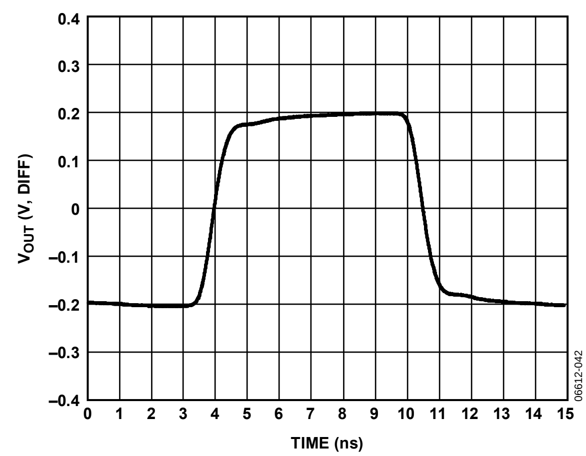

Figure 42. AD8104 Small Signal Pulse Response, 200 mV p-p

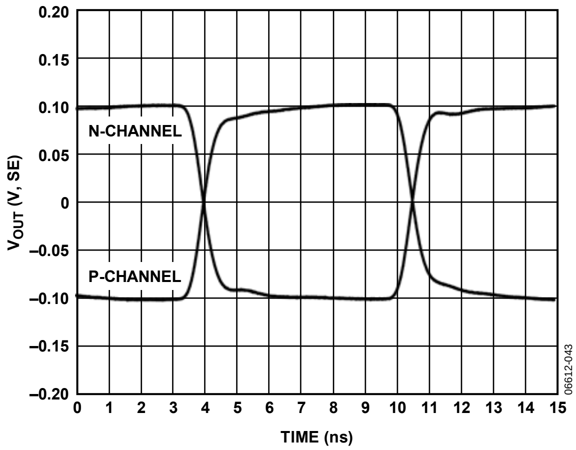

Figure 43. AD8104 Small Signal Pulse Response, Single-Ended, 200 mV p-p

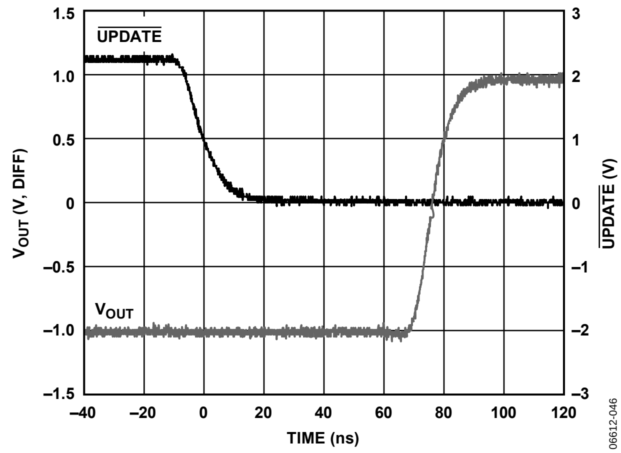

Figure 46. AD8104 Switching Time

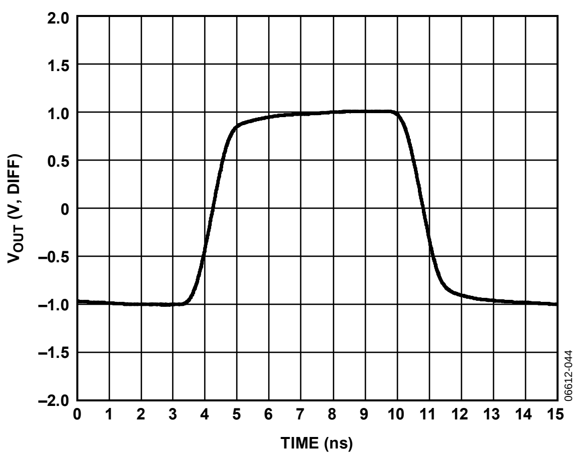

Figure 44. AD8104 Large Signal Pulse Response, 2 V p-p

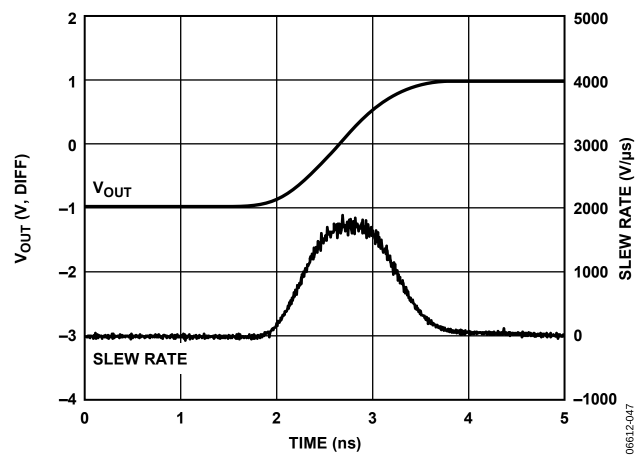

Figure 47. AD8104 Large Signal Rising Edge and Slew Rate

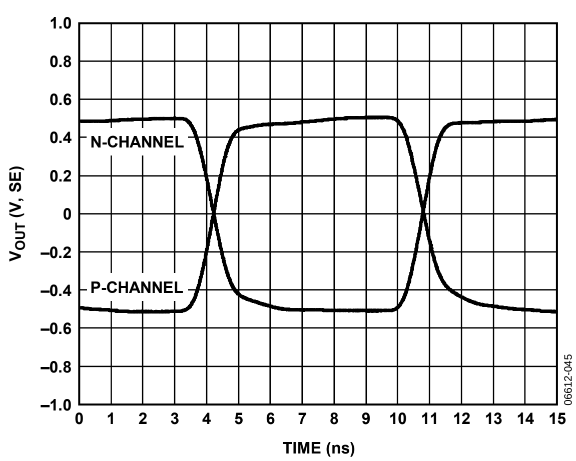

Figure 45. AD8104 Large Signal Pulse Response, Single-Ended, 2 V p-p

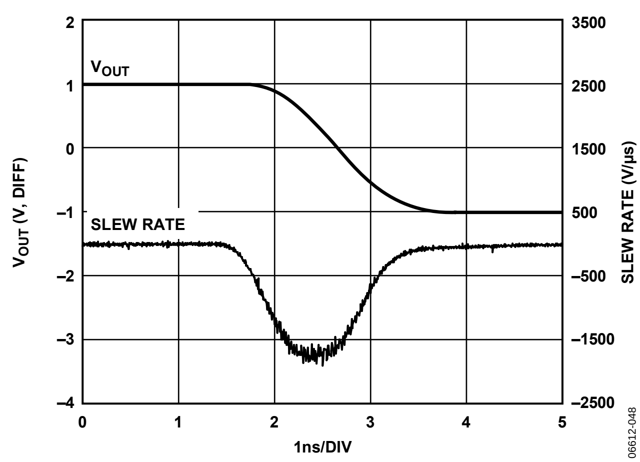

Figure 48. AD8104 Large Signal Falling Edge and Slew Rate

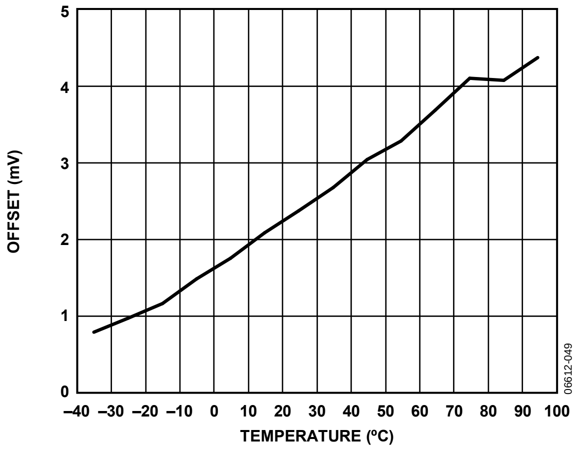

Figure 49. AD8104 V_{OS} vs. Temperature with All Outputs Enabled

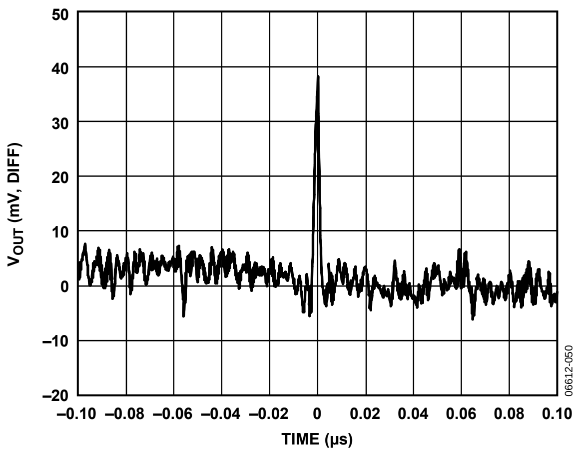

Figure 50. AD8104 Switching Transient (Glitch)

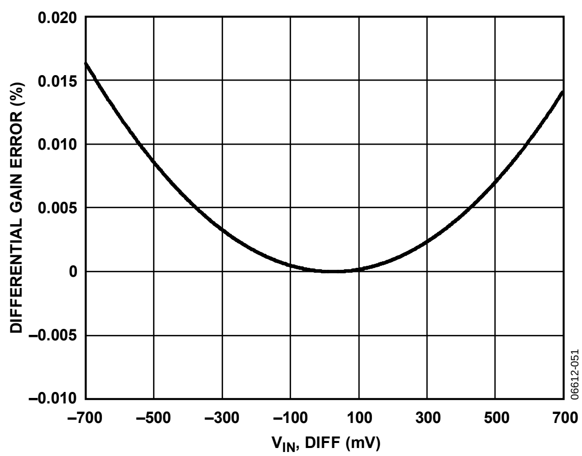

Figure 51. AD8104 Gain vs. DC Voltage, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 600 mV p-p, Differential

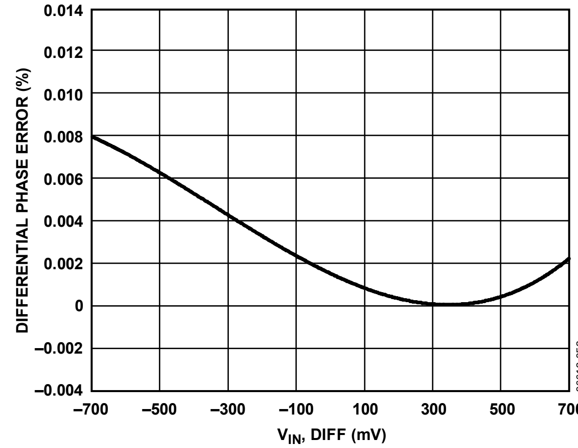

Figure 52. AD8104 Phase vs. DC Voltage, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 600 mV p-p, Differential

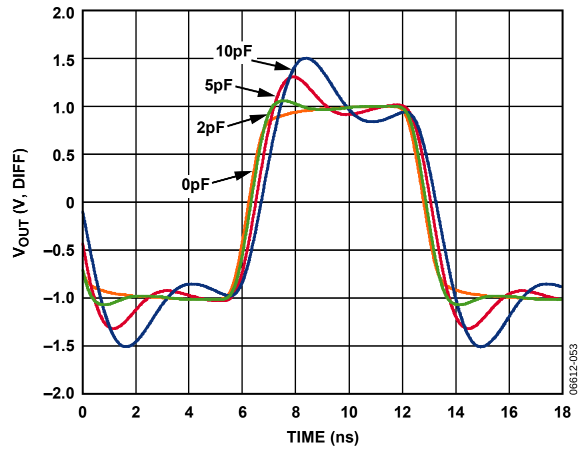

Figure 53. AD8104 Large Signal Pulse Response with Capacitive Loads

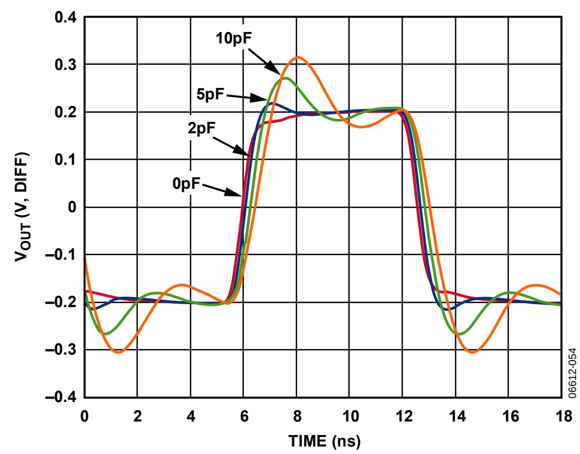

Figure 54. AD8104 Small Signal Pulse Response with Capacitive Loads

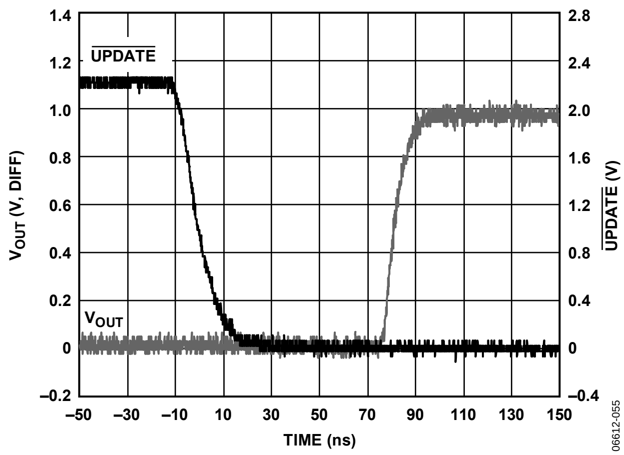

Figure 55. AD8104 Enable Time

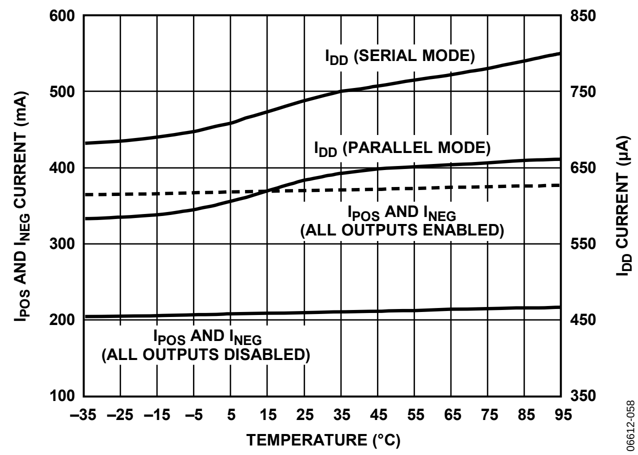

Figure 58. AD8104, AD8105 Quiescent Supply Currents vs. Temperature

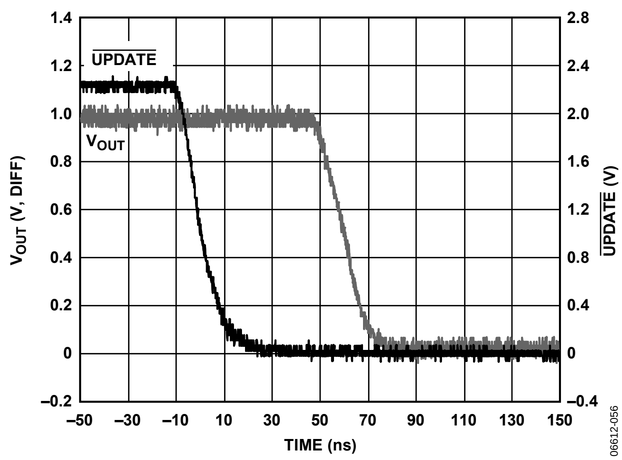

Figure 56. AD8104 Disable Time

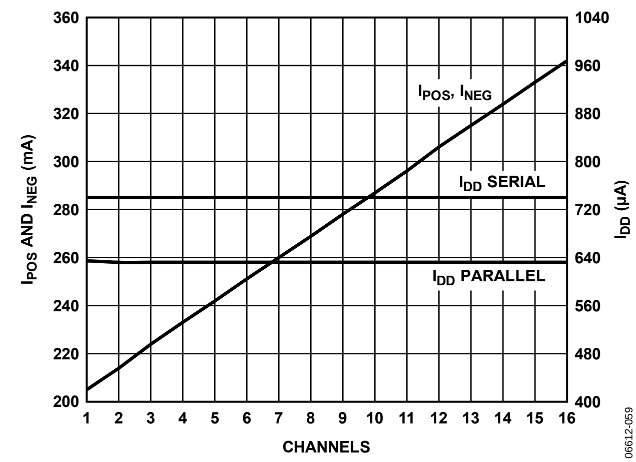

Figure 59. AD8104, AD8105 Quiescent Supply Currents vs. Enabled Outputs

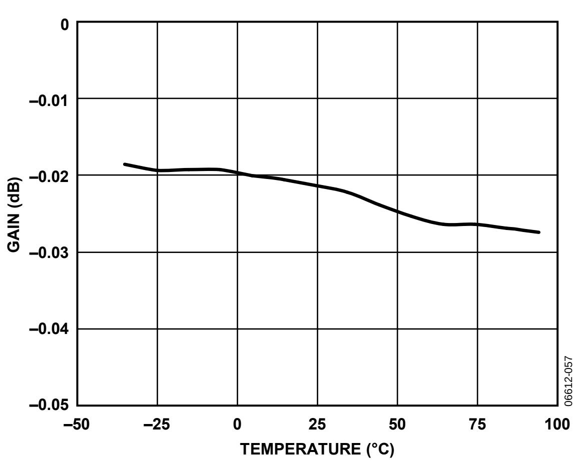

Figure 57. AD8104 DC Gain vs. Temperature

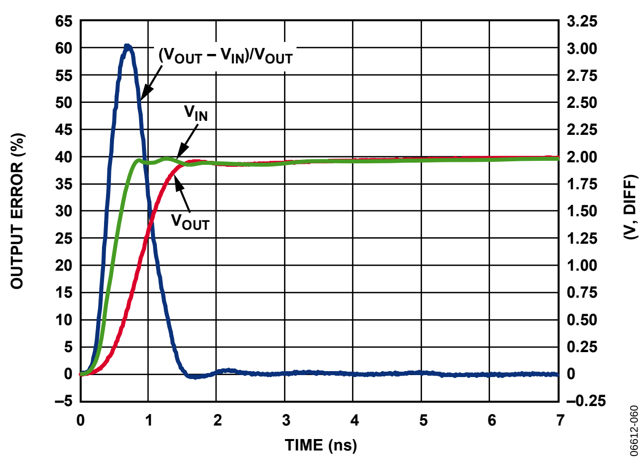

Figure 60. AD8104 Settling Time

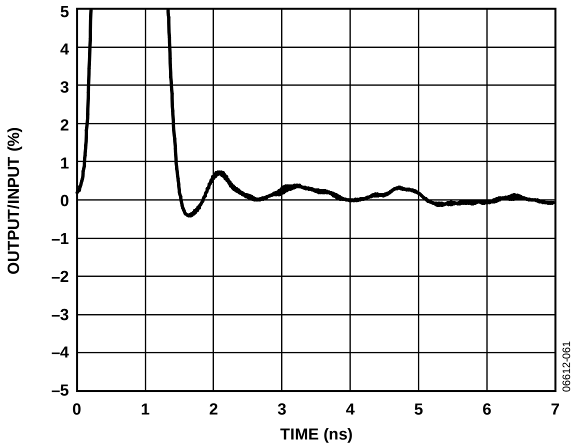

Figure 61. AD8104 Settling Time (Zoom)

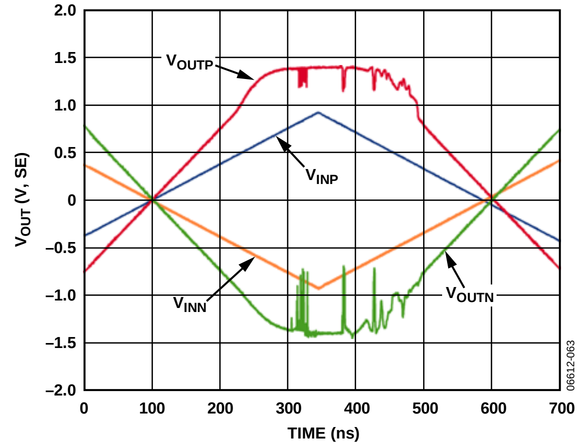

Figure 63. AD8105 Overdrive Recovery, Single-Ended

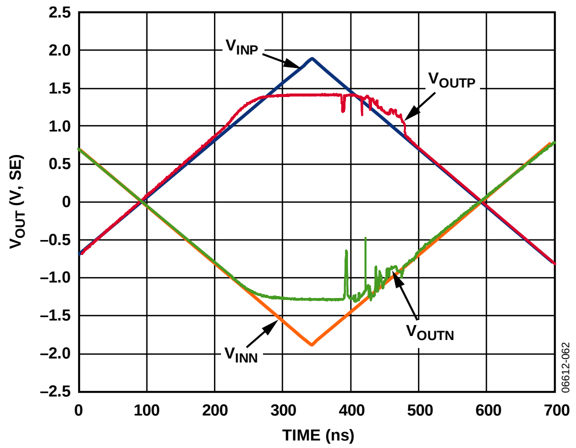

Figure 62. AD8104 Overdrive Recovery, Single-Ended

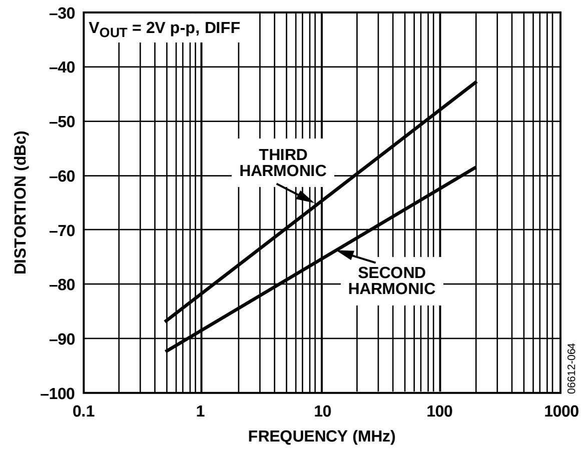

Figure 64. AD8104 Harmonic Distortion

THEORY OF OPERATION

The AD8104/AD8105 are fully differential crosspoint arrays with 16 outputs, each of which can be connected to any one of 32 inputs. Organized by output row, 32 switchable input transconductance stages are connected to each output buffer to form 32-to-1 multiplexers. There are 16 of these multiplexers, each with its inputs wired in parallel, for a total array of 512 transconductance stages forming a multicast-capable crosspoint switch.

Decoding logic for each output selects one (or none) of the transconductance stages to drive the output stage. The enabled transconductance stage drives the output stage, and feedback forms a closed-loop amplifier with a differential gain of +1 (the difference between the output voltages is equal to the difference between the input voltages). A second feedback loop controls the common-mode output level, forcing the average of the differential output voltages to match the voltage on the VOCM reference pin. Although each output has an independent common-mode control loop, the VOCM reference is common for the entire chip, and as such needs to be driven with a low impedance to avoid crosstalk.

Each differential input to the AD8104/AD8105 is buffered by a receiver. The purpose of this receiver is to provide an extended input common-mode range, and to remove this common mode from the signal chain. Like the output multiplexers, the input receiver has both a differential loop and a common-mode control loop. A mask-programmable feedback network sets the closed-loop differential gain. For the AD8104, this differential gain is +1, and for the AD8105, this differential gain is +2. The receiver has an input stage that does not respond to the common mode of the signal. This architecture, along with the attenuating feedback network, allows the user to apply input voltages that extend from rail to rail. Excess differential loop gain bandwidth product reduces the effect of the closed-loop gain on the bandwidth of the device.

The output stage of the AD8104/AD8105 is designed for low differential gain and phase error when driving composite video signals. It also provides slew current for fast pulse response when driving component video signals. Unlike many multiplexer designs, these requirements are balanced such that large signal bandwidth is very similar to small signal bandwidth. The design load is 150 Ω, but provisions are made to drive loads as low as 75 Ω as long as on-chip power dissipation limits are not exceeded.

The outputs of the AD8104/AD8105 can be disabled to minimize on-chip power dissipation. When disabled, there is a feedback network of 25 kΩ between the differential outputs. This high impedance allows multiple ICs to be bussed together without additional buffering. Care must be taken to reduce output capacitance, which results in more overshoot and frequency domain peaking. A series of internal amplifiers drive internal nodes such that a wideband high impedance is presented at the disabled output, even while the output bus is under large signal swings. When the outputs are disabled and driven externally, the voltage applied to them should not exceed the valid output swing range for the AD8104/AD8105 in order to keep these internal amplifiers in their linear range of operation. Applying excess differential voltages to the disabled outputs can cause damage to the AD8104/AD8105 and should be avoided (see the Absolute Maximum Ratings section for guidelines).

The connection of the AD8104/AD8105 is controlled by a flexible TTL-compatible logic interface. Either parallel or serial loading into a first rank of latches preprograms each output. A global update signal moves the programming data into the second rank of latches, simultaneously updating all outputs. In serial mode, a serial-out pin allows devices to be daisy-chained together for single-pin programming of multiple ICs. A power-on reset pin is available to avoid bus conflicts by disabling all outputs. This power-on reset clears the second rank of latches, but does not clear the first rank of latches. In parallel mode, to quickly clear the first rank, a broadcast parallel programming feature is available. In serial mode, preprogramming individual inputs is not possible and the entire shift register needs to be flushed.

The AD8104/AD8105 can operate on a single +5 V supply, powering both the signal path (with the VPOS/VNEG supply pins), and the control logic interface (with the VDD/DGND supply pins). However, to easily interface to ground-referenced video signals, split supply operation is possible with ±2.5 V supplies. In this case, a flexible logic interface allows the control logic supplies (VDD/DGND) to be run off +2 V/0 V to +5 V/0 V while the core remains on split supplies. Additional flexibility in the analog output common-mode level facilitates unequal split supplies. If +3 V/−2 V supplies to +2 V/−3 V supplies are desired, the VOCM pin can still be set to 0 V for ground-referenced video signals.

APPLICATIONS INFORMATION

PROGRAMMING

The AD8104/AD8105 have two options for changing the programming of the crosspoint matrix. In the first option, a serial word of 192 bits can be provided to update the entire matrix each time. The second option allows for changing the programming of a single output via a parallel interface. The serial option requires fewer signals, but more time (clock cycles) for changing the programming, while the parallel programming technique requires more signals, but can change a single output at a time and requires fewer clock cycles to complete programming.

Serial Programming Description

The serial programming mode uses the $\overline{\text{CLK}}$, DATA IN, $\overline{\text{UPDATE}}$, and $\overline{\text{SER}}$/PAR device pins. The first step is to assert a low on $\overline{\text{SER}}$/PAR in order to enable the serial programming mode. The parallel clock $\overline{\text{WE}}$ should be held high during the entire serial programming operation.

The $\overline{\text{UPDATE}}$ signal should be high during the time that data is shifted into the serial port of the device. Although the data still shifts in when $\overline{\text{UPDATE}}$ is low, the transparent, asynchronous latches allow the shifting data to reach the matrix. This causes the matrix to try to update to every intermediate state as defined by the shifting data.

The data at DATA IN is clocked in at every falling edge of $\overline{\text{CLK}}$. A total of 192 bits must be shifted in to complete the programming. For each of the 16 outputs, there are five bits (D0 to D4) that determine the source of its input followed by one bit (D5) that determines the enabled state of the output. If D5 is low (output disabled), the five associated bits (D0 to D4) do not matter, because no input is switched to that output. These comprise the first 96 bits of DATA IN. The remaining 96 bits of DATA IN should be set to zero. If a string of 96 zeros is not suffixed to the first 96 bits of DATA IN, a certain test mode is employed that can cause the device to draw up to 40% more supply current.

The most significant output address data, the enable bit (D5), is shifted in first, followed by the input address (D4 to D0) entered sequentially with D4 first and D0 last. Each remaining output is programmed sequentially, until the least significant output address data is shifted in. At this point, $\overline{\text{UPDATE}}$ can be taken low, which programs the device according to the data that was just shifted in. The $\overline{\text{UPDATE}}$ latches are asynchronous and when $\overline{\text{UPDATE}}$ is low, they are transparent.

If more than one AD8104/AD8105 device is to be serially programmed in a system, the DATA OUT signal from one device can be connected to the DATA IN of the next device to form a serial chain. All of the $\overline{\text{CLK}}$, $\overline{\text{UPDATE}}$, and $\overline{\text{SER}}$/PAR pins should be connected in parallel and operated as described previously. The serial data is input to the DATA IN pin of the first device of the chain, and it ripples through to the last. Therefore, the data for the last device in the chain should come at the beginning of the programming sequence. The length of the programming sequence is 192 bits times the number of devices in the chain.

Parallel Programming Description

When using the parallel programming mode, it is not necessary to reprogram the entire device when making changes to the matrix. In fact, parallel programming allows the modification of a single output at a time. Because this takes only one $\overline{\text{WE}}$/$\overline{\text{UPDATE}}$ cycle, significant time savings can be realized by using parallel programming.

One important consideration in using parallel programming is that the $\overline{\text{RESET}}$ signal does not reset all registers in the AD8104/AD8105. When taken low, the $\overline{\text{RESET}}$ signal only sets each output to the disabled state. This is helpful during power-up to ensure that two parallel outputs are not active at the same time.

After initial power-up, the internal registers in the device generally have random data, even though the $\overline{\text{RESET}}$ signal has been asserted. If parallel programming is used to program one output, then that output is properly programmed, but the rest of the device has a random program state depending on the internal register content at power-up. Therefore, when using parallel programming, it is essential that all outputs be programmed to a desired state after power-up. This ensures that the programming matrix is always in a known state. From then on, parallel programming can be used to modify a single output or more at a time.

In similar fashion, if $\overline{\text{UPDATE}}$ is taken low after initial power-up, the random power-up data in the shift register is programmed into the matrix. Therefore, in order to prevent the crosspoint from being programmed into an unknown state, do not apply a low logic level to $\overline{\text{UPDATE}}$ after power is initially applied. Programming the full shift register one time to a desired state, by either serial or parallel programming after initial power-up, eliminates the possibility of programming the matrix to an unknown state.

To change the programming of an output via parallel programming, $\overline{\text{SER}}$/PAR and $\overline{\text{UPDATE}}$ should be taken high. The serial programming clock, $\overline{\text{CLK}}$, should be left high during parallel programming. The parallel clock, $\overline{\text{WE}}$, should start in the high state. The 4-bit address of the output to be programmed should be put on A0 to A3. The first five data bits (D0 to D4) should contain the information that identifies the input that is programmed to the output that is addressed. The sixth data bit (D5) determines the enabled state of the output. If D5 is low (output disabled), then the data on D0 to D4 does not matter.

After the desired address and data signals have been established, they can be latched into the shift register by a high to low transition of the $\overline{\text{WE}}$ signal. The matrix is not programmed, however, until the $\overline{\text{UPDATE}}$ signal is taken low. It is thus possible to latch in new data for several or all of the outputs first via successive negative transitions of $\overline{\text{WE}}$ while $\overline{\text{UPDATE}}$ is held high, and then have all the new data take effect when $\overline{\text{UPDATE}}$ goes low. This technique should be used when programming the device for the first time after power-up when using parallel programming.

Reset

When powering up the AD8104/AD8105, it is usually desirable to have the outputs come up in the disabled state. The $\overline{\text{RESET}}$ pin, when taken low, causes all outputs to be in the disabled state. However, the $\overline{\text{UPDATE}}$ signal does not reset all registers in the AD8104/AD8105. This is important when operating in the parallel programming mode. Refer to the Parallel Programming Description section for information about programming internal registers after power-up. Serial programming programs the entire matrix each time; therefore, no special considerations apply.

Since the data in the shift register is random after power-up, it should not be used to program the matrix, or the matrix can enter unknown states. To prevent this, do not apply a logic low signal to $\overline{\text{UPDATE}}$ initially after power-up. The shift register should first be loaded with the desired data, and then $\overline{\text{UPDATE}}$ can be taken low to program the device.

The $\overline{\text{RESET}}$ pin has a 20 kΩ pull-up resistor to VDD that can be used to create a simple power-up reset circuit. A capacitor from $\overline{\text{RESET}}$ to ground holds $\overline{\text{RESET}}$ low for some time while the rest of the device stabilizes. The low condition causes all the outputs to be disabled. The capacitor then charges through the pull-up resistor to the high state, thus allowing full programming capability of the device.

Because the AD8104/AD8105 have random data in the internal registers at power-up, the device may power up in a test state where the supply current is larger than typical. Therefore, the $\overline{\text{RESET}}$ pin should be used to disable all outputs and bring the device out of any test mode.

OPERATING MODES

The AD8104/AD8105 has fully differential inputs and outputs. The inputs and outputs can also be operated in a single-ended fashion. This presents several options for circuit configurations that require different gains and treatment of terminations, if they are used.

Differential Input

Each differential input to the AD8104/AD8105 is applied to a differential receiver. These receivers allow the user to drive the inputs with a differential signal with an uncertain common-mode voltage, such as from a remote source over twisted pair. The receivers respond only to the difference in input voltages, and restores a common-mode voltage suitable for the internal signal path. Noise or crosstalk that is present in both inputs is rejected by the input stage, as specified by its common-mode rejection ratio (CMRR). Differential operation offers a great noise benefit for signals that are propagated over distance in a noisy environment.

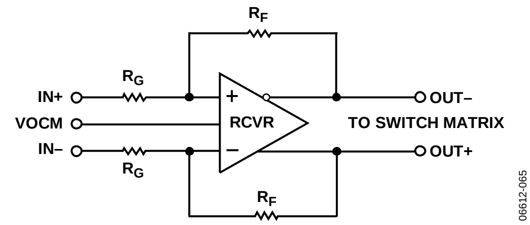

Figure 65. Input Receiver Equivalent Circuit

The circuit configuration used by the differential input receivers is similar to that of several Analog Devices, Inc. general-purpose differential amplifiers, such as the AD8131. It is a voltage feedback amplifier with internal gain setting resistors. The arrangement of feedback makes the differential input impedance appear to be 5 kΩ across the inputs.

$$R_{IN,dm} = 2 \times R_G = 5\ \text{k}\Omega$$

This impedance creates a small differential termination error if the user does not account for the 5 kΩ parallel element, although this error is less than 1% in most cases. Additionally, the source impedance driving the AD8104/AD8105 appears in parallel with the internal gain-setting resistors, such that there may be a gain error for some values of source resistance. The AD8104/AD8105 are adjusted such that its gains are correct when driven by a back-terminated 75 Ω source impedance at each input phase (37.5 Ω effective impedance to ground at each input pin, or 75 Ω differential source impedance across pairs of input pins). If a different source impedance is presented, the differential gain of the AD8104/AD8105 can be calculated by

$$G_{dm} = \frac{V_{OUT,dm}}{V_{IN,dm}} = \frac{R_F}{R_G + R_S}$$

where:

R_G = 2.5 kΩ.
R_S is the user single-ended source resistance (such as 37.5 Ω for a back-terminated 75 Ω source).
R_F = 2.538 kΩ for the AD8104 and 5.075 kΩ for the AD8105.

In the case of the AD8104,

$$G_{dm} = \frac{2.538\,\text{k}\Omega}{2.5\,\text{k}\Omega + R_S}$$

In the case of the AD8105,

$$G_{dm} = \frac{5.075\,\text{k}\Omega}{2.5\,\text{k}\Omega + R_S}$$

When operating with a differential input, care must be taken to keep the common mode, or average, of the input voltages within the linear operating range of the AD8104/AD8105 receiver. This common-mode range can extend rail-to-rail, provided the differential signal swing is small enough to avoid forward biasing the ESD diodes (it is safest to keep the common mode plus differential signal excursions within the supply voltages of the part). See the Specifications section for guaranteed input range.

The differential output of the AD8104/AD8105 receiver is linear for a peak of 1.4 V of output voltage difference (1.4 V peak input difference for the AD8104, and 0.7 V peak input difference for the AD8105). Taking the output differentially, using the two output phases, this allows 2.8 V p-p of linear output signal swing. Beyond this level, the signal path can saturate and limits the signal swing. This is not a desired operation, as the supply current increases and the signal path is slow to recover from clipping. The absolute maximum allowed differential input signal is limited by the long-term reliability of the input stage. The limits in the Absolute Maximum Ratings section should be observed in order to avoid degrading device performance permanently.

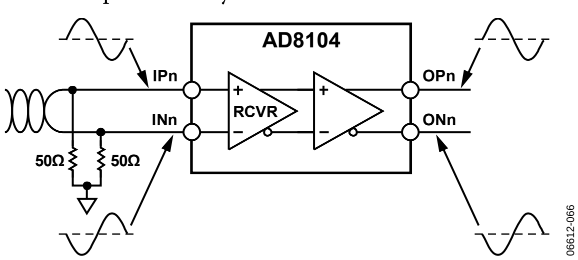

Figure 66. Example of Input Driven Differentially

Single-Ended Input

The AD8104/AD8105 input receivers can be driven single-endedly (unbalanced). From the standpoint of the receiver, there is very little difference between signals applied positive and negative in two phases to the input pair vs. a signal applied to one input only with the other input held at a constant potential. One small difference is that the common mode between the input pins is changing if only one input is moving, and there is a very small common-mode to differential conversion gain in the receiver that adds an additional gain error to the output (see the common-mode rejection ratio for the input stage in the Specifications section). For low frequencies, this gain error is negligible. The common-mode rejection ratio degrades with increasing frequency.

When operating the AD8104/AD8105 receivers single-endedly, the observed input resistance at each input pin is lower than in the differential input case, due to a fraction of the receiver internal output voltage appearing as a common-mode signal on its input terminals, bootstrapping the voltage on the input resistance. This single-ended input resistance can be calculated by the equation

$$R_{IN} = \frac{R_G + R_S}{1 - \dfrac{R_F}{2 \times (R_G + R_S + R_F)}}$$

where:

R_G = 2.5 kΩ.
R_S is the user single-ended source resistance (such as 37.5 Ω for a back-terminated 75 Ω source).
R_F = 2.538 kΩ for the AD8104 and 5.075 kΩ for the AD8105.

In most cases, a single-ended input signal is referred to midsupply, typically ground. In this case, the undriven differential input can be connected to ground. For best dynamic performance and lowest offset voltage, this unused input should be terminated with an impedance matching the driven input, instead of being directly shorted to ground. Due to the differential feedback of the receiver, there is high frequency signal current in the undriven input and it should be treated as a signal line in the board design.

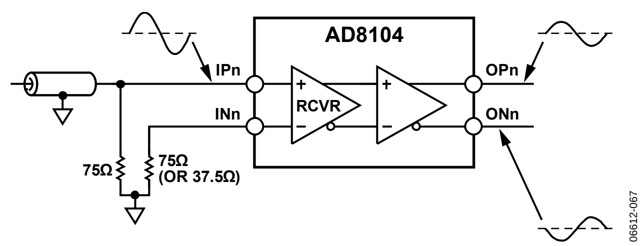

Figure 67. Example of Input Driven Single-Ended

AC Coupling of Inputs

It is possible to ac couple the inputs of the AD8104/AD8105 receiver. This is simplified because the bias current does not need to be supplied externally. A capacitor in series with the inputs to the AD8104/AD8105 creates a high-pass filter with the input impedance of the device. This capacitor needs to be sized such that the corner frequency is low enough for frequencies of interest.

Differential Output

Benefits of Differential Operation

The AD8104/AD8105 have a fully differential switch core, with differential outputs. The two output voltages move in opposite polarity, with a differential feedback loop maintaining a fixed output stage differential gain of +1 (the different overall signal path gains between the AD8104 and AD8105 are set in the input stage for best signal-to-noise ratio). This differential output stage provides a benefit of crosstalk-canceling due to parasitic coupling from one output to another being equal and out of phase. Additionally, if the output of the device is utilized in a differential design, noise, crosstalk, and offset voltages generated on-chip that are coupled equally into both outputs are cancelled by the common-mode rejection ratio of the next device in the signal chain. By utilizing the AD8104/AD8105 outputs in a differential application, the best possible noise and offset specifications can be realized.

Differential Gain

The specified signal path gain of the AD8104/AD8105 refers to its differential gain. For the AD8104, the gain of +1 means that the difference in voltage between the two output terminals is equal to the difference applied between the two input terminals. For the AD8105, the ratio of output difference voltage to applied input difference voltage is +2.

The common mode, or average voltage of the pair of output signals is set by the voltage on the VOCM pin. This voltage is typically set to midsupply (often ground), but can be moved approximately ±0.5 V to accommodate cases where the desired output common-mode voltage may not be midsupply (as in the case of unequal split supplies). Adjusting VOCM can limit differential swing internally below the specifications listed in Table 1.

Regardless of the differential gain of the device, the common-mode gain for the AD8104 and AD8105 is +1 to the output. This means that the common mode of the output voltages directly follows the reference voltage applied to the VOCM input.

The VOCM reference is a high speed signal input, common to all output stages on the device. It requires only small amounts of bias current, but noise appearing on this pin is buffered to the outputs of all the output stages. As such, the VOCM node should be connected to a low noise, low impedance voltage to avoid being a source of noise, offset, and crosstalk in the signal path.

Termination

The AD8104/AD8105 are designed to drive 150 Ω on each output (or an effective 300 Ω differential), but the output stage is capable of supplying the current to drive 100 Ω loads (200 Ω differential) over the specified operating temperature range. If care is taken to observe the maximum power derating curves, the output stage can drive 75 Ω loads with slightly reduced slew rate and bandwidth (an effective 150 Ω differential load).

Termination at the load end is recommended for best signal integrity. This load termination is often a resistor to a ground reference on each individual output. By terminating to the same voltage level that drives the VOCM reference, the power dissipation due to dc termination current is reduced. In differential signal paths, it is often desirable to terminate differentially, with a single resistor across the differential outputs at the load end. This is acceptable for the AD8104/AD8105, but when the device outputs are placed in a disabled state, a small amount of dc bias current is required if the output is to present as a high impedance over an excursion of output bus voltages. If the AD8104/AD8105 disabled outputs are floated (or simply tied together by a resistor), internal nodes saturate and an increase in disabled output current may be observed.

For best pulse response, it is often desirable to place a series resistor in each output to match the characteristic impedance and termination of the output trace or cable. This is known as back-termination, and helps shorten settling time by terminating reflected signals when driving a load that is not accurately terminated at the load end. A side effect of back-termination is an attenuation of the output signal by a factor of two. In this case, a gain of two is usually necessary somewhere in the signal path to restore the signal.

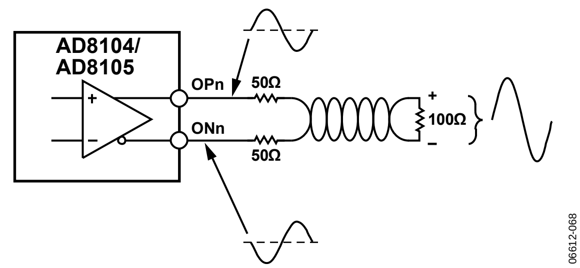

Figure 68. Example of Back-Terminated Differential Load

Single-Ended Output

Usage

The AD8104/AD8105 output pairs can be used single-endedly, taking only one output and not using the second. This is often desired to reduce the routing complexity in the design, or because a single-ended load is being driven directly. This mode of operation produces good results, but has some shortcomings when compared to taking the output differentially. When observing the single-ended output, noise that is common to both outputs appears in the output signal. This includes thermal noise in the chip biasing, as well as crosstalk that is coupled into the signal path. This component noise and crosstalk is equal in both outputs, and as such can be ignored by a differential receiver with a high common-mode rejection ratio. However, when taking the output single-ended, this noise is present with respect to the ground (or VOCM) reference and is not rejected.

When observing the output single-ended, the distribution of offset voltages appears greater. In the differential case, the difference between the outputs when the difference between the inputs is zero is a small differential offset. This offset is created from mismatches in components of the signal path, which must be corrected by the finite differential loop gain of the device. In the single-ended case, this differential offset is still observed, but an additional offset component is also relevant. This additional component is the common-mode offset, which is a difference between the average of the outputs and the VOCM reference. This offset is created by mismatches that affect the signal path in a common-mode manner, and is corrected by the finite common-mode loop gain of the device. A differential receiver would reject this common-mode offset voltage, but in the single-ended case, this offset is observed with respect to the signal ground. The single-ended output sums half the differential offset voltage and all of the common-mode offset voltage for a net increase in observed offset.

Single-Ended Gain

The AD8104/AD8105 operate as a closed-loop differential amplifier. The primary control loop forces the difference between the output terminals to be a ratio of the difference between the input terminals. One output increases in voltage, while the other decreases an equal amount to make the total difference correct. The average of these output voltages is forced to be equal to the voltage on the VOCM terminal by a second control loop. If only one output terminal is observed with respect to the VOCM terminal, only half of the difference voltage is observed. This implies that when using only one output of the device, half of the differential gain is observed. An AD8104 taken with single-ended output appears to have a gain of +0.5. An AD8105 has a single-ended gain of +1.

This factor of one half in the gain increases the noise of the device when referred to the input, contributing to higher noise specifications for single-ended output designs.

Termination

When operating the AD8104/AD8105 with a single-ended output, the preferred output termination scheme is a resistor at the load end to the VOCM voltage. A back-termination can be used, at an additional cost of one half the signal gain.

In single-ended output operation, the complementary phase of the output is not used, and may or may not be terminated locally. Although the unused output can be floated to reduce power dissipation, there are several reasons for terminating the unused output with a load resistance matched to the load on the signal output.

One component of crosstalk is magnetic, coupling by mutual inductance between output package traces and bond wires that carry load current. In a differential design, there is coupling from one pair of outputs to other adjacent pairs of outputs. The differential nature of the output signal simultaneously drives the coupling field in one direction for one phase of the output, and in an opposite direction for the other phase of the output. These magnetic fields do not couple exactly equal into adjacent output pairs due to different proximities, but they do destructively cancel the crosstalk to some extent. If the load current in each output is equal, this cancellation is greater, and less adjacent crosstalk is observed (regardless if the second output is actually being used).

A second benefit of balancing the output loads in a differential pair is to reduce fluctuations in current requirements from the power supply. In single-ended loads, the load currents alternate from the positive supply to the negative supply. This creates a parasitic signal voltage in the supply pins due to the finite resistance and inductance of the supplies. This supply fluctuation appears as crosstalk in all outputs, attenuated by the power supply rejection ratio (PSRR) of the device. At low frequencies, this is a negligible component of crosstalk, but PSRR falls off as frequency increases. With differential, balanced loads, as one output draws current from the positive supply, the other output draws current from the negative supply. When the phase alternates, the first output draws current from the negative supply and the second from the positive supply. The effect is that a more constant current is drawn from each supply, such that the crosstalk-inducing supply fluctuation is minimized.

A third benefit of driving balanced loads can be seen if one considers that the output pulse response changes as load changes. The differential signal control loop in the AD8104/AD8105 forces the difference of the outputs to be a fixed ratio to the difference of the inputs. If the two output responses are different due to loading, this creates a difference that the control loop sees as signal response error, and it attempts to correct this error. This distorts the output signal from the ideal response if the two outputs were balanced.

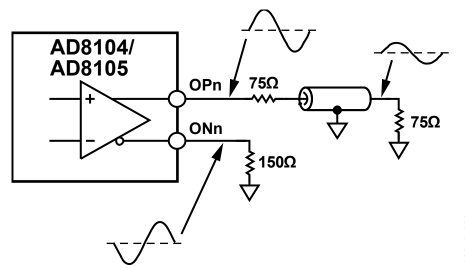

Figure 69. Example of Back-Terminated Single-Ended Load

Decoupling

The signal path of the AD8104/AD8105 is based on high open-loop gain amplifiers with negative feedback. Dominant-pole compensation is used on-chip to stabilize these amplifiers over the range of expected applied swing and load conditions. To guarantee this designed stability, proper supply decoupling is necessary with respect to both the differential control loops and the common-mode control loops of the signal path. Signal-generated currents must return to their sources through low impedance paths at all frequencies in which there is still loop gain (up to 700 MHz at a minimum). A wideband parallel capacitor arrangement is necessary to properly decouple the AD8104/AD8105.

The signal path compensation capacitors in the AD8104/AD8105 are connected to the VNEG supply. At high frequencies, this limits the power supply rejection ratio (PSRR) from the VNEG supply to a lower value than that from the VPOS supply. If given a choice, an application board should be designed such that the VNEG power is supplied from a low inductance plane, subject to a least amount of noise.

The VOCM should be considered a reference pin and not a power supply. It is an input to the high speed, high gain common-mode control loop of all receivers and output drivers. In the single-ended output sense, there is no rejection from noise on the VOCM net to the output. For this reason, care must be taken to produce a low noise VOCM source over the entire range of frequencies of interest. This is not only important to single-ended operation, but to differential operation as well, as there is a common-mode-to-differential gain conversion that becomes greater at higher frequencies.

During operation of the AD8104/AD8105, transient currents flow into the VOCM net from the amplifier control loops. Although the magnitude of these currents are small (10 µA to 20 µA per output), they can contribute to crosstalk if they flow through significant impedances. Driving VOCM with a low impedance, low noise source is desirable.

Power Dissipation

Calculation of Power Dissipation

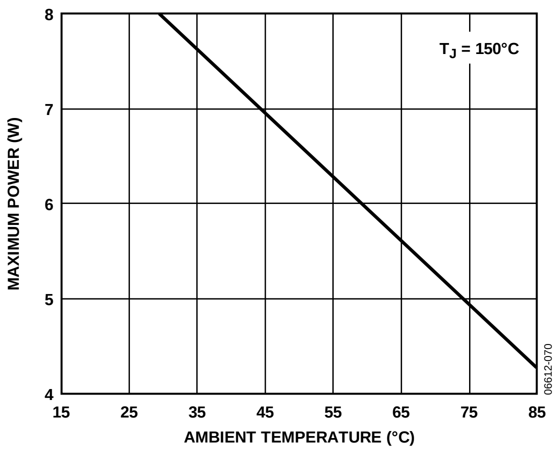

Figure 70. Maximum Die Power Dissipation vs. Ambient Temperature

The curve in Figure 70 was calculated from

$$P_{D,MAX} = \frac{T_{JUNCTION,MAX} - T_{AMBIENT}}{\theta_{JA}} \quad (1)$$

As an example, if the AD8104/AD8105 is enclosed in an environment at 45°C (T_A), the total on-chip dissipation under all load and supply conditions must not be allowed to exceed 7.0 W.

When calculating on-chip power dissipation, it is necessary to include the rms current being delivered to the load, multiplied by the rms voltage drop on the AD8104/AD8105 output devices. For a sinusoidal output, the on-chip power dissipation due to the load can be approximated by

$$P_{D,OUTPUT} = (V_{POS} - V_{OUTPUT,RMS}) \times I_{OUTPUT,RMS}$$

For nonsinusoidal output, the power dissipation should be calculated by integrating the on-chip voltage drop multiplied by the load current over one period.

The user can subtract the quiescent current for the Class AB output stage when calculating the loaded power dissipation. For each output stage driving a load, subtract a quiescent power according to

$$P_{DQ,OUTPUT} = (V_{POS} - V_{NEG}) \times I_{OUTPUT,QUIESCENT}$$

where $I_{OUTPUT,\ QUIESCENT}$ = 1.65 mA for each single-ended output pin.

For each disabled output, the quiescent power supply current in VPOS and VNEG drops by approximately 9 mA.

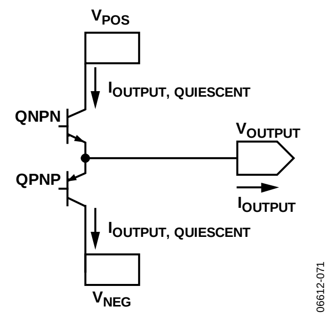

Figure 71. Simplified Output Stage

Example

For the AD8104/AD8105, in an ambient temperature of 85°C, with all 16 outputs driving 1 V rms into 100 Ω loads and power supplies at ±2.5 V, follow these steps:

1. Calculate power dissipation of AD8104/AD8105 using data sheet quiescent currents. Disregard VDD current, as it is insignificant.

   $$P_{D,QUIESCENT} = (V_{POS} \times I_{VPOS}) + (V_{NEG} \times I_{VNEG})$$

   $$P_{D,QUIESCENT} = (2.5\text{ V} \times 340\text{ mA}) + (2.5\text{ V} \times 340\text{ mA}) = 1.7\text{ W}$$

2. Calculate power dissipation from loads. For a differential output and ground-referenced load, the output power is symmetrical in each output phase.

   $$P_{D,OUTPUT} = (V_{POS} - V_{OUTPUT,RMS}) \times I_{OUTPUT,RMS}$$

   $$P_{D,OUTPUT} = (2.5\text{ V} - 1\text{ V}) \times (1\text{ V}/100\ \Omega) = 15\text{ mW}$$

   There are 16 output pairs, or 32 output currents.

   $$nP_{D,OUTPUT} = 32 \times 15\text{ mW} = 0.48\text{ W}$$

3. Subtract the quiescent output stage current for number of loads (32 in this example). The output stage is either standing, or driving a load, but the current only needs to be counted once (valid for output voltages > 0.5 V).

   $$P_{DQ,OUTPUT} = (V_{POS} - V_{NEG}) \times I_{OUTPUT,QUIESCENT}$$

   $$P_{DQ,OUTPUT} = (2.5\text{ V} - (-2.5\text{ V})) \times 1.65\text{ mA} = 8.25\text{ mW}$$

   There are 16 output pairs, or 32 output currents.

   $$nP_{DQ,OUTPUT} = 32 \times 8.25\text{ mW} = 0.26\text{ W}$$

4. Verify that the power dissipation does not exceed the maximum allowed value.

   $$P_{D,ON-CHIP} = P_{D,QUIESCENT} + nP_{D,OUTPUT} - nP_{DQ,OUTPUT}$$

   $$P_{D,ON-CHIP} = 1.7\text{ W} + 0.48\text{ W} - 0.26\text{ W} = 1.9\text{ W}$$

From Figure 70 or Equation 1, this power dissipation is below the maximum allowed dissipation for all ambient temperatures up to and including 85°C.

Short-Circuit Output Conditions

Although there is short-circuit current protection on the AD8104/AD8105 outputs, the output current can reach values of 80 mA into a grounded output. Any sustained operation with too many shorted outputs can exceed the maximum die temperature and can result in device failure (see the Absolute Maximum Ratings section).

Crosstalk

Many systems, such as broadcast video and KVM switches, that handle numerous analog signal channels, have strict requirements for keeping the various signals from influencing any of the others in the system. Crosstalk is the term used to describe the coupling of the signals of other nearby channels to a given channel.

When there are many signals in close proximity in a system, as is undoubtedly the case in a system that uses the AD8104/AD8105, the crosstalk issues can be quite complex. A good understanding of the nature of crosstalk and some definition of terms is required in order to specify a system that uses one or more crosspoint devices.

Types of Crosstalk

Crosstalk can be propagated by means of any of three methods. These fall into the categories of electric field, magnetic field, and sharing of common impedances. This section explains these effects.

Every conductor can be both a radiator of electric fields and a receiver of electric fields. The electric field crosstalk mechanism occurs when the electric field created by the transmitter propagates across a stray capacitance (for example, free space), couples with the receiver, and induces a voltage. This voltage is an unwanted crosstalk signal in any channel that receives it.

Currents flowing in conductors create magnetic fields that circulate around the currents. These magnetic fields then generate voltages in any other conductors whose paths they link. The undesired induced voltages in these other channels are crosstalk signals. The channels that crosstalk can be said to have a mutual inductance that couples signals from one channel to another.

The power supplies, grounds, and other signal return paths of a multichannel system are generally shared by the various channels. When a current from one channel flows in one of these paths, a voltage that is developed across the impedance becomes an input crosstalk signal for other channels that share the common impedance.

All these sources of crosstalk are vector quantities; therefore, the magnitudes cannot simply be added together to obtain the total crosstalk. In fact, there are conditions where driving additional circuits in parallel in a given configuration can actually reduce the crosstalk. Because the AD8104/AD8105 are fully differential designs, many sources of crosstalk either destructively cancel, or are common mode to the signal and can be rejected by a differential receiver.

Areas of Crosstalk

A practical AD8104/AD8105 circuit must be mounted to some sort of circuit board in order to connect it to power supplies and measurement equipment. Great care must be taken to create an evaluation board that adds minimum crosstalk to the intrinsic device. This, however, raises the issue that the crosstalk of a system is a combination of the intrinsic crosstalk of the devices in addition to the circuit board to which they are mounted. It is important to try to separate these two areas when attempting to minimize the effect of crosstalk.

In addition, crosstalk can occur among the inputs to a crosspoint and among the outputs. It can also occur from input to output. Techniques are discussed in the following sections for diagnosing which part of a system is contributing to crosstalk.

Measuring Crosstalk

Crosstalk is measured by applying a signal to one or more channels and measuring the relative strength of that signal on a desired selected channel. The measurement is usually expressed as dB down from the magnitude of the test signal. The crosstalk is expressed by

$$|XT| = 20\log_{10}\left(\frac{A_{SEL}(s)}{A_{TEST}(s)}\right)$$

where:

$s = j\omega$, the Laplace transform variable.
$A_{SEL}(s)$ is the amplitude of the crosstalk induced signal in the selected channel.
$A_{TEST}(s)$ is the amplitude of the test signal.

It can be seen that crosstalk is a function of frequency, but not a function of the magnitude of the test signal (to first order). In addition, the crosstalk signal has a phase relative to the test signal associated with it.

A network analyzer is most commonly used to measure crosstalk over a frequency range of interest. It can provide both magnitude and phase information about the crosstalk signal.

As a crosspoint system or device grows larger, the number of theoretical crosstalk combinations and permutations can become extremely large. For example, in the case of the 32 × 16 matrix of the AD8104/AD8105, look at the number of crosstalk terms that can be considered for a single channel, for example, the input IN00. IN00 is programmed to connect to one of the AD8104/AD8105 outputs where the measurement can be made.

First, the crosstalk terms associated with driving a test signal into each of the other 31 inputs can be measured one at a time, while applying no signal to IN00. Then the crosstalk terms associated with driving a parallel test signal into all 31 other inputs can be measured two at a time in all possible combinations, then three at a time, and so on, until, finally, there is only one way to drive a test signal into all 31 other inputs in parallel.

Each of these cases is legitimately different from the others and may yield a unique value, depending on the resolution of the measurement system, but it is hardly practical to measure all these terms and then specify them. In addition, this describes the crosstalk matrix for just one input channel. A similar crosstalk matrix can be proposed for every other input. In addition, if the possible combinations and permutations for connecting inputs to the other outputs (not used for measurement) are taken into consideration, the numbers rather quickly grow to astronomical proportions. If a larger crosspoint array of multiple AD8104/AD8105 devices is constructed, the numbers grow larger still.

Obviously, some subset of all these cases must be selected to be used as a guide for a practical measure of crosstalk. One common method is to measure all-hostile crosstalk; this means that the crosstalk to the selected channel is measured while all other system channels are driven in parallel. In general, this yields the worst crosstalk number, but this is not always the case, due to the vector nature of the crosstalk signal.

Other useful crosstalk measurements are those created by one nearest neighbor or by the two nearest neighbors on either side. These crosstalk measurements are generally higher than those of more distant channels, so they can serve as a worst-case measure for any other one-channel or two-channel crosstalk measurements.

Input and Output Crosstalk

Capacitive coupling is voltage-driven (dV/dt), but is generally a constant ratio. Capacitive crosstalk is proportional to input or output voltage, but this ratio is not reduced by simply reducing signal swings. Attenuation factors must be changed by changing impedances (lowering mutual capacitance), or destructive canceling must be utilized by summing equal and out of phase components. For high input impedance devices such as the AD8104/AD8105, capacitances generally dominate input-generated crosstalk.

Inductive coupling is proportional to current (dI/dt), and often scales as a constant ratio with signal voltage, but also shows a dependence on impedances (load current). Inductive coupling can also be reduced by constructive canceling of equal and out of phase fields. In the case of driving low impedance video loads, output inductances contribute highly to output crosstalk.

The flexible programming capability of the AD8104/AD8105 can be used to diagnose whether crosstalk is occurring more on the input side or the output side. Some examples are illustrative. A given input pair (IN07 in the middle for this example) can be programmed to drive OUT07 (also in the middle). The inputs to IN07 are just terminated to ground (via 50 Ω or 75 Ω) and no signal is applied.

All the other inputs are driven in parallel with the same test signal (practically provided by a distribution amplifier), with all other outputs except OUT07 disabled. Since grounded IN07 is programmed to drive OUT07, no signal should be present. Any signal that is present can be attributed to the other 31 hostile input signals, because no other outputs are driven (they are all disabled). Thus, this method measures the all hostile input contribution to crosstalk into IN07. Of course, the method can be used for other input channels and combinations of hostile inputs.

For output crosstalk measurement, a single input channel is driven (IN00, for example) and all outputs other than a given output (IN07 in the middle) are programmed to connect to IN00. OUT07 is programmed to connect to IN15 (far away from IN00), which is terminated to ground. Thus OUT07 should not have a signal present since it is listening to a quiet input. Any signal measured at the OUT07 can be attributed to the output crosstalk of the other 16 hostile outputs. Again, this method can be modified to measure other channels and other crosspoint matrix combinations.

Effect of Impedances on Crosstalk

The input side crosstalk can be influenced by the output impedance of the sources that drive the inputs. The lower the impedance of the drive source, the lower the magnitude of the crosstalk. The dominant crosstalk mechanism on the input side is capacitive coupling. The high impedance inputs do not have significant current flow to create magnetically induced crosstalk. However, significant current can flow through the input termination resistors and the loops that drive them. Thus, the PC board on the input side can contribute to magnetically coupled crosstalk.

From a circuit standpoint, the input crosstalk mechanism looks like a capacitor coupling to a resistive load. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20\log_{10}\left((R_S C_M) \times s\right)$$

where:

R_S is the source resistance.
C_M is the mutual capacitance between the test signal circuit and the selected circuit.
s is the Laplace transform variable.

From the preceding equation, it can be observed that this crosstalk mechanism has a high-pass nature; it can also be minimized by reducing the coupling capacitance of the input circuits and lowering the output impedance of the drivers. If the input is driven from a 75 Ω terminated cable, the input crosstalk can be reduced by buffering this signal with a low output impedance buffer.

On the output side, the crosstalk can be reduced by driving a lighter load. Although the AD8104/AD8105 are specified with excellent differential gain and phase when driving a standard 150 Ω video load, the crosstalk is higher than the minimum obtainable due to the high output currents. These currents induce crosstalk via the mutual inductance of the output pins and bond wires of the AD8104/AD8105.

From a circuit standpoint, this output crosstalk mechanism looks like a transformer with a mutual inductance between the windings that drive a load resistor. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20\log_{10}\left(M_{XY} \times \frac{s}{R_L}\right)$$

where:

M_{XY} is the mutual inductance of Output X to Output Y.
R_L is the load resistance on the measured output.

This crosstalk mechanism can be minimized by keeping the mutual inductance low and increasing R_L. The mutual inductance can be kept low by increasing the spacing of the conductors and minimizing their parallel length.

PCB Layout

Extreme care must be exercised to minimize additional crosstalk generated by the system circuit board(s). The areas that must be carefully detailed are grounding, shielding, signal routing, and supply bypassing.

The packaging of the AD8104/AD8105 is designed to help keep the crosstalk to a minimum. On the BGA substrate, each pair is carefully routed to predominately couple to each other, with shielding traces separating adjacent signal pairs. The ball grid array is arranged such that similar board routing can be achieved. Only the outer two rows are used for signals, such that vias can be used to take the input rows to a lower signal plane if desired.

The input and output signals have minimum crosstalk if they are located between ground planes on layers above and below, and separated by ground in between. Vias should be located as close to the IC as possible to carry the inputs and outputs to the inner layer. The input and output signals surface at the input termination resistors and the output series back-termination resistors. To the extent possible, these signals should also be separated as soon as they emerge from the IC package.

PCB Termination Layout

As frequencies of operation increase, the importance of proper transmission line signal routing becomes more important. The bandwidth of the AD8104/AD8105 is large enough that using high impedance routing does not provide a flat in-band frequency response for practical signal trace lengths. It is necessary for the user to choose a characteristic impedance suitable for the application and properly terminate the input and output signals of the AD8104/AD8105. Traditionally, video applications have used 75 Ω single-ended environments. RF applications are generally 50 Ω single-ended (and board manufacturers have the most experience with this application). CAT-5 cabling is usually driven as differential pairs of 100 Ω differential impedance.

For flexibility, the AD8104/AD8105 do not contain on-chip termination resistors. This flexibility in application comes with some board layout challenges. The distance between the termination of the input transmission line and the AD8104/AD8105 die is a high impedance stub, and causes reflections of the input signal. With some simplification, it can be shown that these reflections cause peaking of the input at regular intervals in frequency, dependent on the propagation speed (V_P) of the signal in the chosen board material and the distance (d) between the termination resistor and the AD8104/AD8105. If the distance is great enough, these peaks can occur in-band. In fact, practical experience shows that these peaks are not high-Q, and should be pushed out to three or four times the desired bandwidth to avoid an effect on the signal. For a board designer using FR4 (V_P = 144 × 106 m/s), this means the AD8104/AD8105 input should be placed no farther than 1.5 cm after the termination resistors, and preferably should be placed even closer. The BGA substrate routing inside the AD8104/AD8105 is approximately 1 cm in length and adds to the stub length, so 1.5 cm PCB routing equates to d = 2.5 × 10^{-2} m in the calculations.

$$f_{PEAK} = \frac{(2n+1) \times V_P}{4d}$$

where $n = \{0, 1, 2, 3, \ldots\}$.

In some cases, it is difficult to place the termination close to the AD8104/AD8105 due to space constraints, differential routing, and large resistor footprints. A preferable solution in this case is to maintain a controlled transmission line past the AD8104/AD8105 inputs and terminate the end of the line. This is known as fly-by termination. The input impedance of the AD8104/AD8105 is large enough and stub length inside the package is small enough that this works well in practice. Implementation of fly-by input termination often includes bringing the signal in on one routing layer, then passing through a filled via under the AD8104/AD8105 input ball, then back out to termination on another signal layer. In this case, care must be taken to tie the reference ground planes together near the signal via if the signal layers are referenced to different ground planes.

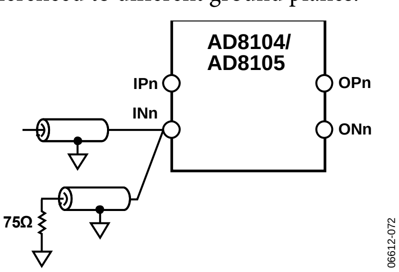

Figure 72. Fly-By Input Termination, Grounds for the Two Transmission Lines Shown Must be Tied Together Close to the INn Pin

If multiple AD8104/AD8105 devices are to be driven in parallel, a fly-by input termination scheme is very useful, but the distance from each AD8104/AD8105 input to the driven input transmission line is a stub that should be minimized in length and parasitics using the discussed guidelines.

When driving the AD8104/AD8105 single-endedly, the undriven input is often terminated with a resistance to balance the input stage. It can be seen that by terminating the undriven input with a resistor of one half the characteristic impedance, the input stage is perfectly balanced (37.5 Ω, for example, to balance the two parallel 75 Ω terminations on the driven input). However, due to the feedback in the input receiver, there is high speed signal current leaving the undriven input. To terminate this high speed signal, proper transmission line techniques should be used. One solution is to adjust the trace width to create a transmission line of half the characteristic impedance and terminate the far end with this resistance (37.5 Ω in a 75 Ω system). This is not often practical as trace widths become large. In most cases, the best practical solution is to place the half-characteristic impedance resistor as close as possible (preferably less than 1.5 cm away) and to reduce the parasitics of the stub (by removing the ground plane under the stub, for example). In either case, the designer must decide if the layout complexity created by a balanced, terminated solution is preferable to simply grounding the undriven input at the ball with no trace.

Although the examples discussed so far are for input termination, the theory is similar for output back-termination. Taking the AD8104/AD8105 as an ideal voltage source, any distance of routing between the AD8104/AD8105 and a back-termination resistor is an impedance mismatch that potentially creates reflections. For this reason, back-termination resistors should also be placed close to the AD8104/AD8105. In practice, because back-termination resistors are series elements, they can be placed close to the AD8104/AD8105 outputs.

OUTLINE DIMENSIONS

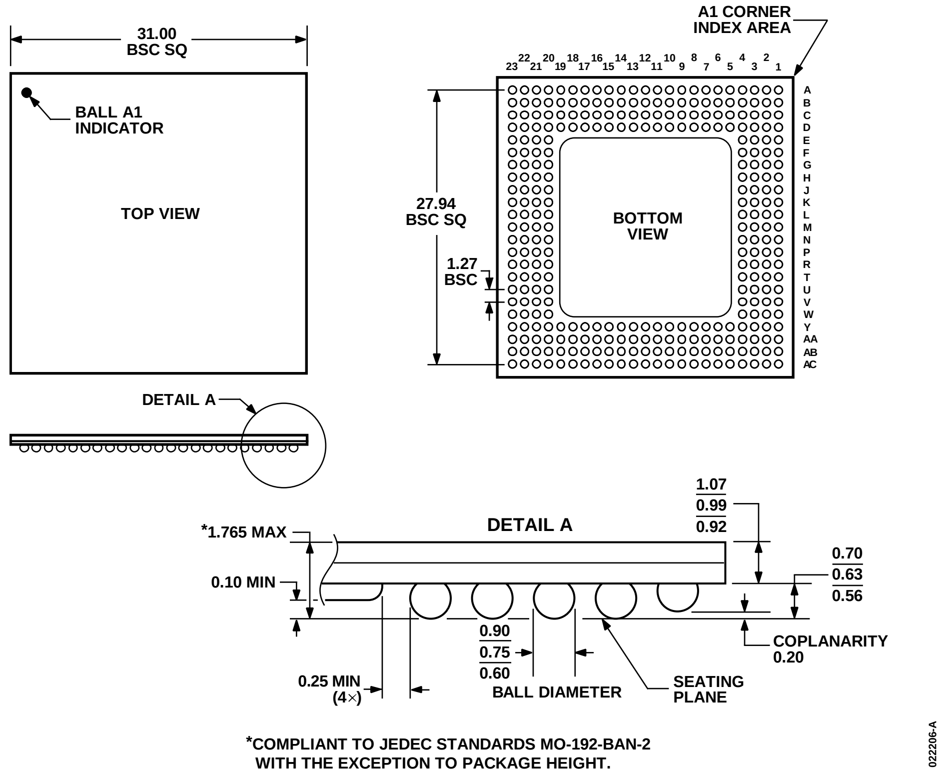

Figure 73. 304-Ball Ball Grid Array, Thermally Enhanced [BGA_ED] (BP-304)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8104ABPZ	−40°C to +85°C	304-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-304
AD8105ABPZ	−40°C to +85°C	304-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-304

[1] Z = RoHS Compliant Part.