

FEATURES

- **SOT-23 Package**
- **Maximum Offset Voltage of 3 μ V**
- **Maximum Offset Voltage Drift of 30nV/ $^{\circ}$ C**
- Noise: 1.5 μ V_{P-P} (0.01Hz to 10Hz Typ)
- Voltage Gain: 140dB (Typ)
- PSRR: 130dB (Typ)
- CMRR: 130dB (Typ)
- Supply Current: 0.8mA (Typ)
- Supply Operation: 2.7V to 6V (LTC2050)
2.7V to $\pm$ 5.5V (LTC2050HV)
- Extended Common Mode Input Range
- Output Swings Rail-to-Rail
- Input Overload Recovery Time: 2ms (Typ)

APPLICATIONS

- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition
- DC Accurate RC Active Filters
- Low Side Current Sense

DESCRIPTION

The LTC[®]2050 and LTC2050HV are zero-drift operational amplifiers available in the 5- or 6-lead SOT-23 and SO-8 packages. The LTC2050 operates from a single 2.7V to 6V supply. The LTC2050HV operates on supplies from 2.7V to $\pm$ 5.5V. The current consumption is 800 μ A and the versions in the 6-lead SOT-23 and SO-8 packages offer power shutdown (active low).

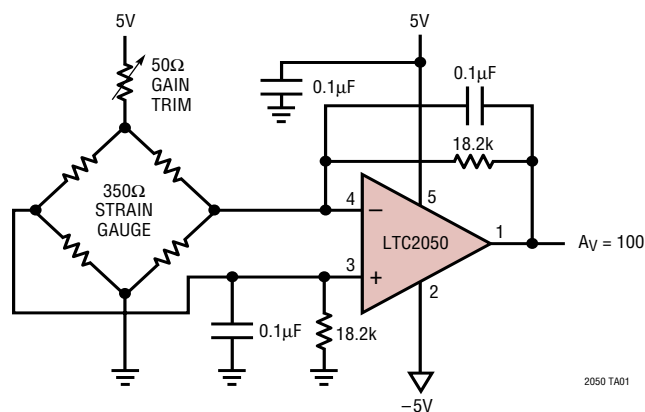
The LTC2050, despite its miniature size, features uncompromising DC performance. The typical input offset voltage and offset drift are 0.5 μ V and 10nV/ $^{\circ}$ C. The almost zero DC offset and drift are supported with a power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) of more than 130dB.

The input common mode voltage ranges from the negative supply up to typically 1V from the positive supply. The LTC2050 also has an enhanced output stage capable of driving loads as low as 2k Ω to both supply rails. The open-loop gain is typically 140dB. The LTC2050 also features a 1.5 μ V_{P-P} DC to 10Hz noise and a 3MHz gain bandwidth product.

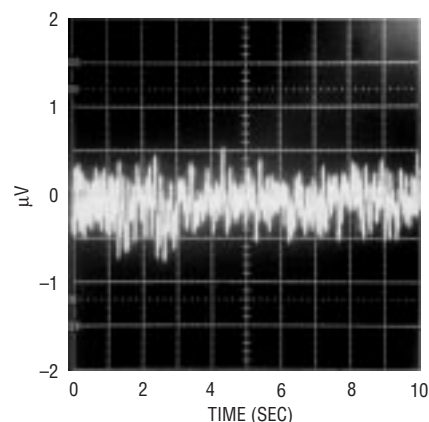
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TYPICAL APPLICATION

Differential Bridge Amplifier



Input Referred Noise 0.1Hz to 10Hz



LTC2050/LTC2050HV

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-)	Operating Temperature Range	-40°C to 85°C
LTC2050 7V	Specified Temperature Range (Note 3) ..	-40°C to 85°C
LTC2050HV 12V	Storage Temperature Range	-65°C to 150°C
Input Voltage ($V^+ + 0.3\text{V}$) to ($V^- - 0.3\text{V}$)	Lead Temperature (Soldering, 10 sec)	300°C
Output Short-Circuit Duration		Indefinite

PACKAGE/ORDER INFORMATION

TOP VIEW S5 PACKAGE 5-LEAD PLASTIC SOT-23 $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 250^{\circ}\text{C/W}$		TOP VIEW S6 PACKAGE 6-LEAD PLASTIC SOT-23 $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 230^{\circ}\text{C/W}$		TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 190^{\circ}\text{C/W}$	
ORDER PART NUMBER	S5 PART MARKING	ORDER PART NUMBER	S6 PART MARKING	ORDER PART NUMBER	S8 PART MARKING
LTC2050CS5 LTC2050HVCS5 LTC2050HVIS5	LTIN LTNY LTNZ	LTC2050CS6 LTC2050HVCS6 LTC2050HVIS6	LTIP LTPA LTPB	LTC2050CS8 LTC2050IS8 LTC2050HVCS8 LTC2050HVIS8	2050 2050I 2050HV 050HVI

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS (LTC2050, LTC2050HV) The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = 3\text{V}$ unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	(Note 2)		± 0.5	± 3	μV
Average Input Offset Drift	(Note 2) ●			± 0.03	$\mu\text{V}/^{\circ}\text{C}$
Long-Term Offset Drift			50		$\text{nV}/\sqrt{\text{mo}}$
Input Bias Current	LTC2050 ●		± 20	± 75	pA
	LTC2050HV ●		± 1	± 50	pA
Input Offset Current	LTC2050 ●			± 150	pA
	LTC2050HV ●			± 200	pA
	LTC2050 ●			± 100	pA
	LTC2050HV ●			± 150	pA
Input Noise Voltage	$R_S = 100\Omega$, 0.01Hz to 10Hz		1.5		$\mu\text{V}_{\text{P-P}}$
Common Mode Rejection Ratio	$V_{\text{CM}} = \text{GND to } (V^+ - 1.3)$	115	130		dB
	$V_{\text{CM}} = \text{GND to } (V^+ - 1.3)$ ●	110	130		dB
Power Supply Rejection Ratio	$V_S = 2.7\text{V to } 6\text{V}$	120	130		dB
	●	115	130		dB

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 3\text{V}$ unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Large-Signal Voltage Gain	$R_L = 10\text{k}$	●	120 115	140 140		dB dB
Output Voltage Swing High	$R_L = 2\text{k to GND}$	●	2.85	2.94		V
	$R_L = 10\text{k to GND}$	●	2.95	2.98		V
Output Voltage Swing Low	$R_L = 2\text{k to GND}$	●		1	10	mV
	$R_L = 10\text{k to GND}$	●		1	10	mV
Slew Rate				2		V/ μs
Gain Bandwidth Product				3		MHz
Supply Current	$V_{\text{SHDN}} = V_{\text{IH}}$, No Load	●		0.75	1.1	mA
	$V_{\text{SHDN}} = V_{\text{IL}}$	●			10	μA
Shutdown Pin Input Low Voltage (V_{IL})		●			$V^- + 0.5$	V
Shutdown Pin Input High Voltage (V_{IH})		●	$V^+ - 0.5$			V
Shutdown Pin Input Current	$V_{\text{SHDN}} = \text{GND}$	●		-0.5	-3	μA
Internal Sampling Frequency				7.5		kHz

(LTC2050, LTC2050HV) $V_S = 5\text{V}$ unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	(Note 2)			± 0.5	± 3	μV
Average Input Offset Drift	(Note 2)	●			± 0.03	$\mu\text{V}/^\circ\text{C}$
Long-Term Offset Drift				50		$\text{nV}/\sqrt{\text{mo}}$
Input Bias Current	LTC2050	●		± 75	± 150 ± 300	pA pA
	LTC2050HV	●		± 7	± 50 ± 150	pA pA
Input Offset Current	LTC2050	●			± 300 ± 400	pA pA
	LTC2050HV	●			± 100 ± 200	pA pA
Input Noise Voltage	$R_S = 100\Omega$, 0.01Hz to 10Hz			1.5		$\mu\text{V}_{\text{P-P}}$
Common Mode Rejection Ratio	$V_{\text{CM}} = \text{GND to } (V^+ - 1.3)$	●	120 115	130 130		dB dB
Power Supply Rejection Ratio	$V_S = 2.7\text{V to } 6\text{V}$	●	120 115	130 130		dB dB
Large-Signal Voltage Gain	$R_L = 10\text{k}$	●	125 120	140 140		dB dB
Output Voltage Swing High	$R_L = 2\text{k to GND}$	●	4.85	4.94		V
	$R_L = 10\text{k to GND}$	●	4.95	4.98		V
Output Voltage Swing Low	$R_L = 2\text{k to GND}$	●		1	10	mV
	$R_L = 10\text{k to GND}$	●		1	10	mV
Slew Rate				2		V/ μs
Gain Bandwidth Product				3		MHz
Supply Current	$V_{\text{SHDN}} = V_{\text{IH}}$, No Load	●		0.8	1.2	mA
	$V_{\text{SHDN}} = V_{\text{IL}}$	●			15	μA
Shutdown Pin Input Low Voltage (V_{IL})		●			$V^- + 0.5$	V
Shutdown Pin Input High Voltage (V_{IH})		●	$V^+ - 0.5$			V
Shutdown Pin Input Current	$V_{\text{SHDN}} = \text{GND}$	●		-0.5	-7	μA
Internal Sampling Frequency				7.5		kHz

ELECTRICAL CHARACTERISTICS (LTC2050HV) The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 5\text{V}$ unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	(Note 2)			± 0.5	± 3	μV
Average Input Offset Drift	(Note 2)	●			± 0.03	$\mu\text{V}/^\circ\text{C}$
Long-Term Offset Drift				50		$\text{nV}/\sqrt{\text{mo}}$
Input Bias Current		●		± 25	± 125 ± 300	pA pA
Input Offset Current		●			± 250 ± 500	pA pA
Input Noise Voltage	$R_S = 100\Omega$, 0.01Hz to 10Hz			1.5		$\mu\text{V}_{\text{P-P}}$
Common Mode Rejection Ratio	$V_{\text{CM}} = V^-$ to $(V^+ - 1.3)$		120	130		dB
	$V_{\text{CM}} = V^-$ to $(V^+ - 1.3)$	●	115	130		dB
Power Supply Rejection Ratio	$V_S = 2.7\text{V}$ to 11V	●	120	130		dB
		●	115	130		dB
Large-Signal Voltage Gain	$R_L = 10\text{k}$		125	140		dB
		●	120	140		dB
Maximum Output Voltage Swing	$R_L = 2\text{k}$ to GND	●	± 4.75	± 4.94		V
	$R_L = 10\text{k}$ to GND	●	± 4.90	± 4.98		V
Slew Rate				2		$\text{V}/\mu\text{s}$
Gain Bandwidth Product				3		MHz
Supply Current	$V_{\text{SHDN}} = V_{\text{IH}}$, No Load	●		1	1.5	mA
	$V_{\text{SHDN}} = V_{\text{IL}}$	●			25	μA
Shutdown Pin Input Low Voltage (V_{IL})		●			$V^- + 0.5$	V
Shutdown Pin Input High Voltage (V_{IH})		●	$V^+ - 0.5$			V
Shutdown Pin Input Current	$V_{\text{SHDN}} = V^-$	●		-3	-20	μA
Internal Sampling Frequency				7.5		kHz

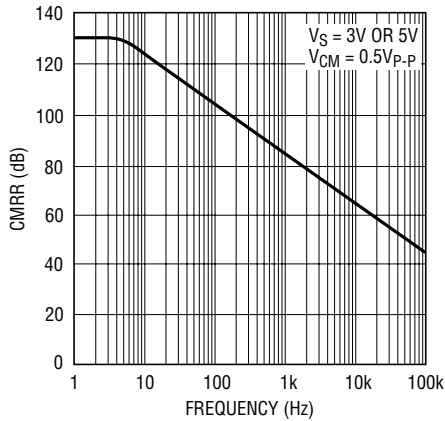
Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: These parameters are guaranteed by design. Thermocouple effects preclude measurements of these voltage levels during automated testing.

Note 3: The LTC2050C, LTC2050HVC are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and expected to meet these extended temperature limits, but are not tested at -40°C and 85°C . The LTC2050I, LTC2050HVI are guaranteed to meet specified performance from -40°C to 85°C .

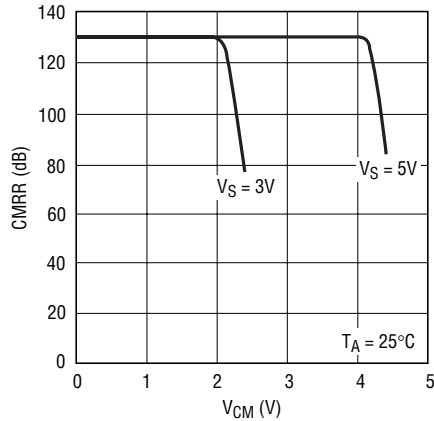
TYPICAL PERFORMANCE CHARACTERISTICS

Common Mode Rejection Ratio vs Frequency



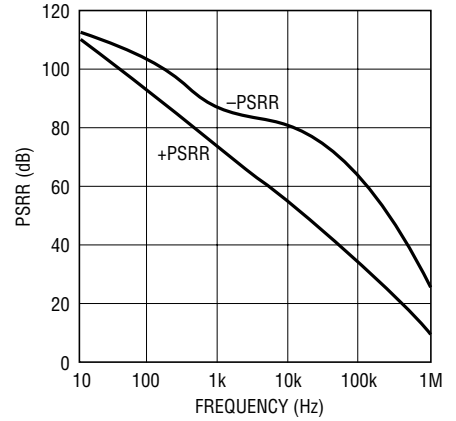
2050 G01

DC CMRR vs Common Mode Input Voltage



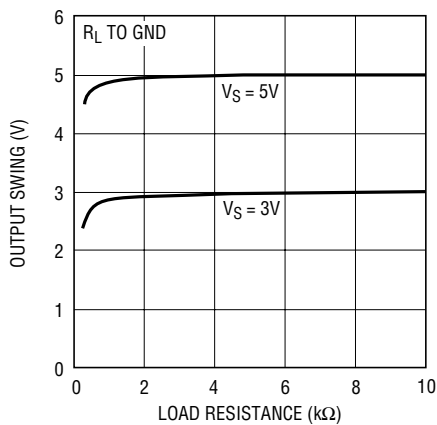
2050 G02

PSRR vs Frequency



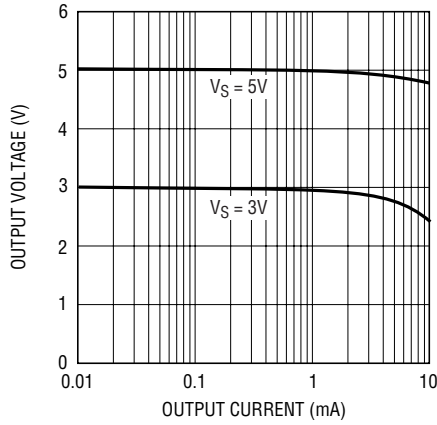
LTC2050 • G14

Output Voltage Swing vs Load Resistance



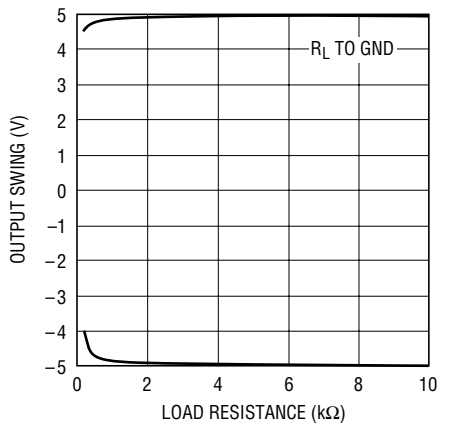
2050 G03

Output Swing vs Output Current



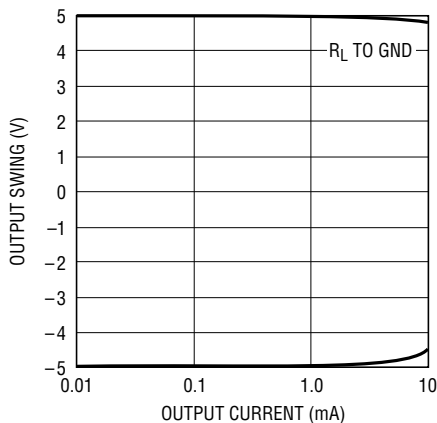
2050 G04

Output Swing vs Load Resistance $\pm 5V$ Supply



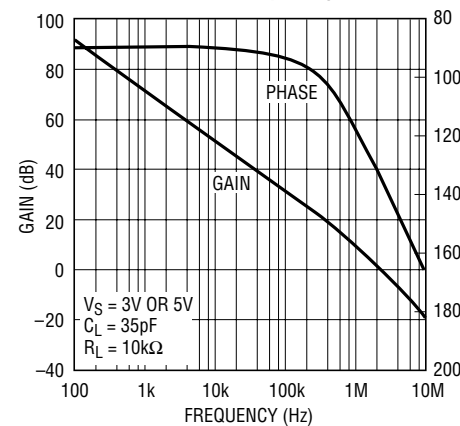
2050 G16

Output Swing vs Output Current $\pm 5V$ Supply



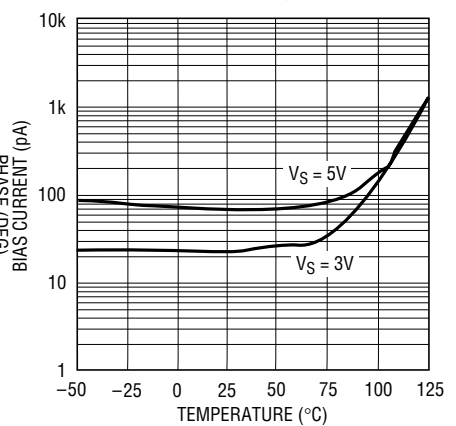
2050 G17

Gain/Phase vs Frequency



2050 G05

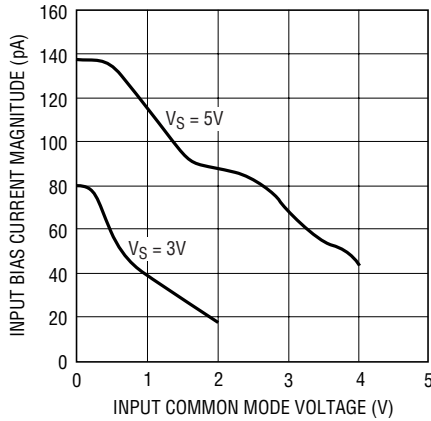
Bias Current vs Temperature



2050 G06

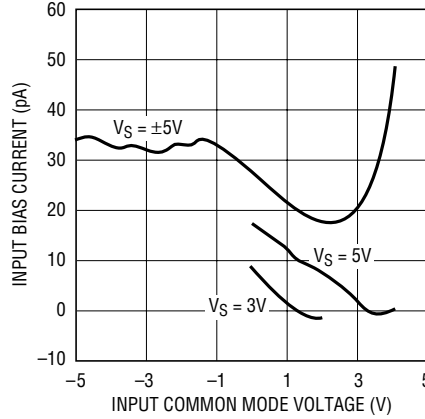
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Input Common Mode Voltage



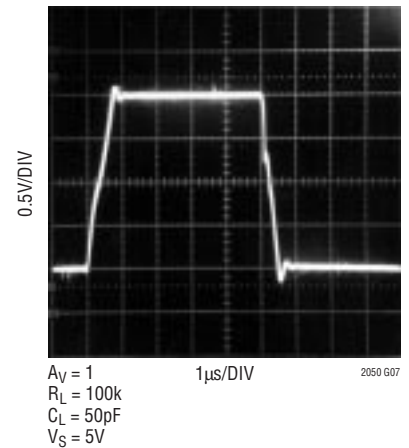
2050 G13

Input Bias Current vs Input Common Mode Voltage (LTC2050HV)



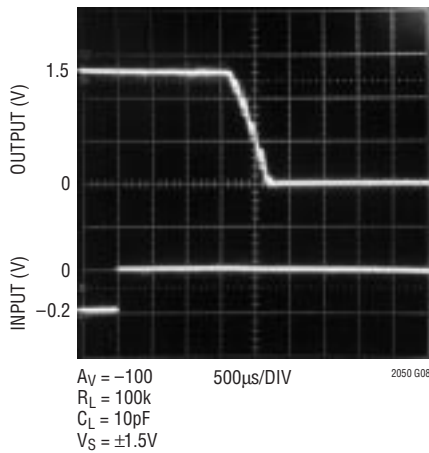
2050 G15

Transient Response



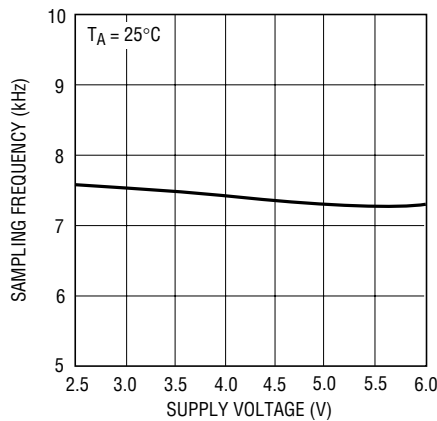
2050 G07

Input Overload Recovery



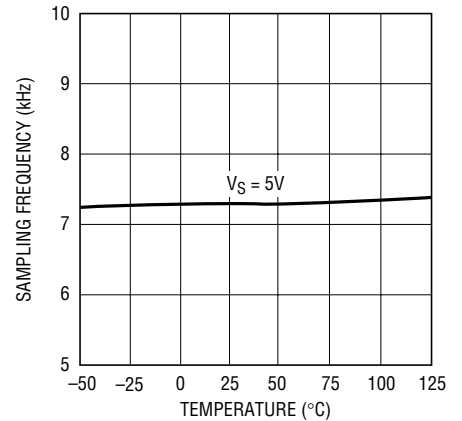
2050 G08

Sampling Frequency vs Supply Voltage



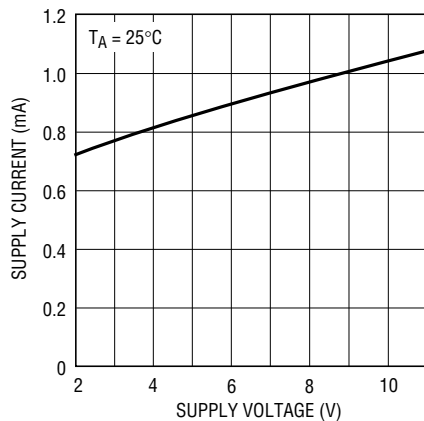
2050 G09

Sampling Frequency vs Temperature



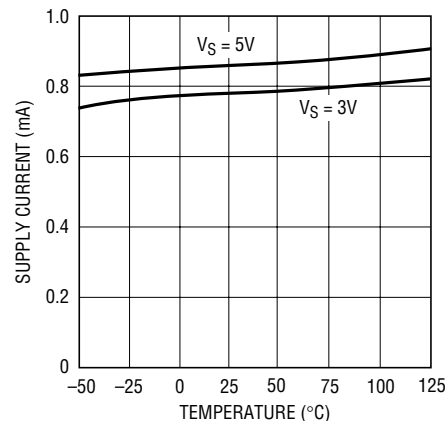
2050 G10

Supply Current vs Supply Voltage



2050 G11

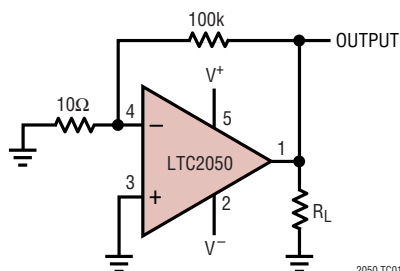
Supply Current vs Temperature



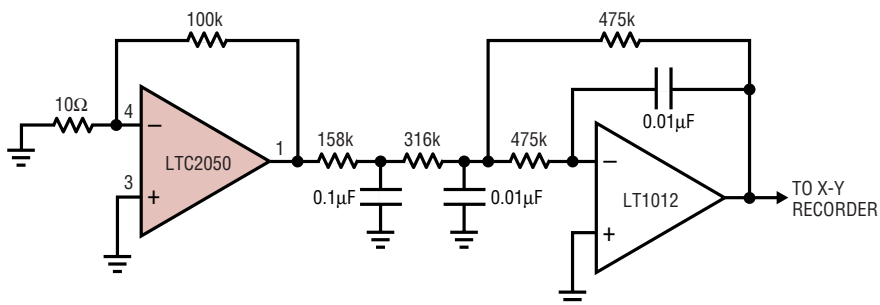
2050 G12

TEST CIRCUITS

Electrical Characteristics
Test Circuit



DC-10Hz Noise Test Circuit



FOR 1Hz NOISE BW INCREASE ALL THE CAPACITORS BY A FACTOR OF 10.

2050 TC02

APPLICATIONS INFORMATION

Shutdown

The LTC2050 includes a shutdown pin in the 6-lead SOT-23 and the SO-8 version. When this active low pin is high or allowed to float, the device operates normally. When the shutdown pin is pulled low, the device enters shutdown mode; supply current drops to 3μA, all clocking stops, and both inputs and output assume a high impedance state.

Clock Feedthrough, Input Bias Current

The LTC2050 uses auto-zeroing circuitry to achieve an almost zero DC offset over temperature, common mode voltage, and power supply voltage. The frequency of the clock used for auto-zeroing is typically 7.5kHz. The term clock feedthrough is broadly used to indicate visibility of this clock frequency in the op amp output spectrum. There are typically two types of clock feedthrough in auto zeroed op amps like the LTC2050.

The first form of clock feedthrough is caused by the settling of the internal sampling capacitor and is input referred; that is, it is multiplied by the closed loop gain of

the op amp. This form of clock feedthrough is independent of the magnitude of the input source resistance or the magnitude of the gain setting resistors. The LTC2050 has a residue clock feedthrough of less than 1μV_{RMS} input referred at 7.5kHz.

The second form of clock feedthrough is caused by the small amount of charge injection occurring during the sampling and holding of the op amp's input offset voltage. The current spikes are multiplied by the impedance seen at the input terminals of the op amp, appearing at the output multiplied by the closed loop gain of the op amp. To reduce this form of clock feedthrough, use smaller valued gain setting resistors and minimize the source resistance at the input. If the resistance seen at the inputs is less than 10k, this form of clock feedthrough is less than 1μV_{RMS} input referred at 7.5kHz, or less than the amount of residue clock feedthrough from the first form described above.

Placing a capacitor across the feedback resistor reduces either form of clock feedthrough by limiting the bandwidth of the closed loop gain.

APPLICATIONS INFORMATION

Input bias current is defined as the DC current into the input pins of the op amp. The same current spikes that cause the second form of clock feedthrough described above, when averaged, dominate the DC input bias current of the op amp below 70°C.

At temperatures above 70°C, the leakage of the ESD protection diodes on the inputs increases the input bias currents of both inputs in the positive direction, while the current caused by the charge injection stays relatively constant. At elevated temperatures (above 85°C) the

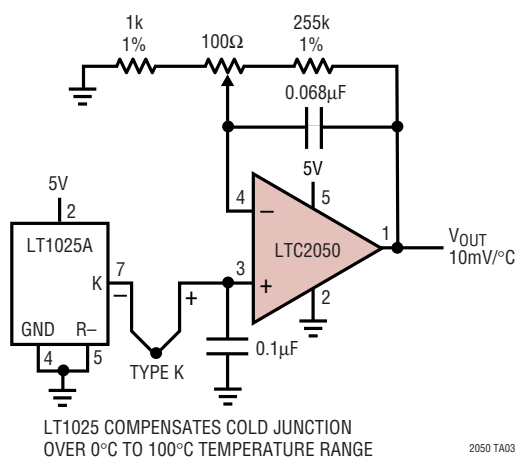
leakage current begins to dominate and both the negative and positive pin's input bias currents are in the positive direction (into the pins).

Input Pins, ESD Sensitivity

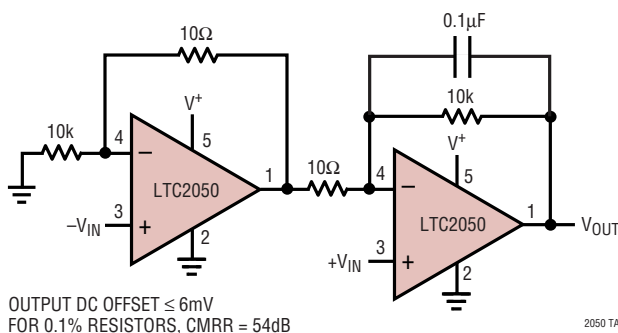
ESD voltages above 700V on the input pins of the op amp will cause the input bias currents to increase (more DC current into the pins). At these voltages, it is possible to damage the device to a point where the input bias current exceeds the maximums specified in this data sheet.

TYPICAL APPLICATIONS

Single Supply Thermocouple Amplifier

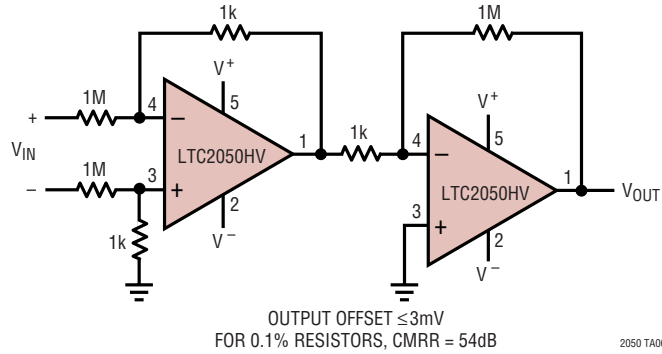


Gain of 1001 Single Supply Instrumentation Amplifier

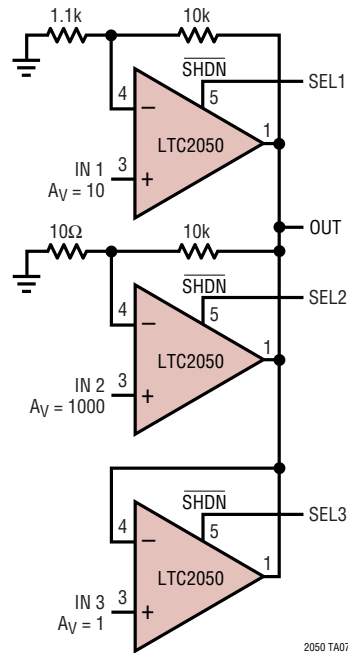


TYPICAL APPLICATIONS

Instrumentation Amplifier with 100V Common Mode Input Voltage



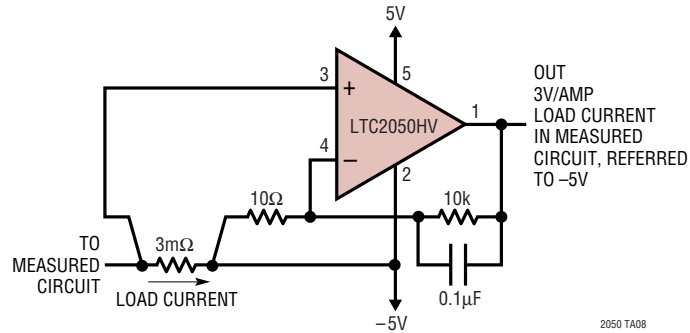
High Precision Three-Input Mux



SELECT INPUTS ARE CMOS LOGIC COMPATIBLE.

TYPICAL APPLICATIONS

Low-Side Power Supply Current Sensing



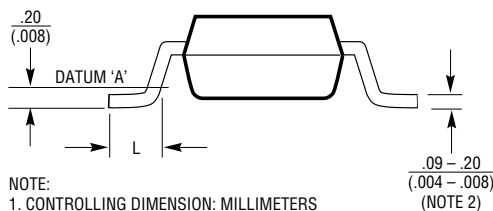
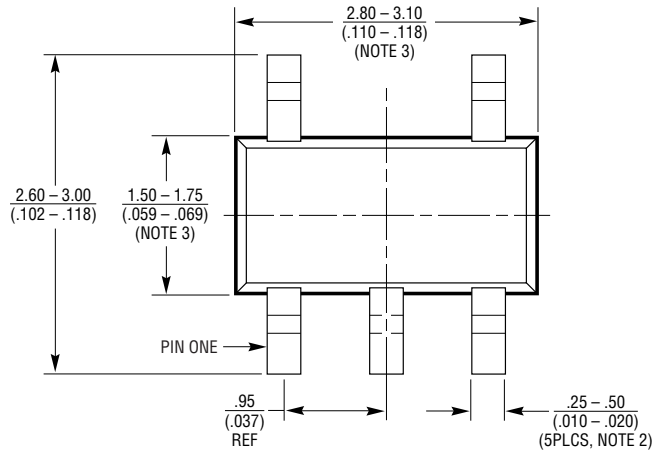
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S5 Package 5-Lead Plastic SOT-23

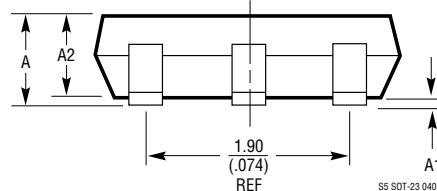
(Reference LTC DWG # 05-08-1633)

(Reference LTC DWG # 05-08-1635)

	SOT-23 (Original)	SOT-23 (ThinSOT)
A	.90 - 1.45 (.035 - .057)	1.00 MAX (.039 MAX)
A1	.00 - .15 (.00 - .006)	.01 - .10 (.0004 - .004)
A2	.90 - 1.30 (.035 - .051)	.80 - .90 (.031 - .035)
L	.35 - .55 (.014 - .021)	.30 - .50 REF (.012 - .019 REF)



- NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
 2. DIMENSIONS ARE IN MILLIMETERS
(INCHES)
 3. DRAWING NOT TO SCALE
 4. DIMENSIONS ARE INCLUSIVE OF PLATING
 5. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
 6. MOLD FLASH SHALL NOT EXCEED .254mm
 7. PACKAGE EIAJ REFERENCE IS:
SC-74A (EIAJ) FOR ORIGINAL
JEDEC MO-193 FOR THIN



S5 SOT-23 0401

PACKAGE DESCRIPTION

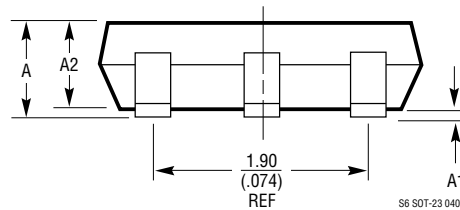
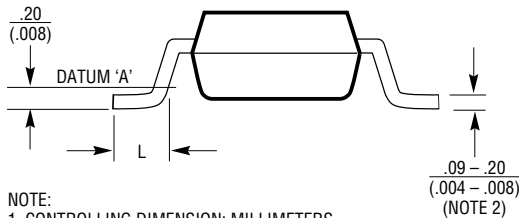
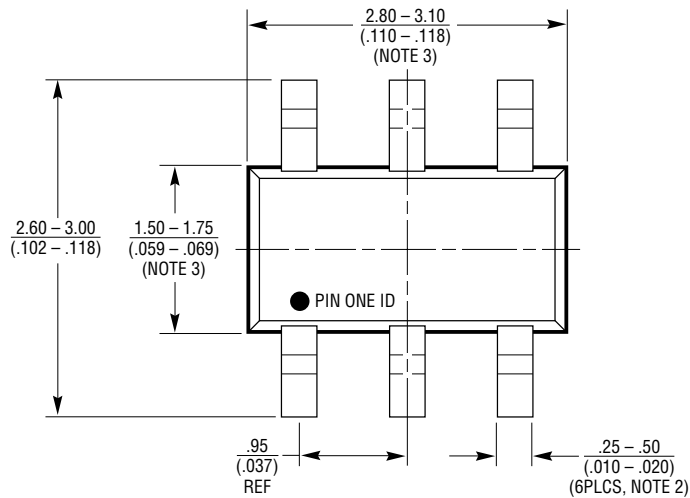
Dimensions in inches (millimeters) unless otherwise noted.

S6 Package**6-Lead Plastic SOT-23**

(Reference LTC DWG # 05-08-1634)

(Reference LTC DWG # 05-08-1636)

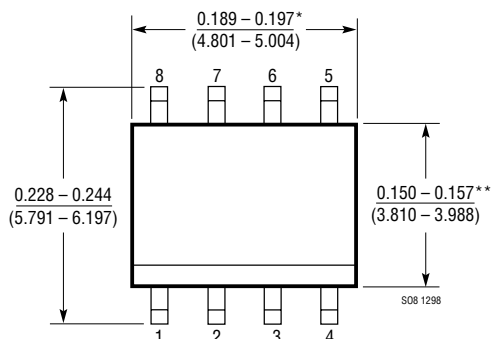
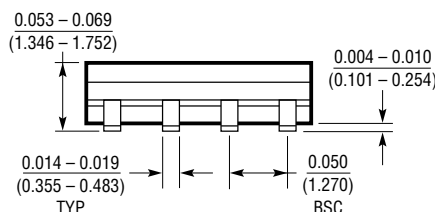
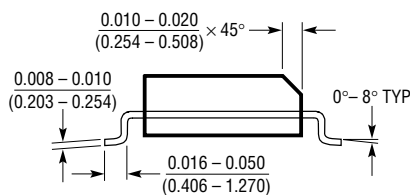
	SOT-23 (Original)	SOT-23 (ThinSOT)
A	$\frac{.90 - 1.45}{(.035 - .057)}$	$\frac{1.00 \text{ MAX}}{(.039 \text{ MAX})}$
A1	$\frac{.00 - 0.15}{(.00 - .006)}$	$\frac{.01 - .10}{(.0004 - .004)}$
A2	$\frac{.90 - 1.30}{(.035 - .051)}$	$\frac{.80 - .90}{(.031 - .035)}$
L	$\frac{.35 - .55}{(.014 - .021)}$	$\frac{.30 - .50 \text{ REF}}{(.012 - .019 \text{ REF})}$

**NOTE:**

1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. DIMENSIONS ARE INCLUSIVE OF PLATING
5. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
6. MOLD FLASH SHALL NOT EXCEED .254mm
7. PACKAGE EIAJ REFERENCE IS:
SC-74A (EIAJ) FOR ORIGINAL
JEDEC MO-193 FOR THIN

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)

(Reference LTC DWG # 05-08-1610)

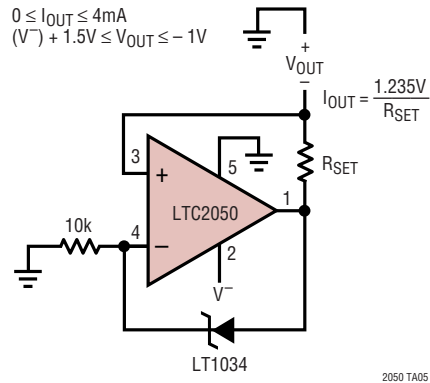
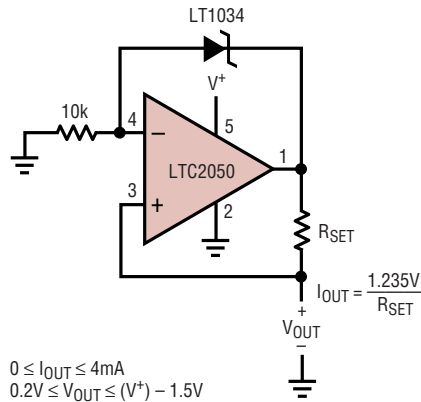


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATIONS

Ground Referred Precision Current Sources



2050 TA05

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1049	Low Power Zero-Drift Op Amp	Low Supply Current 200μA
LTC1050	Precision Zero-Drift Op Amp	Single Supply Operation 4.75V to 16V, Noise Tested and Guaranteed
LTC1051/LTC1053	Precision Zero-Drift Op Amp	Dual/Quad
LTC1150	±15V Zero-Drift Op Amp	High Voltage Operation ±18V
LTC1152	Rail-to-Rail Input and Output Zero-Drift Op Amp	Single Zero-Drift Op Amp with Rail-to-Rail Input and Output and Shutdown
LT1677	Low Noise Rail-to-Rail Input and Output Precision Op Amp	$V_{OS} = 90\mu\text{V}$, $V_S = 2.7\text{V}$ to 44V
LT1884/LT1885	Rail-to-Rail Output Precision Op Amp	$V_{OS} = 50\mu\text{V}$, $I_B = 400\text{pA}$, $V_S = 2.7\text{V}$ to 40V
LTC2051	Dual Zero-Drift Op Amp	Dual Version of the LTC2050 in MS8 Package