International
IOR Rectifier

International
IOR Rectifier

Data Sheet No. PD60225 Rev B

IRMCK203

High Performance Sensorless Motion Control IC

Features

- **Complete Sensorless control IC for Permanent Magnet AC motors**
- **No phase voltage feedback sensing required**
- **Sinusoidal current waveform with Synchronously Rotating Frame closed loop current control**
- **High starting torque and smooth speed ramping**
- **Direct interface to IR2175 current sensing high voltage IC**
- **Auto Retry at startup with configurable starting torque**
- **Versatile loss minimization Space Vector PWM**
- **Serial communication interface (RS232C, RS422, SPI)**
- **I^2C serial interface to 1k bit serial EEPROM for parameter storage for stand alone operation**
- **Phase loss/Overcurrent/Overvoltage protection**
- **7-bit discrete I/O for sequencing and status monitor**
- **Integrated brake IGBT control for dc bus voltage limitation**
- **ServoDesigner™ tool for easy operation**
- **Parallel interface for microcontroller expansion**

Product Summary

Max Clock input	33.3 MHz
Sensorless control computation time	10 µsec max
Speed operating range (typical)	5% to 100%
Speed control resolution	15 bit full range
Adjustable current limit at start-up	15 bit full range
Programmable retry on start-up	max 16 trials
Over current, speed, phase loss, dc bus fault protection	
PWM carrier frequency	16 bit/33MHz
IR2175 Current feedback data resolution	10bit
Inverter leg current sensing (optional)	12bit
RS232C speed	up to 57.6 Kbps
Optional RS422 communication	up to 1 Mbps
Max SPI Clock	8 MHz

Package: QFP80

Description

IRMCK203 is a high performance digital motion control IC for Sensorless AC permanent magnet motor application. Control is based on closed loop vector control for sinusoidal Back EMF motors. With IRMCK203, the users can readily build a high performance Sensorless drive system without any programming effort and minimum start-up time. Built-in unique start-up and ramping algorithm enables wide application. This IC is versatile enough that the users can configure and optimize system performance according to the needs of each application. With International Rectifier iMOTION products including high voltage ICs such as IR2175 current sensing IC and IRAM series of Intelligent IGBT module in combination with IRMCK203, the end result is a fully optimized system with reduced electronics component counts. This simplifies the design for low cost Sensorless drive modules. IRMCK203 can be easily adapted to various permanent magnet motors through ServoDesigner™ tool, which is the fully configurable graphic user interface tool.

Overview

IRMCK203 is a new International Rectifier integrated circuit device designed for one-chip solution for complete closed loop current and velocity control of a high performance Sensorless drive for PM motors. Unlike a traditional microcontroller or DSP, IRMCK203 does not require any programming to complete complex Sensorless algorithm development. Combined with International Rectifier's high voltage gate drive and current sensing IC, the user can implement complete speed control of PM motors with minimum component count and virtually no design effort. In addition to Sensorless closed loop speed control operation, features such as Start-up retry, Phase Loss detection, Low Loss PWM, Regeneration Braking control and various drive protections are all implemented inside IRMCK203. Analog and digital I/Os can also be configured. Host communication logic contains Asynchronous Communication Interface for RS232C or RS422 communication interface, a fast slave SPI interface and an 8 bit wide Host Parallel Interface. All communication ports have the same access capability to the host register set. The users can write to, and read from the predefined registers to configure and monitor the drive through these communication ports.

IRMCK203 Main functions

- Complete closed loop current control based on Synchronously Rotating Frame Field Orientation (using Rotor Angle Observer)
- Closed loop velocity control based on estimated speed
- Configurable parameters (PI controller gains, PI output limit range, current feedback scaling, PWM carrier frequency) provide adaptation to various PM motors
- Built-in Sensorless control logic for start-up, ramping, and running conditions
- Auto Retry (programmable) on start-up with configurable torque current limit
- Analog reference input (can be used for speed reference)
- RS232C/RS422 reference input
- Full dynamic braking control for DC bus voltage limitation
- Cycle-by-cycle on/off Control for Brake IGBT
- Loss minimization Space Vector PWM with deadtime insertion
- Build-in two IR2175 current sensing IC interfaces
- Phase Loss, Overcurrent (GATEKILL input), Overvoltage, Undervoltage, Overspeed protection
- Low cost serial 12bit A/D interface with multiplexer and sample/hold circuit
- Optional Inverter Leg (low side) current sensing in lieu of IR2175 IC
- 4 channel analog output (PWM)
- Local EEPROM for startup initialization of internal data/parameters through host register interface
  AT24C01A, 128X8
- Versatile host communication interface
  RS232C or RS422 host interface
  Fast SPI slave host interface with multi-drop capability
  Parallel Host interface (total 12 pins)
- Multiplexed data/address bus
  Address Enable
  RD/WR
- Discrete I/Os for Standalone mode operation
  STARTSTOP (Input)
  ESTOP (Input)

DIR (Input)
FLTCLR (Input)
FAULT (Output)
SYNC (Output)
REDLED (Output)
GREENLED (Output)

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IRMCK203 Block Diagrams

Basic Block Diagram

Figure 1 shows the basic block diagram of the IRMCK203 surrounded by International Rectifiers' ICs. Host communications are provided over SPI, RS-232C or Host parallel ports. Two current sensing ICs (IR2175) and a three phase high voltage gate drive typically implement the high voltage / current interface between the IRMCK203 IC and motor.

The IRMCK203 can operate in a "stand-alone" mode without the host controller. A serial EEPROM would be utilized to load motor-specific parameters into the IC.

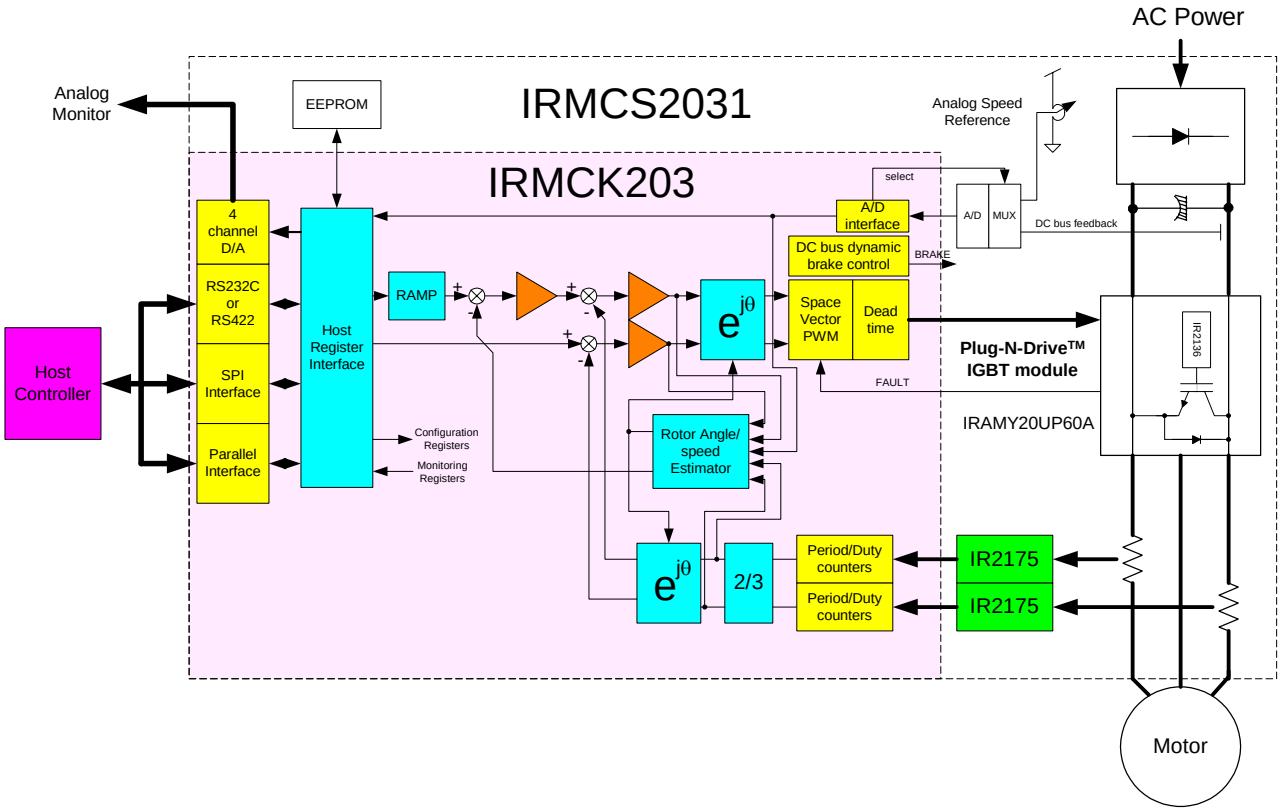


Figure 1: IRMCS2031 Simplified Blocks

Configurable parameters are provided to tailor design to various applications (motor and load). These configurable parameters can be modified via the host register interface through the communication interface. In the IRMCK203 product, a design spread sheet is provided to aid the user for ease of drive start-up, the spread sheet will input high level application data such as motor name plate information, max speed, current limit, speed and current regulator bandwidth, base on this information the program will generate the required configurable parameters. Detail on Drive commissioning is described in the IRMCK203 Application Developer's Guide.

All logic and algorithms are pre-programmed, and the user does not need to make any effort to develop code, alleviating the tedious design process. If needed, the user can configure the drive to tailor the control per specific

needs to meet the required specification. This configuration can be easily done by accessing the host register interface through the communication interface.

Input/Output of IRMCK203

The I/O signals are shown in Figure 2. The interface signals are divided into sub-groups. For detailed pin assignment, please refer to appendix (Pin definition).

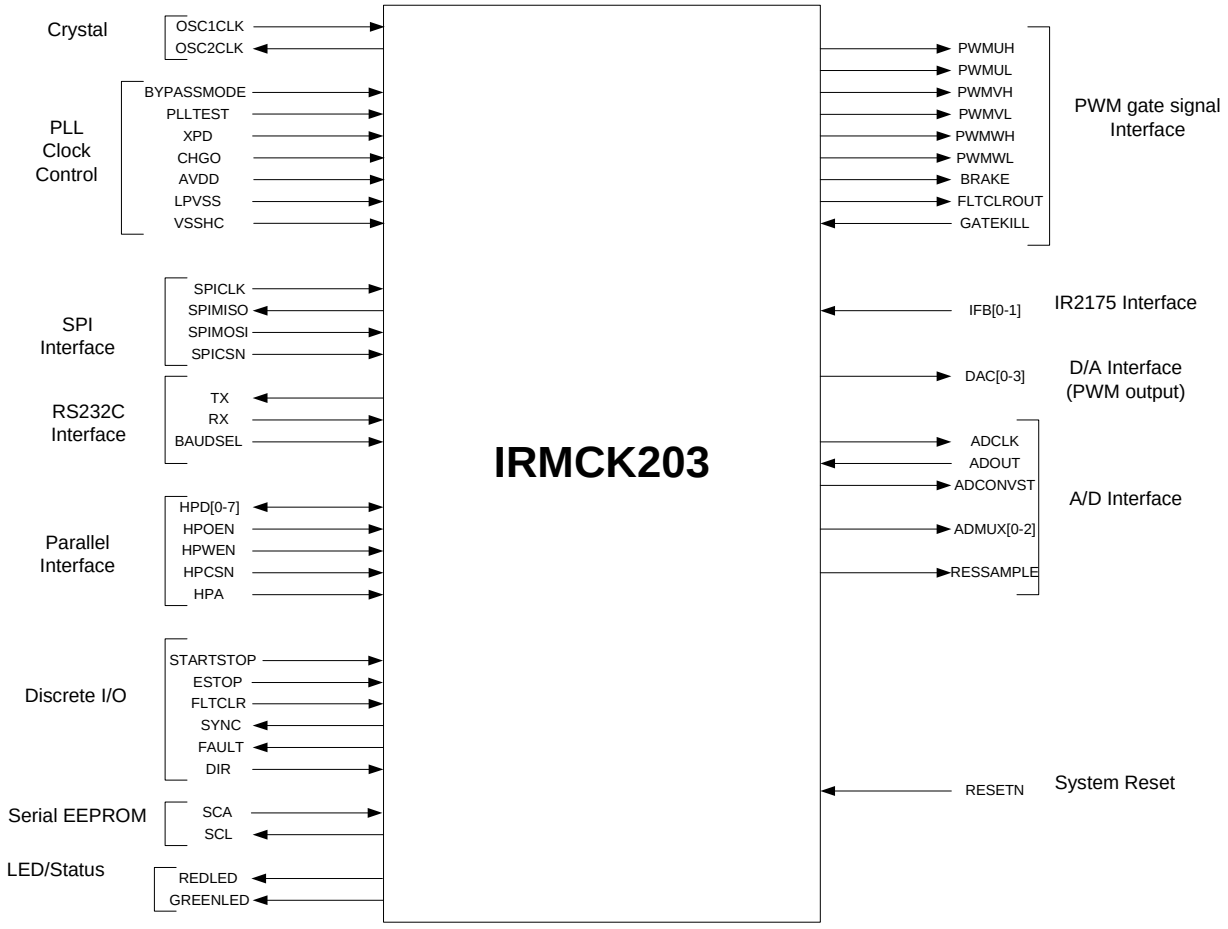


Figure 2: Input/Output of IRMCK203

Host Interface Group			
Signal	**Input (I) / Output (O)**	**Low (L) / High (H) True Asserted**	**Function**
SPICLK	I	Positive edge sensitive	SPI clock
SPIMISO	O	-	Master input and slave output
SPIMOSI	I	-	Master output and slave input
SPICSN	I	L	SPI chip select
HP_nOE	I	L	Parallel data output enable
HP_nWE	I	L	Parallel data write cycle identification
HP_D [7:0]	I/O	-	Parallel data
HP_A	I	H	Parallel data address cycle identification
HP_nCS	I	L	Chip select
TX	O	-	RS-232 data out
RX	I	-	RS-232 data in
BAUDSEL[1:0]	I	H	RS-232 baud rate: 00 = 19.3K bps; 01 = 38.4K bps 10 = 57.6K bps; 11 = 1.031250M bps
SYNC	O	L	Start of PWM cycle
CLK1XOUT	O	-	33.333 MHz output of PLL. This signal has no phase relationship with the OSC1CLK or OSC2CLK inputs.

Discrete I/O Group			
Signal	**Input (I) / Output (O)**	**Low (L) / High (H) True Asserted**	**Function**
STARTSTOP	I	H	Start / Stop command edge sensitive
DIR	I	H	Forward/Reverse Direction command, level sensitive
FAULTCLR	I	H	Fault Clear
ESTOP	I	H	Emergency Stop, state sensitive
PWEN	O	H	PWM enable/disable state
SYNC	O	H	SYNC pulse
FAULT	O	H	Fault state

Motion Peripheral Group			
Signal	**Input (I) / Output (O)**	**Low (L) / High (H) True Asserted**	**Function**
PWMUH	O	-	PWM phase U high side
PWMUL	O		PWM phase U low side
PWMVH	O		PWM phase V high side
PWHVL	O		PWM phase V low side
PWMWH	O		PWM phase W high side
PWMWL	O		PWM phase W low side
BRAKE	O	L	IGBT gate
GATEKILL	I	Varies, Based on Write Register 0x0C Bit 7	When asserted, negates all six PWM signals, host writeable
IFB0	I	-	Channel 0 (phase V)
IFB1	I	-	Channel 1 (phase W)

Analog Interface Group			
Signal	**Input (I) / Output (O)**	**Low (L) / High (H) True Asserted**	**Function**
ADCLK	O	Negative Edge Sensitive	Clock to ADS7818
ADOUT	I	-	Serial data from ADS7818
DAC [3:0]	O	-	Diagnostic DAC
ADCONVST	O	L	Conversion start to ADS7818
RESSAMPLE	O		Sample/hold control signal channel 0 A/D converter
ADMUX0	O	H	Analog input MUX select
ADMUX1	O	H	Analog input MUX select

PLL Interface Group			
Signal	**Input (I) / Output (O)**	**Low (L) / High (H) True Asserted**	**Function**
XPD	I	L	PLL reset
RESETN	I	L	Digital logic reset
BYPASSCLK	I	H	Internal test pin – force to logic low
BYPASSMODE	I	H	Internal test pin – force to logic low
OSC1CLK	I	-	33.33 MHz crystal input
OSC2CLK	I	-	33.33 MHz crystal input
PLLTEST	I	H	Internal test pin – force to logic low
CHGO	I/O	-	Low pass filter
LPVSS	I/O	-	Low pass filter ground

Miscellaneous Group			
Signal	**Input (I) / Output (O)**	**Low (L) / High (H) True Asserted**	**Function**
SCA	I/O	-	EEPROM data
SCL	O	Positive Edge Sensitive	EEPROM clock
GREENLED	O	H	LED signal
REDLED	O	H	LED signal

Power Supply Group	
Signal	**Function**
LVDD	IC Logic +3.3V power supply
AVDD	IC Phase Lock Loop +3.3V analog power supply
MVDD	IC Phase Lock Loop +3.3V digital power supply
VSS	IC Logic power supply return
VSSHC	IC Phase Lock Loop power supply return

Application Connections

Typical application connection is shown in Figure 3. In order to complete a Sensorless drive control, all necessary components are shown in connection to IRMCK203.

Although this is a typical hardware configuration, users can customize the design without the effort of modifying code.

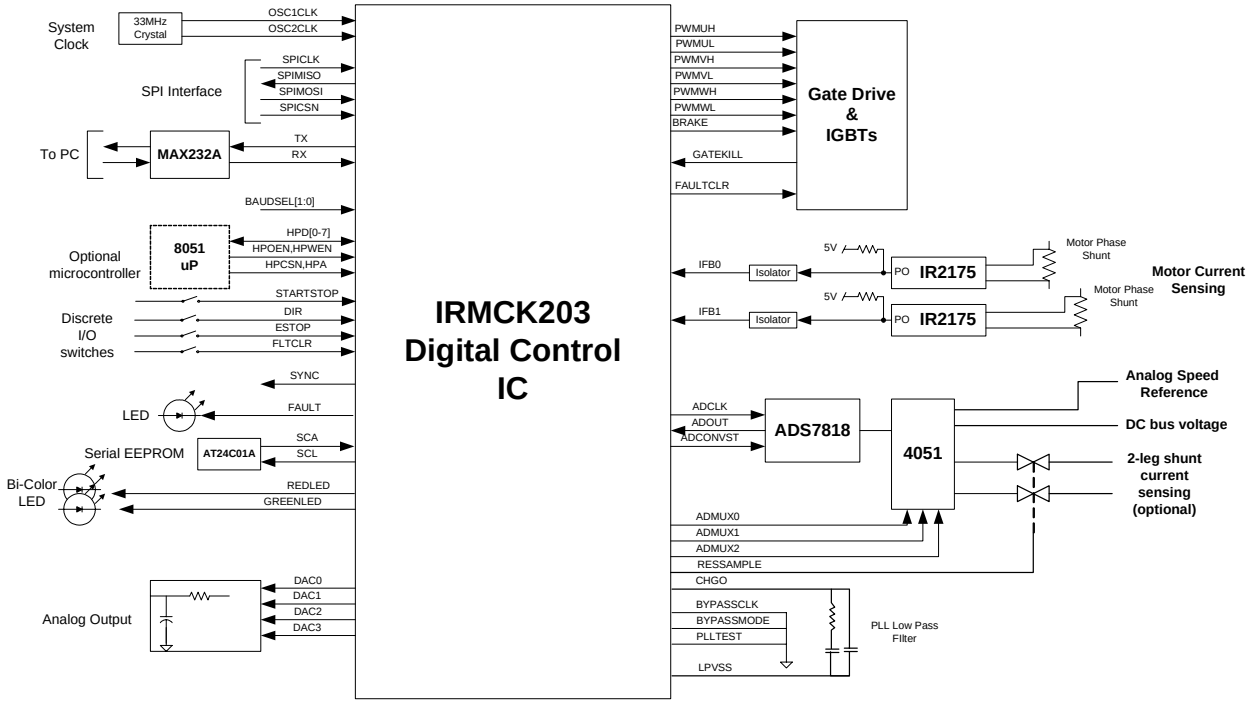


Figure 3: Application Connection of IRMCK203

IC Crystal Clock Circuitry

The clock input to the IC is a 33.33 MHz crystal oscillator. Two shunt capacitors and a possibly a series resistor is required to terminate the crystal to the IC.

The values of the R/C will vary based on actual PCB attributes, and some empirical analysis may be required to get the PLL to start oscillating. Once oscillating, verify that the signal waveform at the OSC1CLK and OSC2CLK pins are sinusoidal rather than trapezoidal. Refer to Table 1 for suggested R/C values. Most low-cost crystals can be used in this application. An example is a Citizen Part number CM309B33.333MABJT available from Digi-Key under part number 300-4160-1-ND.

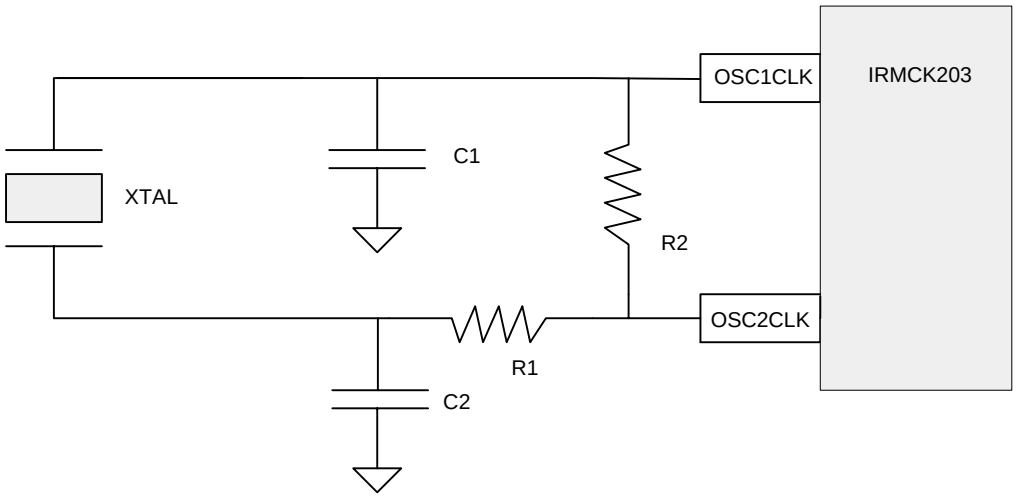


Figure 4: Oscillator Circuit

Component	Value	Units
XTAL	33.33	MHz
C1	5	pF
C2	5	pF
R1	0	Ω
R2	3.9K	Ω

Table 1: Typical Values for the Clock Circuit

PLL Clock Circuitry

The IRMCK203 contains a PLL that creates a 2X and 4X clock from the input 33.33 MHz input clock pin. There are a number of pins on the IC allocated for factory testing purposes that need to be **connected to VSS.** Table 2 shows required PCB signal connections for these pins.

Pin Number	PCB Connection
1	VSS
7	VSS

Table 2: PLL Test Pin Assignments

Low Pass Filter

The low pass filter for this PLL resides between the CHGO and LPVSS pins. Three passive components are required to implement this filter: Cp, Rp and Cs.

Figure 5 shows how to place these components around the IC.

A shield should be placed below Rp, Cp and Cs made out of copper etch.

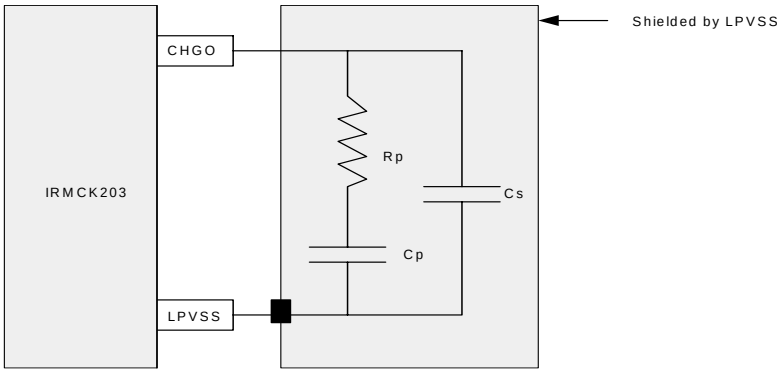


Figure 5: PLL Low Pass Filter Shielding

Implementing the Low Pass Filter Shield

Make all connections between CHGO, Rp, Cp, Cs and LPVSS as short as possible. Create the underlining shield by "copper filling" a larger area in the signal plane of the PCB. Connect this shield to the LPVSS pin of the IC. Do not connect this shield to signal ground (VSS).

Cp Rp and Cs Component Values

For a typical FR4 PCB, the values of the passive components are shown in Table 3.

Component	Value	Units
Rp	3.9K	Ω
Cp	1000	pF
Cs	Not Installed	-

Table 3: PLL Low Pass Filter Values

PLL Reset

There are two reset pins on the IC, XPD and RESETN both low true. XPD holds the PLL circuitry in reset when low. Upon XPD going high, the PLL circuitry begins to lock onto the 33.33 MHz clock input. The PLL circuit may take up to 1 msec to become stable. RESETN asserted low holds the internal DSP logic in reset. Upon RESETN going high, the IC digital logic becomes active.

RESET should be held low during and at least 1 ms after XPD goes high false to hold the internal logic in reset while the PLL becomes stable.

DC Electrical Characteristics and Operating Conditions

Absolute Maximum Ratings

Note: VSS = 0 Volt

PARAMETER	SYMBOL	LIMITS	UNITS	NOTE
Power Supply Voltage	VDD	VSS-0.3 to 4.0	V	
Input Voltage	VI	VSS-0.3 to VDD+0.5	V	Non 5 Volt Tolerant Pins (Table 11)
Input Voltage	VI	VSS-0.3 to 7	V	Only on 5 Volt Tolerant Pins (Table 11)
Output Voltage	VO	VSS-0.3 to VDD+0.5	V	
Output Current per Pin	IOUT	+/- 30	mA	
Storage Temperature	Tstg	-65 to 150	°C	

Table 4: Absolute Maximum Ratings

Recommended Operating Conditions

Note: VSS = 0 Volt

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTE
Power Supply Voltage	VDD	3.0	3.3	3.6	V	
Input Voltage	VI	VSS	-	VDD	V	Non 5 Volt Tolerant Pins (Table 11)
Input Voltage	VI	VSS	-	5.5	V	Only on 5 Volt Tolerant Pins (Table 11)
Ambient Temperature	Ta	-40	-	85	°C	Note 2

Table 5: Recommended Operating Conditions

Notes:
2. The ambient temperature range is recommended for Tj= -40 to 125 °C

DC Characteristics

Common Quiescent and Leakage Current

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current	IDDS	VI=VDD or VSS VDD=MAX IOH=IOL=0 Ta=Tj=85°C	-	-	.35	uA
Input Leakage Current	ILI	VDD=MAX VIH=VDD VIL=VSS	-1	-	1	uA

Table 6: DC Characteristics

Input Characteristics – Non Schmitt Inputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage	VIH1	VDD=MAX	2.0	-	-	V
Low Level Input Voltage	VIL1	VDD=MIN	-	-	0.8	V

Table 7: Non Schmitt Input Characteristics

Input Characteristics – Schmitt Inputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage	VT1+	VDD=MAX	1.1	-	2.4	V
Low Level Input Voltage	VT1-	VDD=MIN	0.6	-	1.8	V
Hysteresis Voltage	VH1	VDD=MIN	0.1	-	-	V

Table 8: Schmitt Input Characteristics

Output Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Output Voltage	VOH3	VDD=MIN IOH=-12mA	VDD - 0.4	-	-	V
Low Level Output Voltage	VOL3	VDD=MIN IOH = 12mA	-	-	VSS + 0.4	V

Table 9: Output Characteristics

Output Characteristics OSC2CLK

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Output Voltage	LVOH	VDD=MIN IOH=-530uA	VDD - 0.4	-	-	V
Low Level Output Voltage	LVOL	VDD=MIN IOH = 730uA	-	-	VSS + 0.4	V

Table 10: Output Characteristics OSC2CLK

Pin and I/O Characteristic Table

Pin Number	Pin Name	INTERNAL IC RESISTOR TERMINATION	Pin Type	5.50 VOLT TOLERANT INPUT	INPUT DC CHARACTERISTIC TABLE	OUTPUT DC CHARACTERISTIC TABLE
1	BYPASSMODE	40K-240K Pull Down	I	-	Table 8	-
2	FLTCLROUT		O	-	-	Table 9
3	OSC1CLK		I	-	Table 7	
4	LVDD		P	-	-	-
5	OSC2CLK		O	-		Table 10
6	VSS		P	-	-	-
7	PLLTEST	20K-120K Pull Down	I	-	Table 7	-
8	XPD		I	-	Table 7	-
9	VSSHC		P	-	-	-
10	MVDD		P	-	-	-
11	VSSHC		P	-	-	-
12	AVDD		P	-	-	-
13	CHGO		O	-	-	-
14	LPVSS		P	-	-	-
15	DIR	20K – 120K Pull Down	I	YES	Table 8	-
16	RESETN	20K -120K Pull Up	I	-	Table 8	-
17	SPICSN		I	-	Table 8	-
18	REDLED		O	-	-	Table 9
19	GREENLED		O	-	-	Table 9
20	VSS		P	-	-	-
21	PWMWL		O	-	-	Table 9
22	PWMWH		O	-	-	Table 9
23	PWMVL		O	-	-	Table 9
24	LVDD		P	-	-	-
25	PWMVH		O	-	-	Table 9
26	PWMUL		O	-	-	Table 9
27	VSS		P	-	-	-
28	PWMUH		O	-		Table 9
29	BRAKE		O	-	-	Table 9
30	BAUDSEL0	20K – 120K Pull Down	I	YES	Table 8	
31	GATEKILL	20K -120K Pull Up	I	-	Table 8	-
32	IFB1		I	YES	Table 8	-
33	IFB2		I	YES	Table 8	-
34	LVDD		P	-	-	-
35	CLK1XOUT		O	-	-	Table 9
36	VSS		P	-		
37	SPIMOSI		I	YES	Table 8	
38	SPIMISO		O	-	-	Table 9
39	SPICLK		I	YES	Table 8	-
40	TX		O	-	-	Table 9

Pin Number	Pin Name	INTERNAL IC RESISTOR TERMINATION	Pin Type	5.50 VOLT TOLERANT INPUT	INPUT DC CHARACTERISTIC TABLE	OUTPUT DC CHARACTERISTIC TABLE
41	RX		I	YES	Table 8	-
42	BAUDSEL1	20K -120K Pull Up	I	YES	Table 8	-
43	LVDD		P	-	-	-
44	ADMUX0		O	-	-	Table 9
45	VSS		P	-	-	-
46	ADMUX1		O	-	-	Table 9
47	ADMUX2		O	-	-	Table 9
48	RESSAMPLE		O	-	-	Table 9
49	ADCONVST		O	-	-	Table 9
50	ADCLK		O	-	-	Table 9
51	ADOUT		I	YES	Table 8	-
52	SYNC		O	-	-	Table 9
53	FAULT		O	-	-	Table 9
54	STARTSTOP	20K -120K Pull Down	I	YES	Table 8	-
55	ESTOP	20K -120K Pull Down	I	YES	Table 8	-
56	FLTCLR	20K -120K Pull Down	I	YES	Table 8	-
57	LVDD		P	-	-	-
58	PWMEN		O	-	-	Table 9
59	DAC3		O	-	-	Table 9
60	VSS		P	-	-	-
61	DAC2		O	-	-	Table 9
62	DAC1		O	-	-	Table 9
63	DAC0		O	-	-	Table 9
64	HP_D0	20K -120K Pull Down	B	-	Table 7	Table 9
65	HP_D1	20K -120K Pull Down	B	-	Table 7	Table 9
66	HP_D2	20K -120K Pull Down	B	-	Table 7	Table 9
67	LVDD		P	-	-	-
68	HP_D3	20K -120K Pull Down	B	-	Table 7	Table 9
69	HP_D4	20K -120K Pull Down	B	-	Table 7	Table 9
70	VSS		P	-	-	-
71	HP_D5	20K -120K Pull Down	B	-	Table 7	Table 9
72	HP_D6	20K -120K Pull Down	B	-	Table 7	Table 9
73	HP_D7	20K -120K Pull Down	B	-	Table 7	Table 9
74	HP_nOE		I	YES	Table 8	-
75	HP_nWE		I	YES	Table 8	
76	HP_A		I	YES	Table 8	-
77	HP_nCS		I	YES	Table 8	-

Pin Number	Pin Name	INTERNAL IC RESISTOR TERMINATION	Pin Type	5.50 VOLT TOLERANT INPUT	INPUT DC CHARACTERISTIC TABLE	OUTPUT DC CHARACTERISTIC TABLE
78	VSS		P	-	-	
79	SCL		O	-	-	Table 9
80	SDA	20K -120K Pull Up	B	-	Table 7	Table 9

Table 11: Pin and I/O Characteristics

Power Consumption

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
P_{Total}	PTOTAL	VDD=3.3V	-	1.2	-	WATT

Table 12: IRMCK203 Power Consumption

AC Electrical Characteristics and Operating Conditions

System Level AC Characteristics

Sync Pulse to Sync Pulse Timing

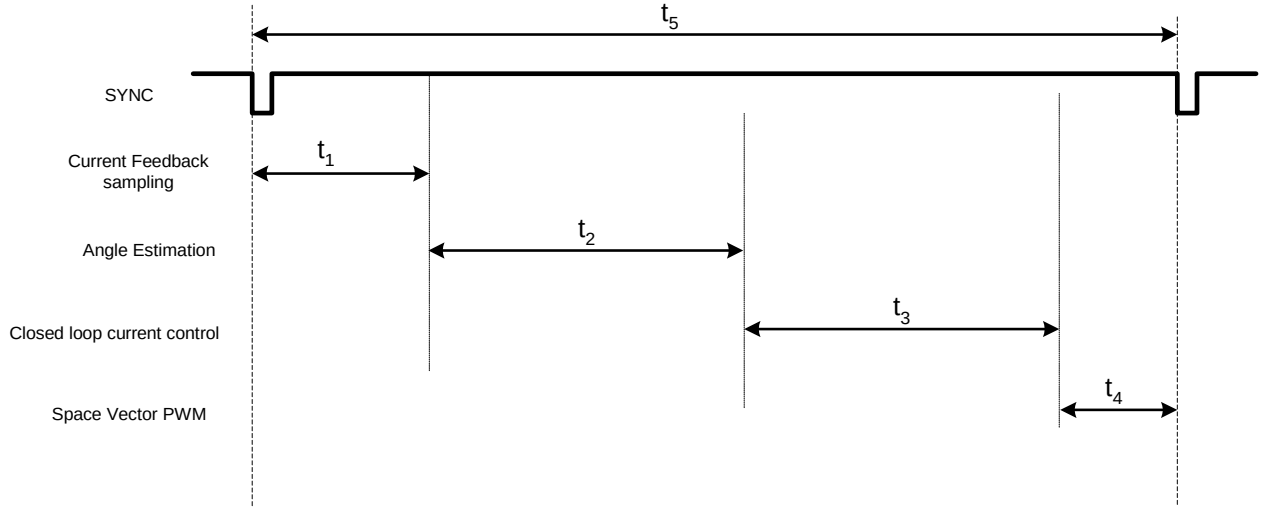


Figure 6: System Level SYNC To SYNC Timing

SYMBOL	DESCRIPTION	TIME (µsec)
t_1	Current Feedback Sample Delay Using IR2175 for current feedback Using Leg Shunts for current feedback (optional)	 4.3 2.0
t_2	Rotor Angle Estimation Time	4.9
t_3	Current and velocity control	3.1
t_4	Space Vector PWM calculation time	2.3
t_5	Total SYNC to SYNC minimum time	14.6 (max)

Table 13: System Level SYNC to SYNC Timing

FAULT and REDLED Response to GATEKILL

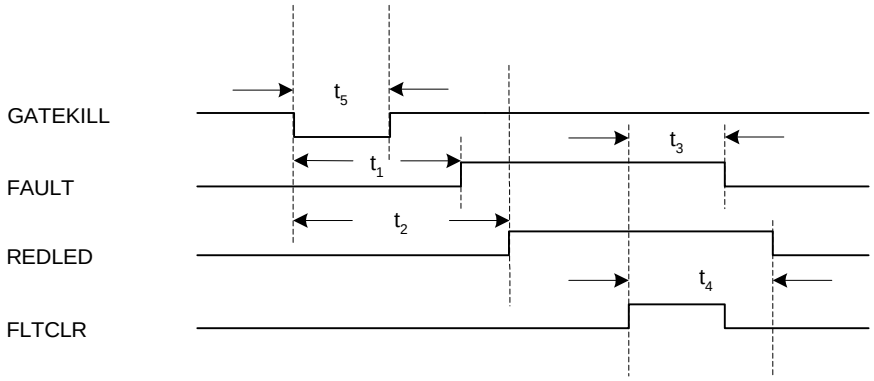


Figure 7: FAULT and REDLED Response to GATEKILL

SYMBOL	DESCRIPTION	MIN	TYP	UNITS
t_1	FAULT Response to GATEKILL		640	ns
t_2	REDLED Response to GATEKILL		640	ns
t_3	FAULT Response to FLTCLR		190	ns
t_4	REDLED Response to FLTCLR		190	ns
t_5	GATEKILL Pulse Width	485		ns

Table 14: FAULT and REDLED Response to GATEKILL

Host Interface AC Characteristics

SPI Timing

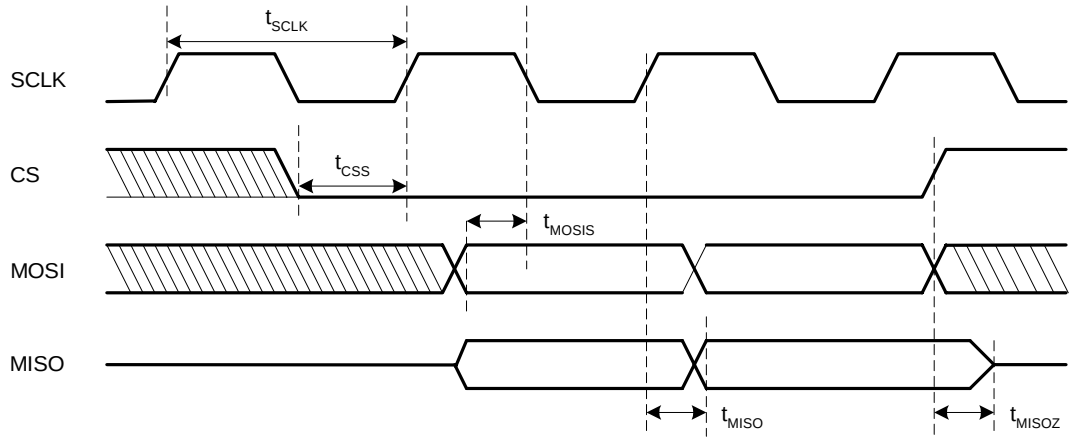


Figure 8: SPI Timing

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
f_{SCLK}	SPI Clock Frequency		8	MHz
t_{SCLK}	SPI Clock Period	125		ns
t_{CSS}	CS to SCLK high Setup	20		ns
t_{MOSIS}	MOSI to SCLK low Setup	20		ns
t_{MISO}	SCLK to MISO Valid	73		ns
t_{MIOZ}	CS to MISO High Impedance	15	35	ns

Table 15: SPI Timing

Host Parallel Timing

Host Parallel Read Cycle

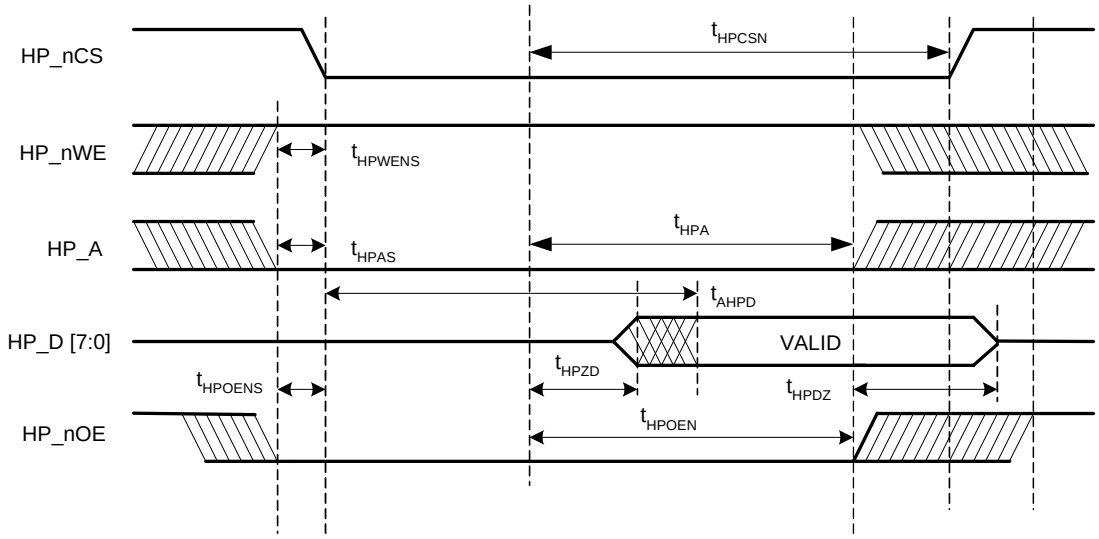


Figure 9: Host Parallel Read Cycle

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTE
t_{HPCSN}	HP_nCS Period	70		ns	
t_{HPWENS}	HP_nWE Setup	40		ns	Note 3
t_{HPAS}	HP_A Setup	40		ns	
t_{AHPD}	HP_D [7:0] Access	60	105	ns	
t_{HPZD}	HP_D [7:0] Active	0	9	ns	
t_{HPDZ}	HP_D [7:0] High Impedance	0	6	ns	
t_{HPOENS}	HP_nOE Setup	40		ns	Note 3
t_{HPOEN}	HP_nOE Period	70		ns	

Table 16: Host Parallel Read Cycle Timing

Note:
3. HP_nOE, HP_nWE must be stable before the high to low transition of HP_nCS.

Host Parallel Write Cycle

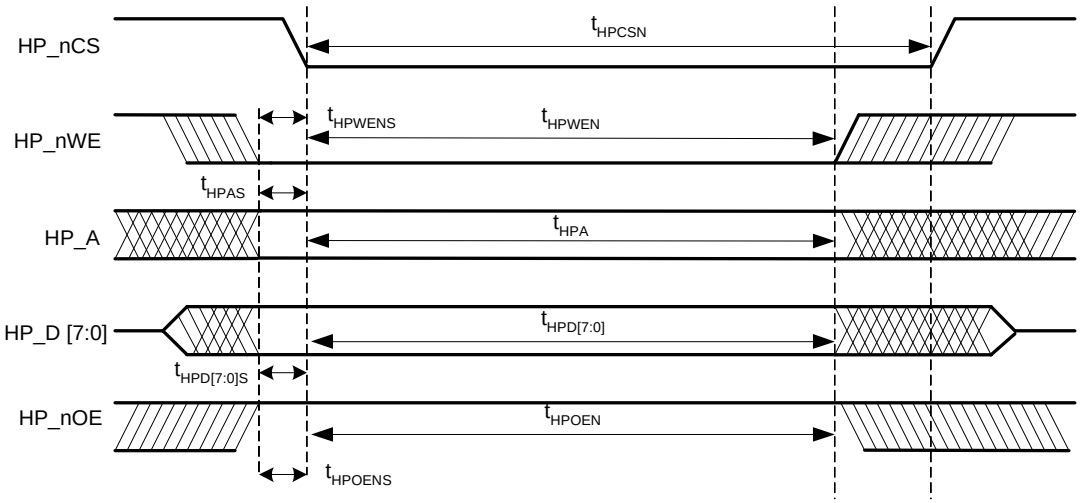


Figure 10: Host Parallel Write Cycle

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTE
t_{HPCSN}	HP_nCS Period	70		ns	
t_{HPWENS}	HP_nWE Setup	40		ns	
t_{HPWEN}	HP_nWE Period	70		ns	
t_{HPAS}	HP_A Setup	-10		ns	
t_{HPA}	HP_A Period	70		ns	
$t_{HPD[7:0]}$	HP_D [7:0] Setup	-10		ns	
t_{HPOENS}	HP_nOE Setup	40		ns	
t_{HPOEN}	HP_nOE Period	70		ns	Note 4

Table 17: Host Parallel Write Cycle Timing

Note:

4. HP_nOE must be asserted high while HP_nCS low during a Host Parallel Write Cycle.

Discrete I/O Electrical Characteristics

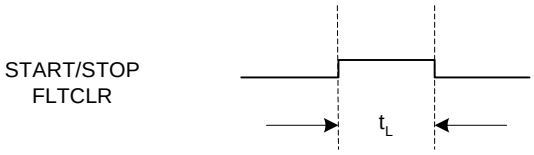


Figure 11: Discrete I/O Timing

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_L	Pulse Width STARTSTOP	100		ns
	Pulse Width FLTCLR	1		us

Table 15: Discrete I/O Timing

Motion Peripheral Electrical Characteristics

PWM Electrical Characteristics

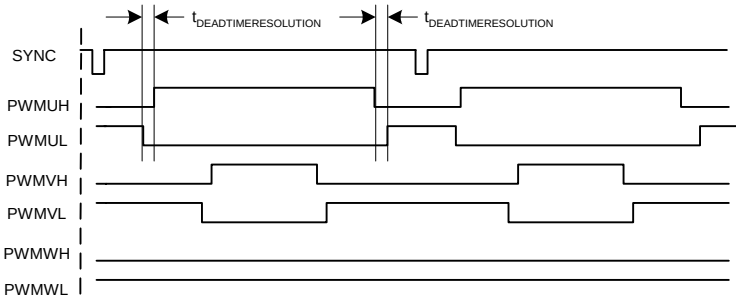


Figure 12: PWM Timing

SYMBOL	DESCRIPTION		UNITS
$t_{DEADTIMERESOLUTION}$	Deadtime Insertion Logic Resolution	30	ns

Table 16: PWM Timing

IR2175 Interface

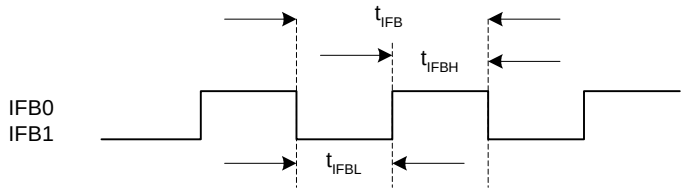


Figure 13: IR2175 Interface

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
f_{IFB}	Current Feedback Input Frequency	95	165	kHz
t_{IFB}	Current Feedback Period	10.52	6.06	us
t_{IBH}	Current Feedback High Pulse Width	500 ns	10 us	
t_{IFBH}	Current Feedback Low Pulse Width	500 ns	10 us	

Table 17: IR2175 Interface

Analog Interface Electrical Characteristics

ADC Timing

System Level Timing

The IRMCK203 contains logic to drive an ADC Converter, Analog MUX and associated Sample and Hold circuits. Figure 14 shows the system level timing of these elements. The IRMCK203 is specifically designed to interface to the Burr-Brown ADS7818 ADC. As such, all interface signals between the ADC and IRMCK203 are guaranteed to meet worst case timing specifications over the IRMCK203 and ADS7818 specified operation environment. For interfacing to other ADCs, please contact International Rectifier for detailed specifications. Also refer to the Application Developers Guide for a detailed description of ADC, MUX and Sample and Hold signal system level protocol.

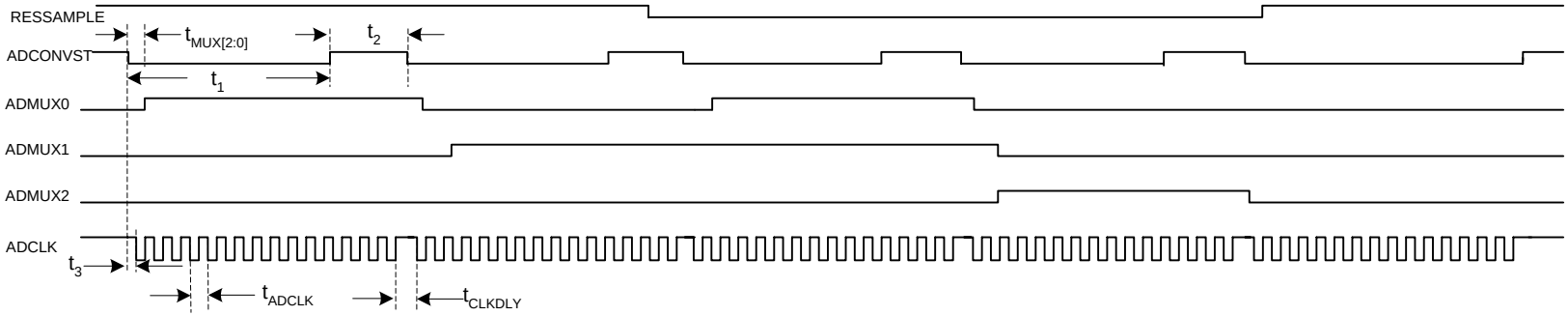


Figure 14: Top Level ADC Timing

SYMBOL	DESCRIPTION	TYP	UNITS
$t_{MUX[2:0]}$	ADCONVST to MUX[2:0]	22	ns
t_1	ADCONVST Low Period	1.44	us
t_2	ADCONVST High Period	630	ns
t_3	ADCONVST to ADCLK Falling	60	ns
t_{ADCLK}	ADCLK Period	127.5	ns
t_{CLKDLY}	ADCLK STALL Period	210	ns

Table 18: Top Level ADC Timing

PLL Interface Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Consumption	IDDS	Static	-	-	170	uA
Current Consumption	IDD	Dynamic	-	5	-	MA
Peak jitter	Tpj	-	-	-	1000	ps
Cycle jitter	Tcj	-	-500	-	+500	ps
Lock-up Time	Tlock	-	-	-	1	ms
PLL Reset Period	Trst	Recommended operating condition	10	-	-	Ns

Table 20: PLL Electrical Characteristics

Appendix A Host Register Map

Register Access

A host computer controls the IRMCK203 using its slave-mode Full-Duplex SPI port, a standard RS-232 port or a 8-bit parallel port for connection to a microprocessor. All interfaces are always active and can be used interchangeably, although not simultaneously. Control/status registers are mapped into a 128-byte address space.

Host Parallel Access

The IRMCK203 contains an address register that is updated with the Host Register address when HP_A = 1. After each subsequent data byte is either read or written, the internal address register is incremented. The diagram below shows that Data Bytes 0 to N would access register locations initially specified by the Address Byte. The Address Byte with the HP_A signal can be asserted at any time.

Address Byte HP_A = 1	Data Byte 0 HP_A = 0	..... HP_A = 0	Data Byte N HP_A = 0

Host Parallel Data Transfer Format

SPI Register Access

When configured as an SPI device read only and read/write operations are performed using the following transfer format:

Command Byte	Data Byte 0	.....	Data Byte N

Data Transfer Format

Bit Position							
7	6	5	4	3	2	1	0
Read Only	Register Map Starting Address						

Command Byte Format

Data transfers begin at the address specified in the command byte and proceed sequentially until the SPI transfer completes. As in the Host Parallel Access, the internal address register is incremented after each SPI byte is transferred. Note that accesses are read/write unless the “read only” bit is set.

RS-232 Register Access

The IRMCK203 includes an RS-232 interface channel that provides a direct connection to the host PC. The software interface combines a basic "register map" control method with a simple communication protocol to accommodate potential communication errors.

RS-232 Register Write Access

A Register write operation consists of a command/address byte, byte count, register data and checksum. When the IRMCK203 receives the register data, it validates the checksum, writes the register data, and transmits and acknowledgement to the host.

Command / Address Byte	Byte Count	1-6 bytes of register data	Checksum

Register Write Operation

Command Acknowledgement Byte	Checksum

Register Write Acknowledgement

Bit Position							
7	6	5	4	3	2	1	0
1=Read/ 0=Write	Register Map Starting Address						

Command/Address Byte Format

Bit Position							
7	6	5	4	3	2	1	0
1=Error/ 0=OK	Register Map Starting Address						

Command Acknowledgement Byte Format

The following example shows a command sequence sent from the host to the IRMCK203 requesting a two-byte register write operation:

0x2F	Write operation beginning at offset 0x2F
0x02	Byte count of register data is 2
0x00	Data byte 1
0x04	Data byte 2
0x35	Checksum (sum of preceding bytes, overflow discarded)

A good reply from the IRMCK203 would appear as follows:

0x2F	Write completed OK at offset 0x2F
0x2F	Checksum

An error reply to the command would have the following format:

0xAF	Write at offset 0x2F completed in error
0xAF	Checksum

RS-232 Register Read Access
A register read operation consists of a command/address byte, byte count and checksum. When the IRMCK203 receives the command, it validates the checksum and transmits the register data to the host.

Command / Address Byte	Byte Count	Checksum

Register Read Operation

Command Acknowledgement Byte	Register Data (Byte Count bytes)	Checksum

Register Read Acknowledgement (transfer OK)

Command Acknowledgement Byte	Checksum

Register Read Acknowledgement (error)

The following example shows a command sequence sent from the host to the IRMCK203 requesting four bytes of read register data:

0xA0	Read operation beginning at offset 0x20 (high-order bit selects read operation)
0x04	Requested data byte count is 4
0xA4	Checksum

A good reply from the IRMCK203 might appear as follows:

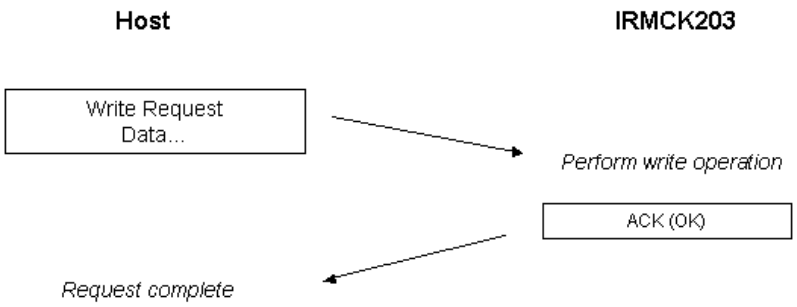
0x20	Read completed OK at offset 0x20
0x11	Data byte 1
0x22	Data byte 2
0x33	Data byte 3
0x44	Data byte 4
0xCA	Checksum

An error reply to the command would have the following format:

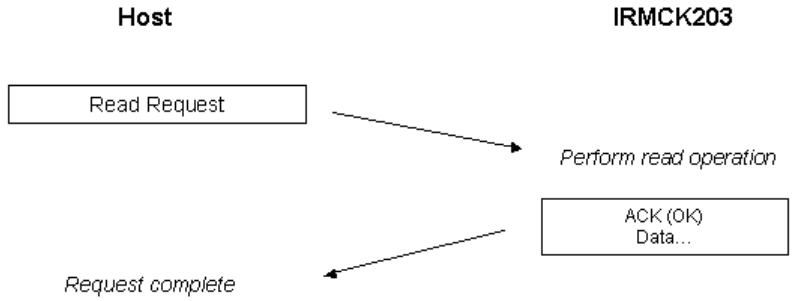
0xA0	Read at offset 0x20 completed in error
0xA0	Checksum

RS-232 Timeout
The IRMCK203 receiver includes a timer that automatically terminates transfers from the host to the IRMCK203 after a period of 32 msec.

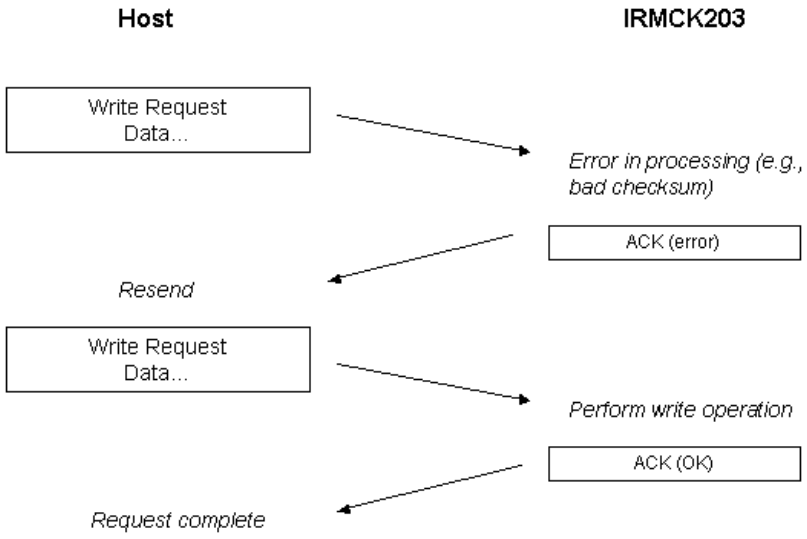
RS-232 Transfer Examples
The following example shows a normal exchange executing a register write access.



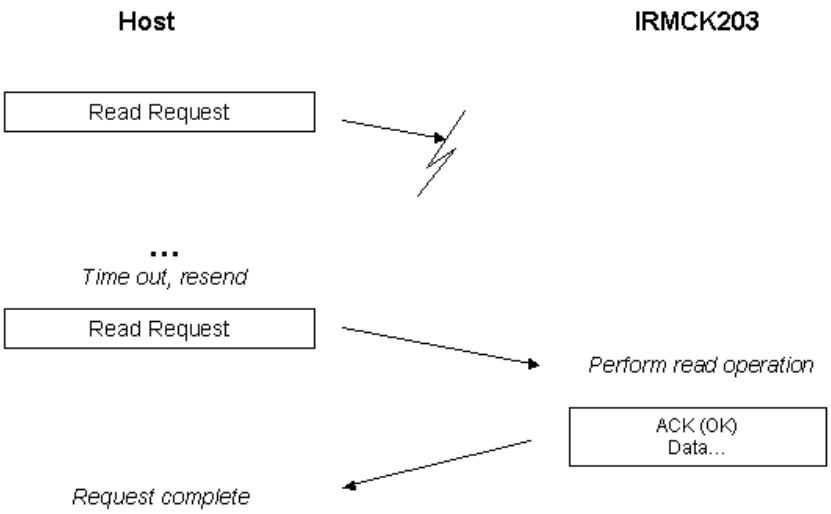
The example below shows a normal register read access exchange.



The following example shows a register write request that is repeated by the host due to a negative acknowledgement from the IRMCK203.



In the final example, the host repeats a register read access request when it receives no response to its first attempt.


Host
IRMCK203
Read Request
...
Time out, resend
Read Request
Perform read operation
ACK (OK)
Data...
Request complete

Write Register Definitions

PwmConfig Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0xC	Gatekill Sns (W)	SPARE	Gate SnsL (W)	Gate SnsU (W)	SyncSns	BrakeSns	SD (W)	SPARE
0xD	PwmPeriod (LSBs) (W)							
0xE	TwoPhs Pwm (W)	TwoPhs Type (W)	PwmConfig (W)		PwmPeriod (MSBs) (W)			
0xF	PwmDeadTm (W)							
0x44	ModScl (LSBs) (W)							
0x45	ModScl (MSBs) (W)							
0x51	PwmGuardBand (W)							

PwmConfig Write Register Map

Field Name	Access (R/W)	Field Description
SD	W	Shutdown control output to IR2137.
BrakeSns	W	Logic Sense for BRAKE signal output to gate driver IC. 0 = Active low, 1 = active high.
SyncSns	W	Logic Sense for PWM SYNC signal output to microprocessor. 0 = Active low, 1 = active high.
GateSnsU	W	Upper IGBT gate sense. 1 = active high gate control, 0 = active low gate control.
GateSnsL	W	Lower IGBT gate sense. 1 = active high gate control, 0 = active low gate control.
GatekillSns	W	GATEKILL signal sense. 1 = active high GATEKILL, 0 = active low GATEKILL.
PwmPeriod	W	PWM Carrier period. Actual PWM carrier period is 2 * (PwmPeriod + 1) * (System Clock Period).
PwmConfig	W	PWM Configuration. 0 = Asymmetrical center aligned PWM, 1 = Symmetrical Center aligned PWM.
TwoPhsType	W	Used only for two-phase PWM modulation mode: 0 = Type 1 2-phase PWM 1 = Type 2 2-phase PWM
TwoPhsPwm	W	Selects PWM modulation mode: 0 = Enable 3-phase space vector PWM modulation 1 = Enable 2-phase space vector PWM modulation

Field Name	Access (R/W)	Field Description
PwmDeadTm	W	Gate drive dead time in units of system clock cycles (e.g., 30 ns with 33 MHz clock).
ModScl	W	Space vector modulator scale factor. This register, which depends on the PWM carrier frequency, should be set as follows: ModScl = PwmPeriod * sqrt(3) * 4096 / 2355 where PwmPeriod is the value in the PwmConfig write register group's PwmPeriod register.
PwmGuardBand	W	This parameter provides a guard band (scaling: 1 = 30nsec) such that PWM switching will not migrate into the current feedback sampling instant (Sync Pulse region). This guard band is provided to improve feedback noise. The parameter only applies to the 3-phase Space Vector modulation scheme. Please do not modify this parameter without consulting a motor drive FAE.

PwmConfig Write Register Field Definitions

CurrentFeedbackConfig Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x15	IfbkScl (LSB) (W)							
0x16	IfbkScl (MSB) (W)							
0x7D	OffsetCalDelay (W)							

CurrentFeedbackConfig Write Register Map

Field Name	Access (R/W)	Field Description
IfbkScl	W	Rotating frame Iq component and Id component current feedback scale factor. Constant used to scale current measurements before they are used in the field orientation calculation. This is a 15-bit fixed-point signed number with 10 fractional bits that ranges from –16 to + 16 + 1023 / 1024.
OffsetCal Delay	W	This parameter specifies the delay time (1 = 1 sec) to restart current offset measurement after a stop command is issued. Only applies if Leg Shunt current feedback is selected.12-bit signed value for V phase current feedback offset. When the IfbOffsEnb bit in the SystemControl write register group is "0" this value is automatically added to each current measurement in hardware.

CurrentFeedbackConfig Write Register Field Definitions

SystemControl Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x17	SPARE					HostEstop	StartCmd	Rotation

SystemControl Write Register Map

Field Name	Access (R/W)	Field Description
Rotation	W	Direction of motor rotation: 0 = Reverse motor rotation; 1 = Forward motor rotation.
StartCmd	W	Start/Stop bit. Setting this bit to 1 issues a start command. Setting this bit to 0 stops the motor.
HostEstop	W	Emergency coast stop will take place when this bit is set to one.

SystemControl Write Register Field Definitions

TorqueLoopConfig Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x1A	KpIreg – Current Loop Proportional Gain (LSBs) (W)							
0x1B	KpIreg – Current Loop Proportional Gain (MSBs) (W)							
0x1C	KxIreg – Current Loop Integral Gain (LSBs) (W)							
0x1D	KxIreg – Current Loop Integral Gain (MSBs) (W)							
0x22	VqLim – Quadrature Current Output Limit (LSBs) (W)							
0x23	VqLim – Quadrature Current Output Limit (MSBs) (W)							
0x26	VdLim – Direct Current Output Limit (LSBs) (W)							
0x27	VdLim – Direct Current Output Limit (MSBs) (W)							

TorqueLoopConfig Write Register Map

Field Name	Access (R/W)	Field Description
KpIreg	W	15-bit signed current loop PI controller proportional gain. Scaled with 14 fractional bits for an effective range of 0 – 1.
KxIreg	W	15-bit signed current loop PI controller integral gain. Scaled with 19 fractional bits for an effective range of 0 - .03125.
VqLim	W	16-bit Quadrature current PI controller voltage output limit.
VdLim	W	16-bit Direct current PI controller voltage output limit.

TorqueLoopConfig Write Register Field Definitions

VelocityControl Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x32	KpSreg – Velocity loop proportional gain (LSBs) (W)							
0x33	KpSreg – Velocity loop proportional gain (MSBs) (W)							
0x34	KxSreg – Velocity loop integral gain (LSBs) (W)							
0x35	KxSreg – Velocity loop integral gain (MSBs) (W)							
0x36	MotorLim – Velocity loop Output Positive Limit (LSBs) (W)							
0x37	MotorLim – Velocity loop Output Positive Limit (MSBs) (W)							
0x38	RegenLim – – Velocity loop Output Negative Limit (LSBs)							
0x39	RegenLim – – Velocity loop Output Negative Limit (MSBs)							
0x3A	SpdScl – Speed Scale Factor (LSBs)							
0x3B	SpdScl – Speed Scale Factor (MSBs)							
0x3C	TargetSpd – Setpoint/target speed (LSBs)							
0x3D	TargetSpd – Setpoint/target speed (MSBs)							
0x3E	AccelRate							
0x3F	DecelRate							
0x7A	MinSpd							

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x18	StartLim (LSBs)							
0x19	StartLim (MSBs)							

VelocityControl Write Register Map

Field Name	Access (R/W)	Field Description
KpSreg	W	15-bit velocity loop proportional gain, in fixed point with 5 fractional bits. Range = 0 - 512.
KxSreg	W	15-bit velocity loop integral gain, in fixed point with 13 fractional bits. Range = 0 - 2.
MotorLim	W	Motoring torque current limit (4095 = rated motor current).16-bit speed PI controller output positive limit.
RegenLim	W	Regeneration torque current limit (4095 = rated motor current)16-bit speed PI controller output negative limit (2's complement)..
SpdScl	W	Motor Speed Scale factor.
TargetSpd	W	Velocity loop speed setpoint in SPEED units, which are determined by the user via the SpdScl register setting.
AccelRate	W	Acceleration rate limit.
DecelRate	W	Deceleration rate limit.
MinSpd	W	Minimum speed protection. This parameter sets the minimum reference speed.
StartLim	W	Drive start-up current limit. (4095 = rated motor current).

VelocityControl Write Register Field Definitions

FaultControl Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x42	SPARE						FltClr	DcBusM Enb

FaultControl Write Register Map

Field Name	Access (R/W)	Field Description
DcBusMEnb	W	DC Bus monitor enable. 1 = Monitor DC bus voltage and generate appropriate brake signal control and disable PWM output when voltage fault conditions occur. GatekillFlt and OvrSpdFlt faults cannot be disabled. DC bus voltage thresholds are as follows: Overvoltage – 410V Brake On – 380V Brake Off – 360V Nominal – 310V Undervoltage off – 140V Undervoltage – 120V
FltClr	W	This bit clears all active fault conditions. The user should monitor the FaultStatus read register group to determine fault status and set this bit to "1" to clear any faults that have occurred. A fault condition automatically clears the PwmEnbW and FocEnbW bits in the SystemControl write register group. Note that this bit also directly controls the output 2137 FLTCLR pin. After clearing a fault, the user must explicitly set this bit to "0" to re-enable fault processing.

FaultControl Write Register Field Definitions

SystemConfig Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x50	ExtCtrl	AdcIfbEnb	Ramp Stop	SPARE				

SystemConfig Write Register Map

Field Name	Access (R/W)	Field Description
RampStop	W	Selects the stopping mode: 0 - Configure for Coast stopping 1 - Configure for Ramp stopping
AdcIfbEnb	W	Selects the current feedback mode: 0 - Selects IR2175 current feedback 1 - Selects Leg-Shunt current feedback
ExtCtrl	W	Setting this bit to "1" enables direct control of basic motor operation via the external User Interface pins. When this bit is "1", the FocEnbW and PwmEnbW bits in the SystemControl write register group are ignored.

SystemConfig Write Register Field Definitions

EepromControl Registers (Write Registers)

At power up, the write registers can be optionally initialized with values stored in EEPROM. The EepromControl write register group and EepromStatus read register group are used to read and write these EEPROM values. Since the EeAddrW write register (which selects the EEPROM offset to read or write) does not require initialization at power up, the location corresponding to that register in EEPROM (at offset 0x5D) is used to store a register map version code. At power on, the IRMCK203 initializes the write registers from EEPROM only if the version code stored at this offset in EEPROM matches its internal register map version code (which can be read from the RegMapVer field of the EepromStatus read register group).

To enable write register initialization at power up, write the appropriate register map version code to EEPROM at offset 0x5D. To disable write register initialization at power up, write a zero (or any non-matching version code) to offset 0x5D of the EEPROM.

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x5C	SPARE					EeWrite	EeRead	EeRst
0x5D	EeAddrW / RegMapVersCode (W)							
0x5E	EeDataW (W)							

EepromControl Write Register Map

Field Name	Access (R/W)	Field Description
EeRst	W	Self-clearing EEPROM reset. Writing a "1" to this bit resets the I2C EEPROM interface.
EeRead	W	Self-clearing I2c EEPROM Read. Writing a "1" to this bit initiates an EEPROM read from the byte located at EEPROM address EeAddrW. After setting this bit the user should poll the EeBusy bit in the EepromStatus read register group to determine when the read completes and then read the data from EeDataR in the EepromStatus read register group.
EeWrite	W	Self-clearing EEPROM Write. Writing a "1" to this bit initiates an EEPROM write from the data byte in EeDataW to the EEPROM address EeAddrW .
EeAddrW	W	EEPROM Address Register. Contains the address for the next EEPROM read or write operation.
EeDataW	W	EEPROM Data Register. Contains the data for the next EEPROM write operation.

EepromControl Write Register Field Definitions

ClosedLoopAngleEstimator Registers (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x60	IScl (LSBs) (W)							
0x61	IScl (MSBs (W)							
0x62	FlxBInit (LSBs) (W)							
0x63	FlxBInit (MSBs) (W)							
0x6A	PllKp (LSBs) (W)							
0x6B	SPARE		PllKp (MSBs (W)					
0x6C	PllKi (LSBs) (W)							
0x6D	SPARE		PllKi (MSBs (W)					
0x6E	VoltScl (LSBs) (W)							
0x6F	VoltScl (MSBs (W)							
0x70	Rs (LSBs) (W)							
0x71	Rs (MSBs (W)							
0x72	Ld (LSBs) (W)							
0x73	Ld (MSBs (W)							
0x74	AtanTau (LSBs) (W)							
0x75	AtanTau (MSBs (W)							
0x76	FlxTau (LSBs) (W)							
0x77	SPARE				FlxTau (MSBs) (W)			

ClosedLoopAngleEstimator Write Register Map

Field Name	Access (R/W)	Field Description
IScl	W	Current scaler for motor flux calculation.
FlxBInit	W	Initialization value of Beta flux at start.
PllKp	W	Flux phase lock loop proportional gain.
PllKi	W	Flux phase lock loop integral gain.
VoltScl	W	Voltage scaler for motor flux calculation.
Rs	W	Motor per phase resistance including cable (@25C).
Ld	W	Motor per phase inductance.
AtanTau	W	Rotor angle estimator phase compensation gain.
FlxTau	W	Rotor angle estimator flux model time constant.

ClosedLoopAngleEstimator Write Register Field Definitions

OpenLoopAngleEstimator Registers (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x66	KTorque (LSBs) (W)							
0x67	KTorque (MSBs (W)							
0x5F	VFGain (W)							

OpenLoopAngleEstimator Write Register Map

Field Name	Access (R/W)	Field Description
KTorque	W	Motor mechanical model torque constant.
VFGain	W	Open-Loop Volts/Hz Flux gain. (for diagnostic use only).

OpenLoopAngleEstimator Write Register Field Definitions

StartupAngleEstimator Registers (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x64	ParkI (W)							
0x65	SPARE	Zero SpdFlt Disable	Use2xFrq Scale	PhsLosFlt Disable	DiagnosticCtrl (W)			
0x68	WeThr (LSBs) (W)							

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x69	WeThr (MSBs (W)							
0x78	ParkTm (W)							

StartupAngleEstimator Write Register Map

Field Name	Access (R/W)	Field Description
ParkI	W	DC current injection level during motor parking (start-up mode).
DiagnosticCtrl	W	1 (0001) – Enable Parking diagnostic 2 (0010) – Enable start-up diagnostic 5 (0101) – Enable current regulator diagnostic 9 (1001) – Enable volts Hertz diagnostic
PhsLosFlt Disable	W	Enable/disable phase loss fault: 0 = Enable Phase Loss Fault; 1 = Disable Phase Loss Fault
Use2xFrqScale	W	Selects speed scaling: 0 - Norminal speed scale 1 - Reduce speed feedback scaling by half Please do not modify this parameter without consulting motor control FAEs
ZeroSpdFlt Disable	W	Zero speed fault enable/disable: 0 - Enbale Zero Speed Fault 1 - Disable Zero Speed Fault
WeThr	W	Frequency threshold level (switch over from open-loop to closed-loop mode).
ParkTm	W	Time duration of parking mode. 255 = 4 sec

StartupAngleEstimator Write Register Field Definitions

StartupRetrial Registers (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x1E	RetryTm (LSBs)							
0x1F	RetryTm (MSBs)							
0x79	ParkTmRet							
0x7B	FlxThrL							
0x7C	FlxThrH							

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x7E	NumRetries							
0x7F	ParkIRet							

StartupRetrial Write Register Map

Field Name	Access (R/W)	Field Description
RetryTm	W	This parameter provides the adjustment to the sampling instant for determination of start failure. The sampling instant starts when Closed_Loop = 1. Scaling 1 count = 1.966 msec. Please do not modify this parameter without consulting a motor drive FAE.
ParkTmRet	W	During motor start-up, dc current is injected to the motor for maximization of startup torque per ampere rating. ParkTm controls the duration of dc current injection. However, users are able to use a longer duration after two or more restarts by setting this parameter (ParkTmRet scaling 255 = 4 secs.). This is done to increase the chance of a successful start-up.Start-up failure may be caused by increased shaft friction. After first start-up retry, the parking time can be increased to improve parking performance.
FlxThrL	W	The low flux threshold level for determining a successful startup (scaling: 129 = 100% flux). Please do not modify this parameter without consulting a motor drive FAE.The low flux threshold level for determining a successful startup.
FlxThrH	W	The upper flux threshold level for determining a successful startup (scaling: 64 = 100% flux). Please do not modify this parameter without consulting a motor drive FAE.The high flux threshold level for determining start-up failure.
NumRetries	W	If start-up fails, the user can program start-up retrial. This parameter determines the number of start-up retries. A value of zero will disable startup retrial. The maximum number of retries is 15.
ParkIRet	W	During motor start-up, dc current is injected to the motor for maximization of startup torque per ampere rating. Users are able to use a higher level of dc current injection (ParkIRet scaling 255 = Motor Rated Amp * 0.866) after two or more restarts. This is done to increase the chance of a successful start-up.Start-up failure may be caused by increased shaft friction. After first start-up retry, the parking current can be increased to improve parking performance.

StartupRetrial Write Register Field Definitions

PhaseLossDetect Registers (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x79	ParkTmRet							
0x28	AdjPark1							
0x29	AdjPark2							
0x2A	RetryTm							

PhaseLossDetect Write Register Map

Field Name	Access (R/W)	Field Description
AdjPark1	W	Anticipated W-phase motor current gain scaler used during initial stage of Phase Loss detection.
AdjPark2	W	Anticipated W-phase motor current gain scaler used during final stage of Phase Loss detection.
PhsLosThr	W	Phase Loss detection current error threshold.

PhaseLossDetect Write Register Field Definitions

D/AConverter Registers (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x4F	DacSel							

D/AConverter Write Register Map

Field Name	Access (R/W)	Field Description
DacSel	W	Selects D/A converter diagnostic outputs 0 - 3. A value of 0 selects: Data 0 = Alpha fluxFlux Data 1 = Electrical Rotor angle Data 2 = Alpha voltageTorque current Data 3 = Closed loop/open loop status (0 = open, 1 = closed) A value of 1 selects: Data 0 = Alpha currentDC bus voltage Data 1 = Torque current feedbackAlpha voltage Data 2 = IQ refTorque current reference Data 3 = Motor speed A value of 2 selects: Data 0 = Q-axis command voltage Data 1 = D-axis command voltage Data 2 = Alpha current Data 3 = Beta current A value of 3 selects: Data 0 = Flux magnitude Data 1 = Current error at parking Data 2 = Parking diagnostic flag Data 3 = W-phase current

D/AConverter Write Register Field Definitions

Factory Test Register (Write Register)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x58	Test							

Factory Write Register Map

Field Name	Access (R/W)	Field Description
Test	W	Reserved for factory use. Data written to this register could be read from a read register at location 0x58.

Factory Write Register Field Definitions

Read Register Definitions

SystemStatus Register Group (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x7	StartStop	FwdRev	ESTOP	PwrID		ExtCtrlR	Foc EnbR	Pwm EnbR

SystemStatus Read Register Map

Field Name	Access (R/W)	Field Description
PwmEnbR	R	PWM Enable bit status.
FocEnbR	R	FOC Enable bit status.
ExtCtrlR	R	Reflects the status of the ExtCtrl bit in the System Configuration write register (address 0x50).
PwrID	R	Power ID. 0 = 3 kW, 1 = 2 kW, 2 = 500 W.
ESTOP	R	User Interface emergency stop signal (1 – emergency stop)
FwdRev	R	User Interface “DIR" digital input status. 1 - Forward rotation request 0 - Reverse rotation request
StartStop	R	User Interface “START/STOP" digital input status. 1 - Start 0 - Stop

SystemStatus Read Register Field Definitions

DcBusVoltage Register Group (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0xA	DcBusVolts (LSBs)							
0xB	SPARE			Brake	DcBusVolts (MSBs)			

DcBusVoltage Read Register Map

Field Name	Access (R/W)	Field Description
DcBusVolts	R	DC Bus Voltage. Data range is 0 - 4095, which corresponds to a DC bus voltage between 0 and 500 volts.
Brake	R	Brake signal status. 1 = Brake signal active.

DcBusVoltage Read Register Field Definitions

FocDiagnosticData Register Group (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0xC	RotatorAngle (LSB)							
0xD	SPARE	Parking Done	Start_ Fail	Closed_ Loop	RotatorAngle (MSB)			
0xE	Id – Synchronous Frame Direct Current (LSBs)							
0xF	Id – Synchronous Frame Direct Current (MSBs)							
0x10	Iq – Synchronous Frame Quadrature Current (LSBs)							
0x11	Iq – Synchronous Frame Quadrature Current (MSBs)							
0x12	IqRef_C – Synchronous Frame Quadrature Current command (LSB)							
0x13	IqRef_C – Synchronous Frame Quadrature Current command (MSB)							
0x14	Flx_Alpha – Estimated Motor Flux (LSB)							
0x15	Flx_Alpha – Estimated Motor Flux (MSB)							
0x16	I_Alpha – Alpha Frame Current (LSB)							
0x17	I_Alpha – Alpha Frame Current (MSB)							
0x18	V_Alpha – Alpha Frame Voltage (LSB)							
0x19	V_Alpha – Alpha Frame Voltage (MSB)							

FocDiagnosticData Read Register Map

Field Name	Access (R/W)	Field Description
RotatorAnlge	R	Estimated rotor angle (electrical), which is used for synchronous frame to stationary frame transformation. The scaling is 4096 = 2PI. The range is 0 – 4095.
Closed_Loop	R	This is a drive control status flag which indicates that the drive has switched from open-loop to closed-loop operation. The switch over is done during drive start-up (initial speed ramping)
Start_Fail	R	This is a drive control status flag indicating that the drive has failed to start due to various reasons (for instance: shaft jam). The start-stop sequencer uses this bit and parameter NumRetry to determine whether a start-up retry should be activated.
Parking Done	R	This is a status flag indicating that the drive has finished obtaining the initial rotor angle (parking) for motor startup. During drive start-up, the first start-up stage is parking stage.
Id, Iq	R	Synchronous or rotating frame direct and quadrature current values in 2's complement representation. The full scale current values range from –16384 to 16383. (Scaling: 4095 = rated motor current)
IqRef_C	R	Synchronous or rotating frame quadrature current command values in 2's complement representation. The full scale current values range from –16384 to 16383.
Flx_Alpha	R	Estimated motor flux value. Scaling is 5000 = rated motor flux.
I_Alpha	R	Stationary frame current. Scaling is platform dependent (current shunt resistor). Drive commissioning tool (Spreadsheet) provides the scaling of I_Alpha (AiBi scale).
V_Alpha	R	Stationary frame Alpha voltage. This voltage is constructed by dc bus voltage and modulation index in the Stationary frame. The scaling is platform dependent.

FocDiagnosticData Read Register Field Definitions

FaultStatus Register Group (Read Registers)

The Fault Status register records fault conditions that occur during drive operation. When any of these fault conditions occur, the PWM output is automatically disabled. The user should monitor this register continuously for fault conditions. A fault condition can be cleared by writing a "1" to the FaultClr bit in the FaultControl write register group. (This does not automatically re-enable PWM output.)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x1E	PhsLoss Flt	RetryFlt	ZeroSpd Flt	ExecTm Flt	OvrSpdFlt	OvFlt	LvFlt	GatekillFlt

FaultStatus Read Register Map

Field Name	Access (R/W)	Field Description
GatekillFlt	R	Filtered and latched version of IR2137 FAULT output.
LvFlt	R	DC bus low voltage fault. This fault occurs if the DC bus drops below 120V.

Field Name	Access (R/W)	Field Description
OvFlt	R	DC bus overvoltage fault. This fault occurs if the DC bus voltage exceeds 410V.
OvrSpdFlt	R	Over speed fault. This fault occurs whenever the motor reaches the positive or negative limits. The user should use the scale factor in the SpdScl field of the VelocityControl write register group to scale the motor speed so that it falls between -16384 and +16383 with these limits as the over speed condition.
ExecTmFlt	R	Execution time fault.
ZeroSpdFlt	R	Zero Speed fault. When speed is less than MinSpd/2 (half minimum speed) for a continuous period of 4 seconds, the zero speed fault will be set.
RetryFlt	R	Start-up retry fault. After a certain number (determined by parameter NumRetries) of start-up failures, this fault will be set.
PhsLossFlt	R	Phase loss fault. Drive to motor phase connection may be loose.

FaultStatus Read Register Field Definitions

VelocityStatus Register Group (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x26	Spd (LSBs)							
0x27	Spd (MSBs)							

VelocityStatus Read Register Map

Field Name	Access (R/W)	Field Description
Spd	R	Current motor speed in SPEED units. (See the description of SpdScl in the VelocityControl write register group.)

VelocityStatus Read Register Field Definitions

CurrentFeedbackOffset Register Group (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x30	IfbVOffs (LSBs) (R)							
0x31	IfbWOffs (LSBs) (R)				IfbVOffs (MSBs) (R)			
0x32	IfbWOffs (MSBs) (R)							

CurrentFeedbackOffset Read Register Map

Field Name	Access (R/W)	Field Description
IfbVOffs, IfbWOffs	R	Current feedback offset values from the last IFB Offset calculation. These values are automatically applied to each current feedback measurement value whenever the IfbOffsEnb bit in the SystemControl write register group is set.

CurrentFeedbackOffset Read Register Field Definitions

EepromStatus Registers (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x38	SPARE							EeBusy
0x39	EdDataR (R)							
0x3A	EeAddrR (R)							

EepromStatus Read Register Map

Field Name	Access (R/W)	Field Description
EeBusy	R	I2C EEPROM Interface busy bit. The user should wait for this bit to clear before initiating EEPROM read or write operations.

Field Name	Access (R/W)	Field Description
EeDataR	R	EEPROM Data Register. Contains the data from the last EEPROM read operation. Note that writing to the EeRst field in the EepromControl write register group invalidates this register.
EeAddrR	R	EEPROM Address read register shows the value stored in EEPROM at the offset of the EeAddrW write register (0x5D). Since this address in the EEPROM contains the BPIRMCK203 register map version, the user can read this field to determine whether or not the write registers were initialized at power on.

EepromStatus Read Register Field Definitions

FOCDiagnosticDataSupplement Register Group (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x3C	ElecAngR (LSBs) (R)							
0x3D	SPARE				ElecAngR (MSBs) (R)			
0x3E	SpdRef (LSBs) (R)							
0x3F	SpdRef (MSBs) (R)							
0x40	SpdErr (LSBs) (R)							
0x41	SpdErr (MSBs) (R)							
0x42	IqRefR (LSBs) (R)							
0x43	IqRefR (MSBs) (R)							

FOCDiagnosticDataSupplement Read Register Map

Field Name	Access (R/W)	Field Description
ElecAngR	R	Electrical angle.
SpdRef	R	Speed PI controller reference input.
SpdErr	R	Speed PI controller error.
IqRefR	R	Speed PI controller output.

FOCDiagnosticDataSupplement Read Register Field Definitions

ProductIdentification Registers (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x7C	ProductID (R)							
0x7D	RegMapVerID (R)							
0x7E	RevCodeID (LSBs) (R)							
0x7F	RevCodeID (MSBs) (R)							

ProductIdentification Read Register Map

Field Name	Access (R/W)	Field Description
ProductID	R	Product identification code.
RegMapVerID	R	Current register map version code.
RevCodeID	R	IRMCK203 Revision Code. Revision code format is “XX.XX”, where each “X” is a 4-bit hexadecimal number.

ProductIdentification Read Register Field Definitions

Factory Register (Read Register)

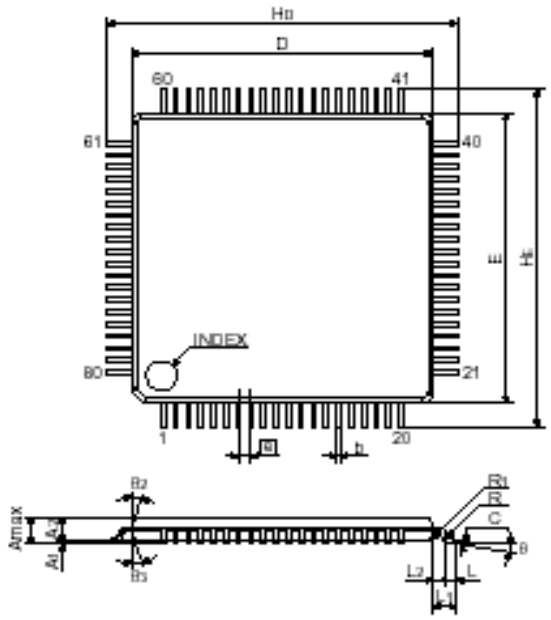
Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x58	Test (R)							

Factory Read Register Map

Field Name	Access (R/W)	Field Description
Test	R	Data value resulting from a write to write register 0x58. Used for factory use only.

Factory Read Register Field Definitions

Appendix B Package



Lead type STD (TQFP14-80pin STD)

Symbol	Dimension in Millimeters			Dimension in Inches *		
	Min.	Nom.	Max.	Min.	Nom.	Max.
E	11.9	12	12.1	(0.469)	(0.472)	(0.476)
D	11.9	12	12.1	(0.469)	(0.472)	(0.476)
A			1.2			(0.047)
A1		0.1			(0.004)	
A2	0.9	1	1.1	(0.035)	(0.039)	(0.043)
e		0.5			(0.020)	
b	0.11	0.16	0.26	(0.005)	(0.006)	(0.010)
C	0.1	0.125	0.175	(0.004)	(0.005)	(0.006)
θ	0°		8°	(0°)		(8°)
L	0.3	0.5	0.7	(0.012)	(0.020)	(0.027)
L1		1			(0.039)	
Lz		0.5			(0.020)	
HE	13.6	14	14.4	(0.535)	(0.551)	(0.566)
HD	13.6	14	14.4	(0.535)	(0.551)	(0.566)
θz						
θ1						
R						
R1						

* for reference

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