MN4017B / MN4017BS

5-Stage Johnson Counters

■ Description

The MN4017B/S are 5-stage Johnson decade counters constructed with five D-type flip-flops. One of the outputs (O_0 ~ O_9) becomes High level according to the number of counter pulses applied to CP_0 or $\overline{CP}_1$. The counter is advanced by either a positive going edge of CP_0 while $\overline{CP}_1$ is Low or a negative going edge of $\overline{CP}_1$ while CP_0 is High. A High on the reset input (MR) resets the counter to zero ($O_0 = \overline{O}_{5-9}$ = High, O_1 ~ O_9 = Low) independent of the clock inputs (CP_0, $\overline{CP}_1$).
These are equivalent to MOTOROLA MC14017B and RCA CD4017B.

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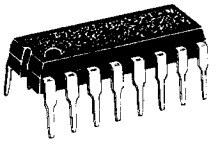


16-Pin • Plastic DIL Package

P- 4

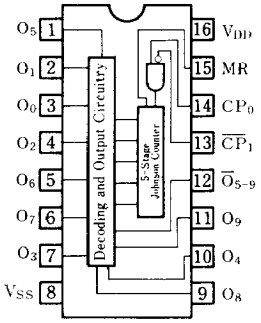
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

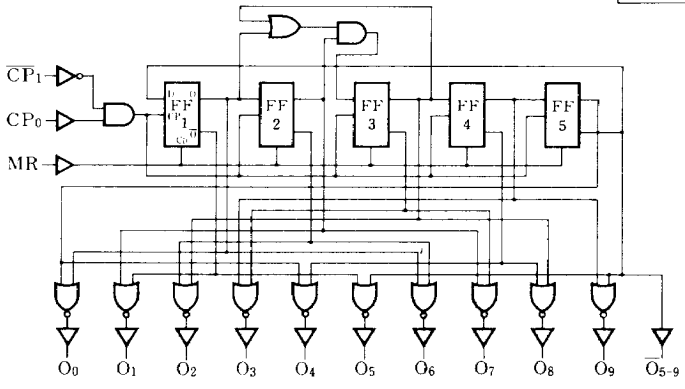
MR	CP_0	$\overline{CP}_1$	Mode
H	×	×	$O_0 = \overline{O}_{5-9}$ = H , O_1—O_9 = L
L	H	↘	Counter Advances
L	↗	L	
L	L	×	No Change
L	×	H	
L	H	↗	
L	↘	L	

Note) × : don't care

Pin Configuration



■ Logic Diagram



Pin Explanation

CP_0 : Positive clock input (↗)
$\overline{CP}_1$: Negative clock input (↘)
MR : Reset input
O_0~O_9 : Output (10 Bits)

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

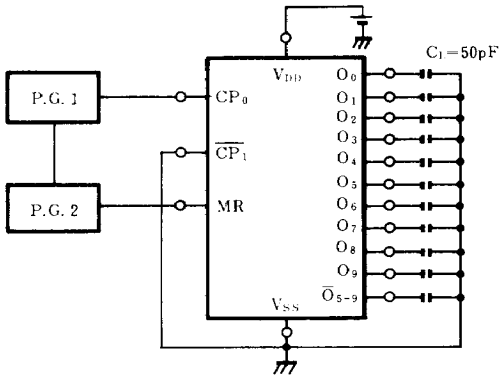
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

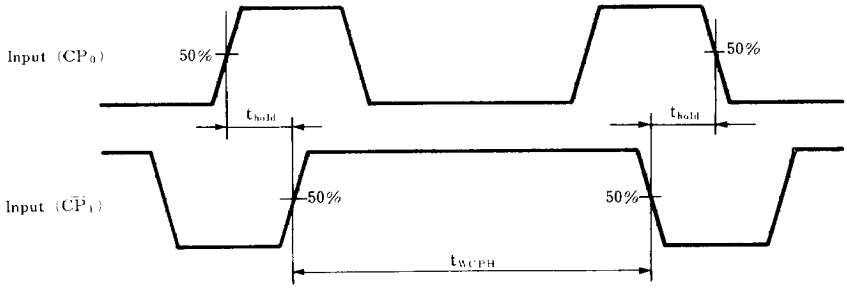
■ **Switching Characteristics** ($Ta = 25℃$, $V_{SS} = 0V$, $C_L = 50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow O_0$ to O_9 (H→L)	5	t_{PHL}	—	195	585	ns
	10		—	75	225	
	15		—	50	150	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow O_0$ to O_9 (L→H)	5	t_{PLH}	—	245	735	ns
	10		—	95	285	
	15		—	60	180	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow \overline{O}_{5\text{-}9}$ (H→L)	5	t_{PHL}	—	245	735	ns
	10		—	90	270	
	15		—	60	180	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow \overline{O}_{5\text{-}9}$ (L→H)	5	t_{PLH}	—	190	570	ns
	10		—	75	225	
	15		—	50	150	
Propagation Delay Time MR→O_1 to O_9 (H→L)	5	t_{PHL}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time MR→$\overline{O}_{5\text{-}9}$ (L→H)	5	t_{PLH}	—	110	330	ns
	10		—	45	135	
	15		—	35	105	
Propagation Delay Time MR→O_0 (L→H)	5	t_{PLH}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Hold Time $CP_0 \rightarrow \overline{CP}_1$	5	t_{hold}	—	70	210	ns
	10		—	25	75	
	15		—	15	45	
Hold Time $\overline{CP}_1 \rightarrow CP_0$	5	t_{hold}	—	85	255	ns
	10		—	30	90	
	15		—	20	60	
Minimum Clock Pulse Width	5	t_{WCP}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Minimum Reset Pulse Width	5	t_{WMRH}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Reset Recovery Time	5	t_{RMR}	—	25	75	ns
	10		—	10	40	
	15		—	10	30	
Maximum Clock Frequency	5	f_{max}	3	6	—	ns
	10		8	16	—	
	15		12	24	—	
Input Capacitance		C_I	—	—	7.5	pF

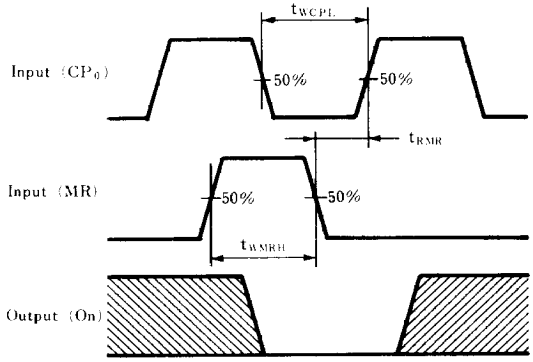
1. Switching Time Test Circuit



2. Waveforms



Waveforms showing hold times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0
Hold times are shown as positive values, but may be specified as negative values.



Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths
Conditions: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW to HIGH transition; t_{WCP} and t_{RMR} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH to LOW transition.

■ Timing Diagram