

AO4617

Complementary Enhancement Mode Field Effect Transistor

General Description

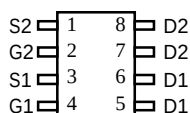
The AO4617 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications. *Standard Product AO4617 is Pb-free (meets ROHS & Sony 259 specifications). AO4617L is a Green Product ordering option. AO4617 and AO4617L are electrically identical.*

Features

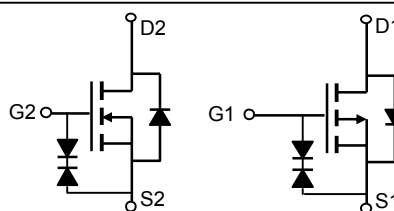
n-channel	p-channel
$V_{DS} (V) = 40V$	-40V
$I_D = 6A (V_{GS}=10V)$	-5A ($V_{GS} = -10V$)
$R_{DS(ON)}$	$R_{DS(ON)}$
$< 32m\Omega (V_{GS}=10V)$	$< 48m\Omega (V_{GS} = -10V)$
$< 45m\Omega (V_{GS}=4.5V)$	$< 75m\Omega (V_{GS} = -4.5V)$

ESD rating: 3000V (HBM)

UIS TESTED!
 $R_g, C_{iss}, C_{oss}, C_{rss}$ Tested



SOIC-8



n-channel

p-channel

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^A	I_D	6	-5	A
$T_A=25^\circ C$		5	-4	
Pulsed Drain Current ^B	I_{DM}	30	-25	A
Power Dissipation	P_D	2	2	W
	$T_A=70^\circ C$	1.28	1.28	
Avalanche Current ^B	I_{AR}	13	17	A
Repetitive avalanche energy 0.3mH ^B	E_{AR}	25	43	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ C$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^A		n-ch	74	110	$^\circ C/W$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	n-ch	35	50	$^\circ C/W$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^A		p-ch	74	110	$^\circ C/W$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	p-ch	35	50	$^\circ C/W$

N Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=32\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^{\circ}\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 1	mA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	2.2	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=6\text{A}$ $T_J=125^{\circ}\text{C}$		26 39	32 48	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=5\text{A}$		36	45	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=6\text{A}$		18		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=20\text{V}$, $f=1\text{MHz}$		506		pF
C_{oss}	Output Capacitance			106		pF
C_{rss}	Reverse Transfer Capacitance			38		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		2.6	3.9	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $I_D=6\text{A}$		8.4		nC
$Q_g(4.5\text{V})$	Total Gate Charge			4.1		nC
Q_{gs}	Gate Source Charge			1.6		nC
Q_{gd}	Gate Drain Charge			2.7		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $R_L=3.3\Omega$, $R_{GEN}=3\Omega$		4.8		ns
t_r	Turn-On Rise Time			2		ns
$t_{D(off)}$	Turn-Off DelayTime			17		ns
t_f	Turn-Off Fall Time			2.1		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=6\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		17.4		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=6\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		10.9		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $\leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL

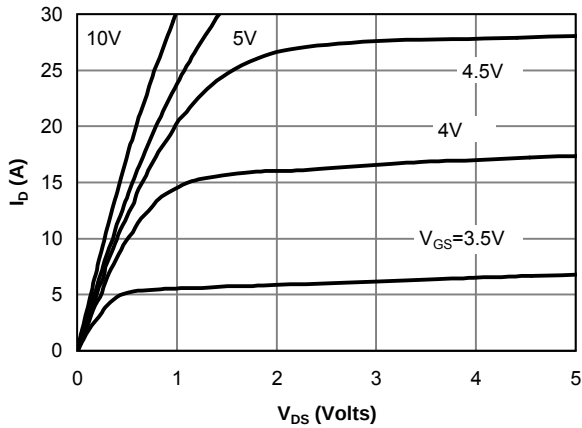


Figure 1: On-Region Characteristics

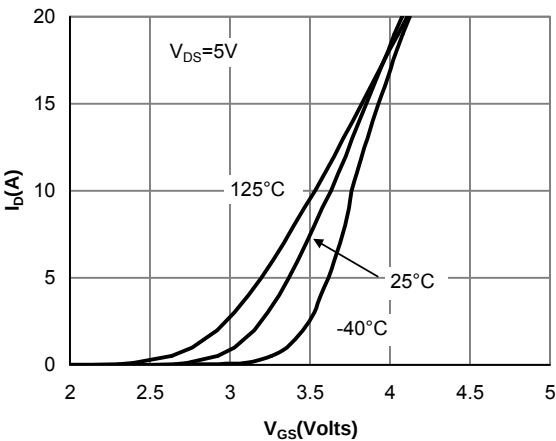


Figure 2: Transfer Characteristics

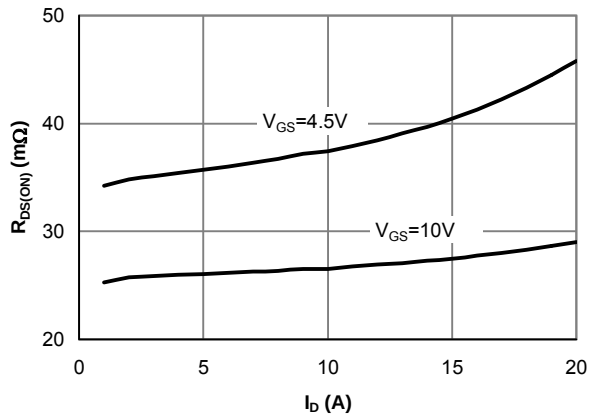


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

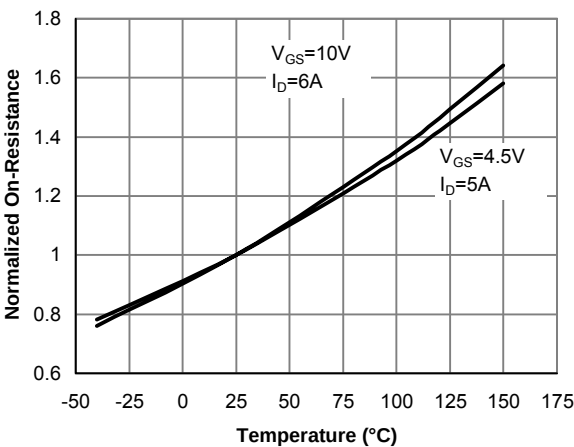


Figure 4: On-Resistance vs. Junction Temperature

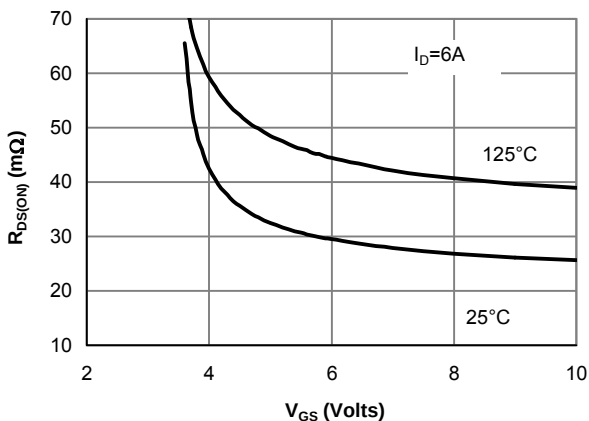


Figure 5: On-Resistance vs. Gate-Source Voltage

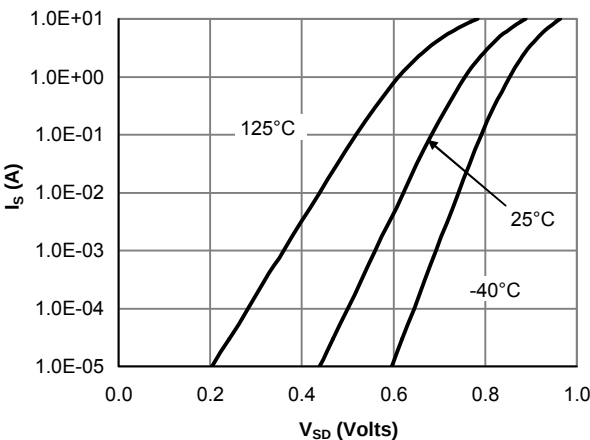


Figure 6: Body-Diode Characteristics

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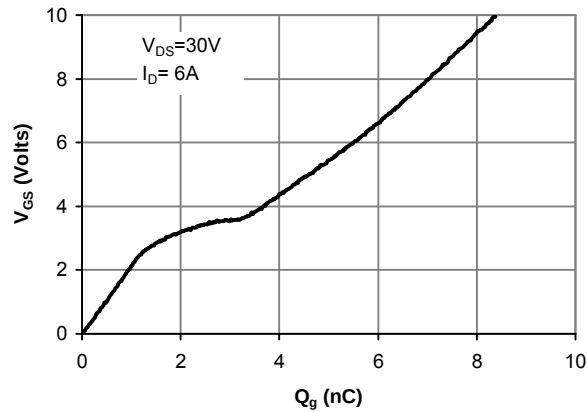


Figure 7: Gate-Charge Characteristics

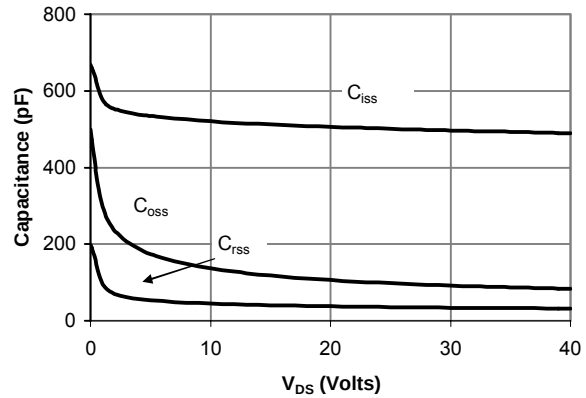


Figure 8: Capacitance Characteristics

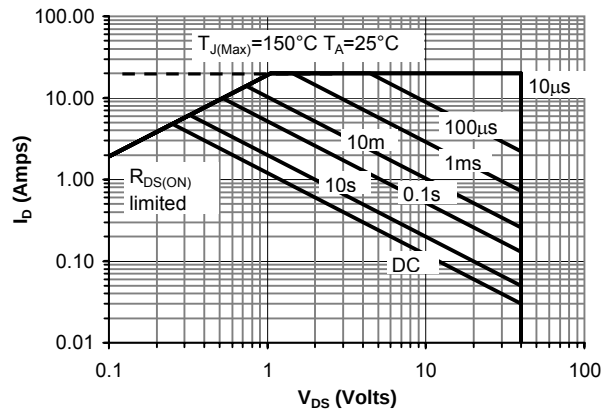


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

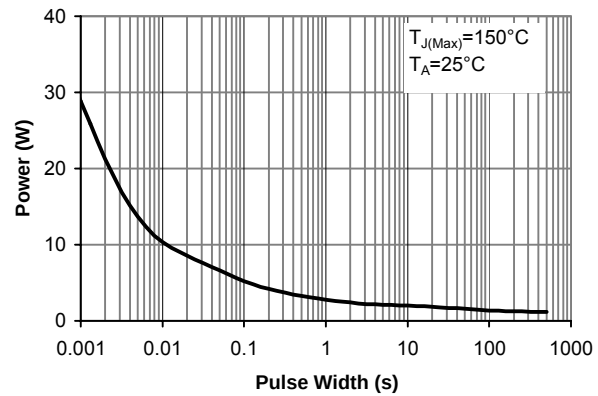


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

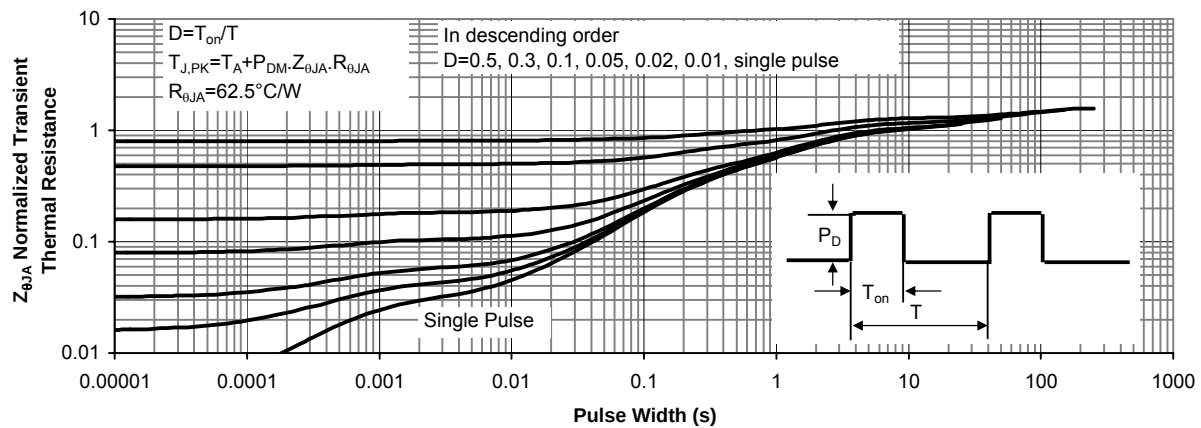


Figure 11: Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	-40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-32V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±150	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-1	-2	-3	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-25			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-5A T _J =125°C		40 56	48 68	mΩ
		V _{GS} =-4.5V, I _D =-4A		61	75	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-5A		11		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.76	-1	V
I _S	Maximum Body-Diode Continuous Current				3.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-20V, f=1MHz		1006		pF
C _{oss}	Output Capacitance			152		pF
C _{rss}	Reverse Transfer Capacitance			77		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		11		Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge (10V)	V _{GS} =-10V, V _{DS} =-20V, I _D =-5A		17.4		nC
Q _g (4.5V)	Total Gate Charge (4.5V)			8.9		nC
Q _{gs}	Gate Source Charge			3.1		nC
Q _{gd}	Gate Drain Charge			4.6		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-20V, R _L =4Ω, R _{GEN} =3Ω		9.7		ns
t _r	Turn-On Rise Time			6.3		ns
t _{D(off)}	Turn-Off DelayTime			35.5		ns
t _f	Turn-Off Fall Time			26		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-5A, dI/dt=100A/μs		21.8		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-5A, dI/dt=100A/μs		15.5		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6,12,14 are obtained using <300μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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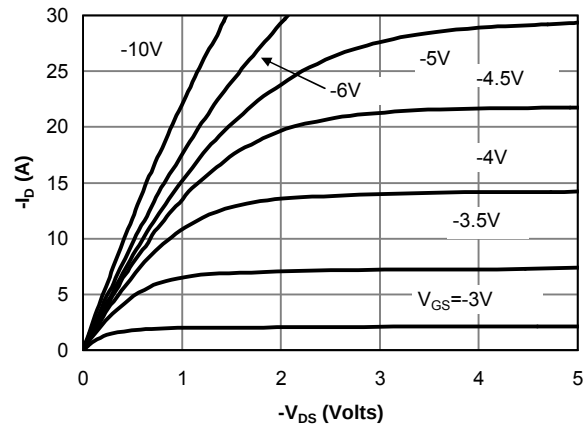


Fig 1: On-Region Characteristics

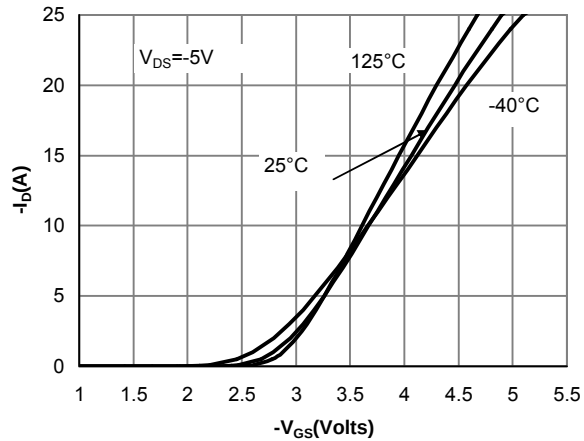


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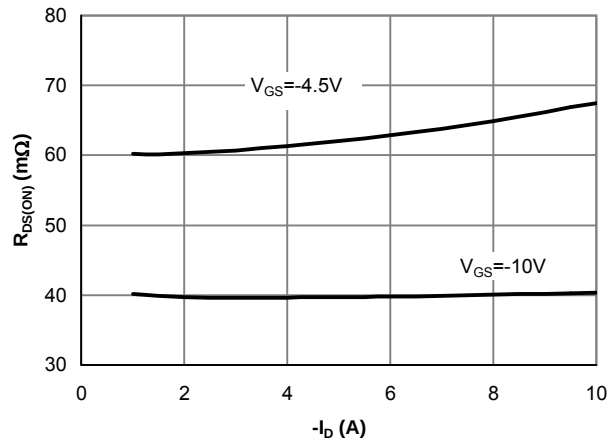


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

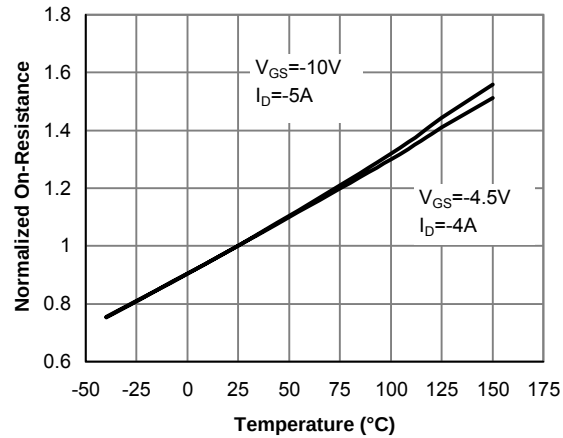


Figure 4: On-Resistance vs. Junction Temperature

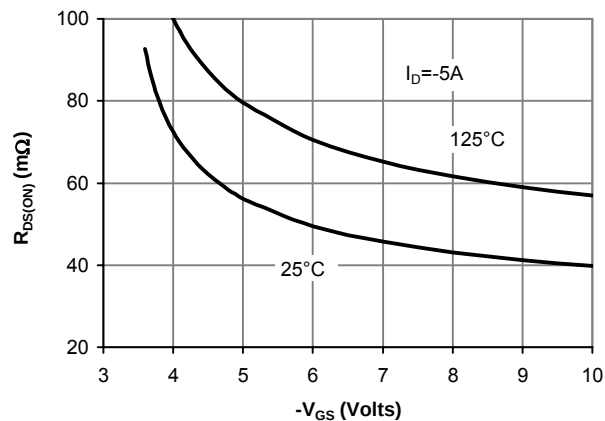


Figure 5: On-Resistance vs. Gate-Source Voltage

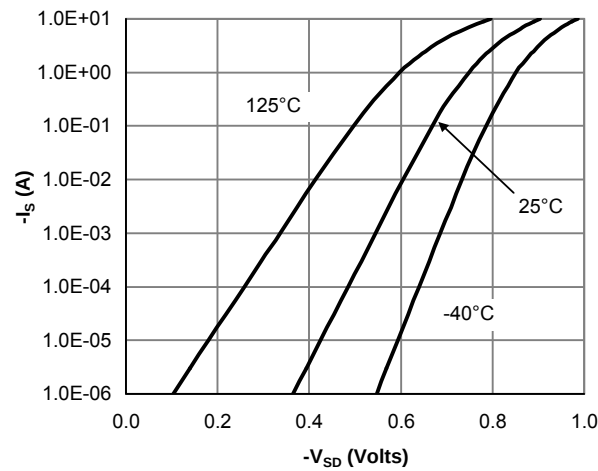


Figure 6: Body-Diode Characteristics

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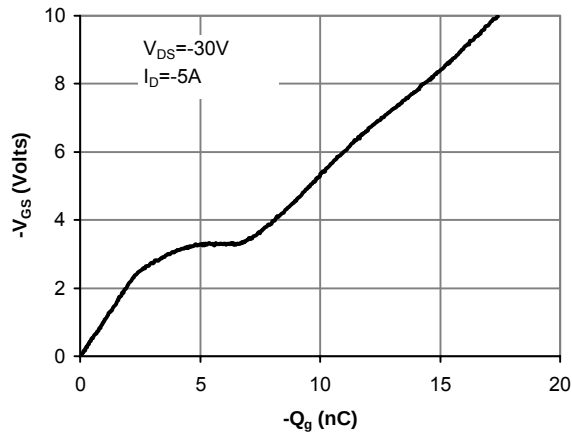


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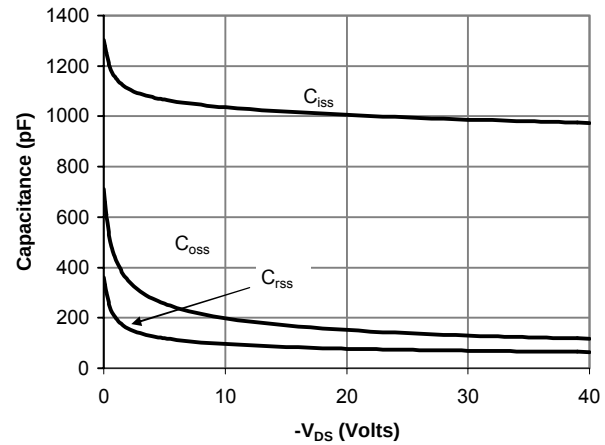


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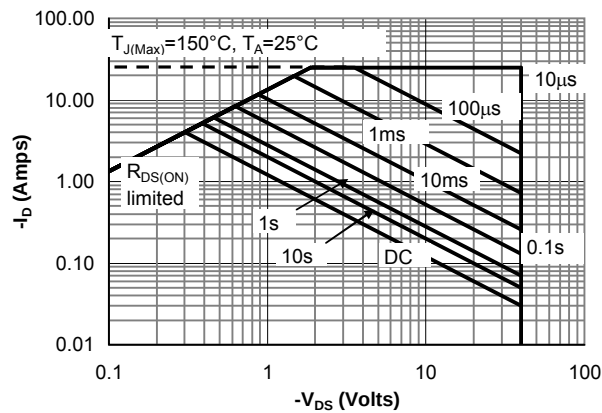


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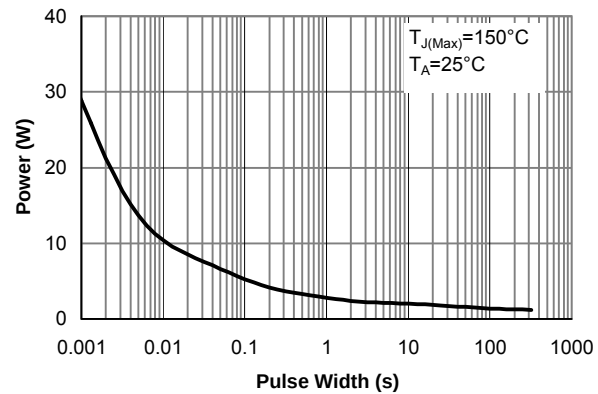


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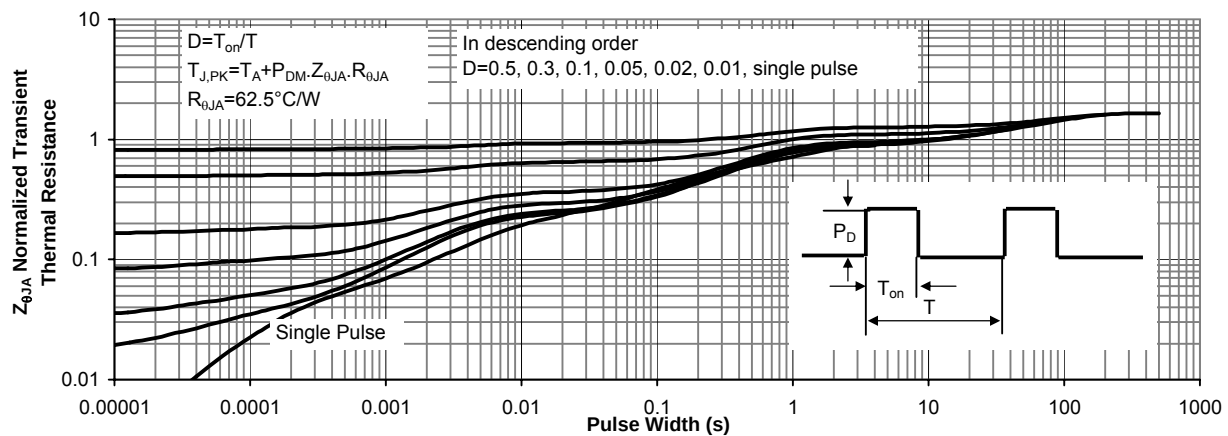


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)