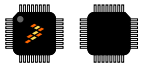
Kinetis K80 Sub-Family

High performance ARM® Cortex®-M4F MCU with up to 256KB of Flash, 256KB of SRAM, Full Speed USB connectivity, and QuadSPI for interfacing to Serial NOR flash

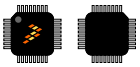
The K80 sub-family extends Kinetis products with new features including QuadSPI serial flash interface and separate voltage domain for a sub-set of IO pins. The QuadSPI interface supports connections to Non-Volatile Memory for data or code. The extended memory resources allow developers to enhance their embedded applications with greater capability and features. Software compatibility with previous Kinetis devices ensures quick transitions from other Kinetis subfamilies. Enhancements include High Speed RUN for greater performance, and smart Peripherals like LPUART which can operate in STOP modes.

MK80FN256VLL15
MK80FN256VDC15
MK80FN256VLQ15
MK80FN256CAx15

121 XFBGA (DC)
8 x 8 x 0.5 mm Pitch 0.65 mm



100 LQFP (LL)
14 x 14 x 1.7 Pitch 0.5mm



144 LQFP (LQ)
20 x 20 x 1.6 Pitch 0.5 mm

121 WLCSP (Ax)
4.64 mm x 4.53 mm

Performance

- Up to 150 MHz ARM Cortex-M4 based core with DSP instructions and Single Precision Floating Point unit

Memories and memory expansion

- Up to 256 KB program flash with 256 KB RAM
- FlexBus external bus interface and SDRAM controller
- Dual QuadSPI with XIP
- 32 KB Boot ROM with built in bootloader
- Supports SDR and DDR serial flash and octal configurations

System and Clocks

- Multiple low-power modes
- Memory protection unit with multi-master protection
- 3 to 32 MHz main crystal oscillator
- 32 kHz low power crystal oscillator
- 48 MHz internal reference

Timers

- One 4 ch-Periodic interrupt timer
- Two 16-bit low-power timer PWM modules
- Two 8-ch motor control/general purpose/PWM timers
- Two 2-ch quadrature decoder/general purpose timers
- Real-time clock with independent 3.3V power domain
- Programmable delay block

Human-machine interface

- Low-power hardware touch sensor interface (TSI)
- General-purpose input/output

Analog modules

- One 16-bit SAR ADCs, two 6-bit DAC and one 12-bit DAC
- Two analog comparators (CMP) containing a 6-bit DAC and programmable reference input
- Voltage reference 1.2V

Operating Characteristics

- Main VDD Voltage and Flash write voltage range:1.71V–3.6 V
- Temperature range (ambient): -40 to 105°C
- Independent V_{DDIO} for PORTE (QuadSPI): 1.71V–3.6 V

Communication interfaces

- USB full-/low-speed On-the-Go controller
- Secure Digital Host Controller (SDHC) and FlexIO
- One I2S module, three SPI, four I2C modules and five LPUART modules

Security

- Hardware random-number generator
- Supports DES, AES, SHA accelerator (CAU)
- Multiple levels of embedded flash security

Ordering Information

Part Number	Memory		Maximum number of I\O's
	Flash	SRAM	
MK80FN256VLL15	256 KB	256 KB	66
MK80FN256VDC15	256 KB	256 KB	87
MK80FN256CAx15R[1]	256 KB	256 KB	87
MK80FN256VLQ15[2]	256 KB	256 KB	102

1. The 121-pin WLCSP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.
2. The 144-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

Related Resources

Type	Description	Resource
Product Selector	The Product Selector lets you find the right Kinetis part for your design.	K-Series Product Selector
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	K8x Fact Sheet
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K80P121M150SF5RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_K_1N03P[1]
Package drawing	Package dimensions are provided in package drawings.	• LQFP 100-pin: 98ASS23308W[1] • XFBGA 121-pin: 98ASA00595D[1] • LQFP 144-pin: 98ASS23177W[2] • WLCSP 121-pin: Under development[2]

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.
2. This package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

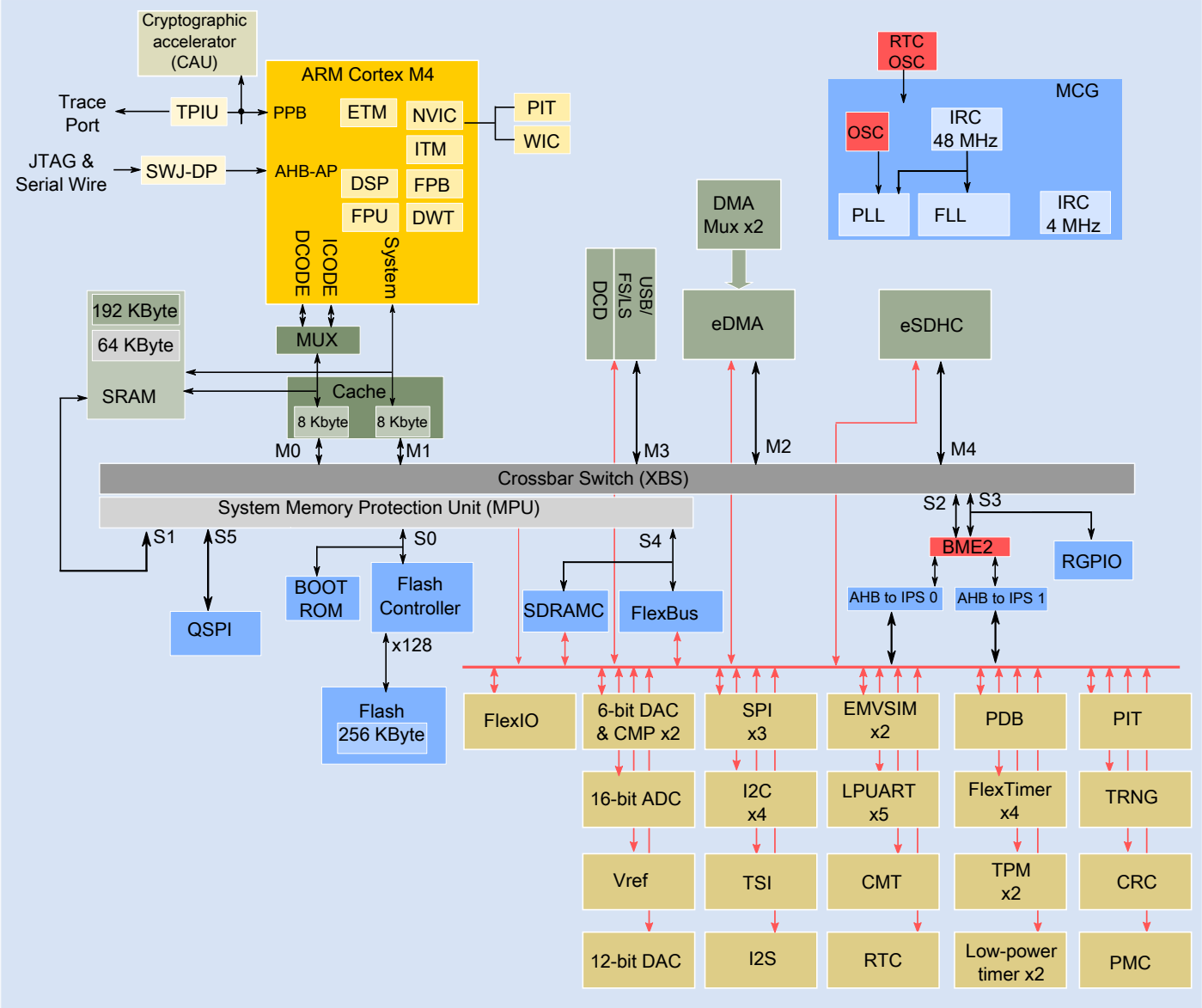


Figure 1. K80 Block Diagram

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1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{DDIO_E}	V_{DDIO_E} is an independent voltage supply for PORTE [1]	–0.3	3.8	V
V_{BAT}	RTC supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
V_{IO}	Input voltage (except PORTE, VBAT domain pins, and USB0)[2]	–0.3	V_{DD} + 0.3	V
V_{IO_E}	PORTE input voltage[3]	–0.3	V_{DDIO_E} + 0.3	V
I_D	Maximum current single pin limit (digital output pins)	–25	25	mA
VREGIN	USB regulator input	–0.3	6.0	V
V_{USB0_Dx}	USB0_DP and USB_DM input voltage	–0.3	3.63	V

1. V_{DDIO_E} is independent of the V_{DD} domain and can operate at a voltage independent of V_{DD}. However, it is required that the V_{DD} domain be powered up before V_{DDIO_E}. V_{DDIO_E} must never be higher than V_{DD} during power ramp up, or power down. V_{DD} and V_{DDIO_E} may ramp together if tied to the same power supply.
2. Includes ADC, CMP, and RESET_b inputs.
3. PORTE analog input voltages cannot exceed V_{DDIO_E} supply when $V_{DD} \geq V_{DDIO\_E}$. PORTE analog input voltages cannot exceed V_{DD} supply when $V_{DD} < V_{DDIO\_E}$.

1.4.1 Recommended POR Sequencing

Cases

- VDD = VDDIO_E
- VDD > VDDIO_E
- VDD < VDDIO_E

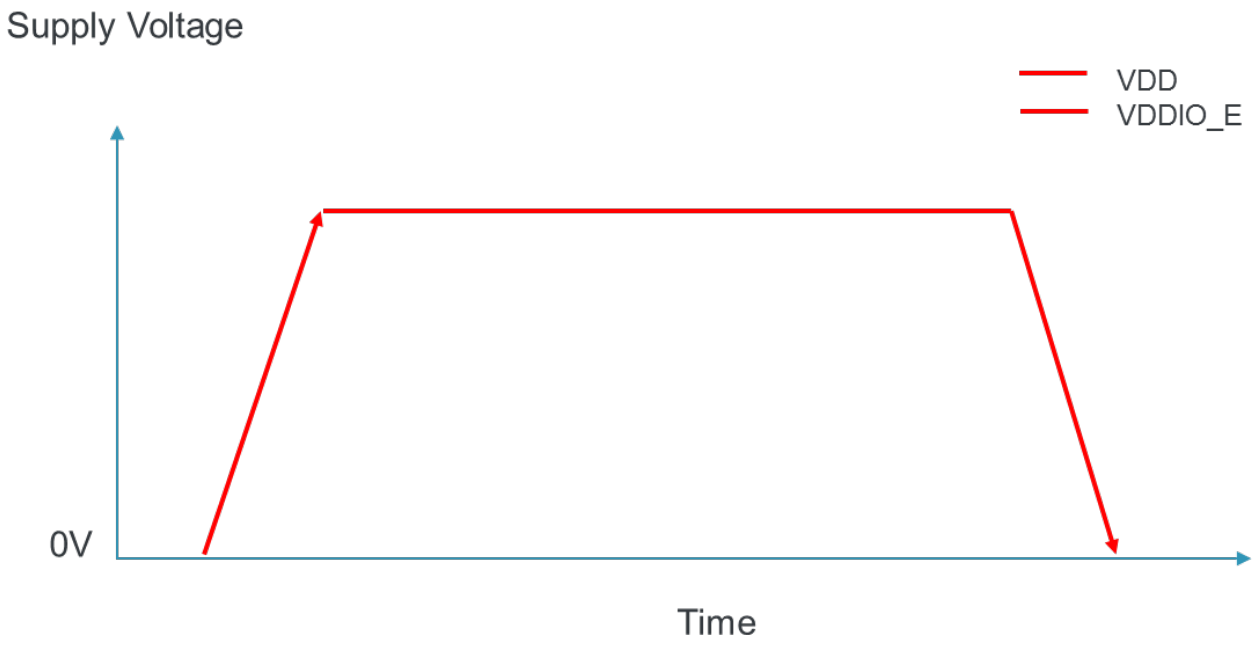


Figure 2. VDD = VDDIO_E

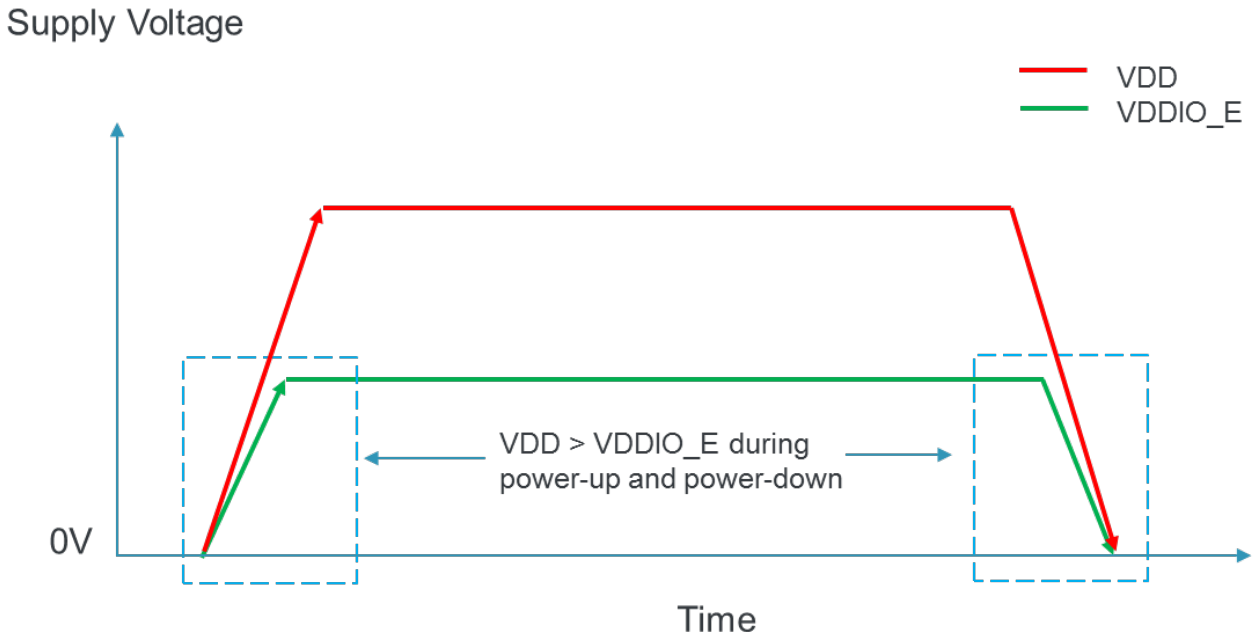


Figure 3. VDD > VDDIO_E

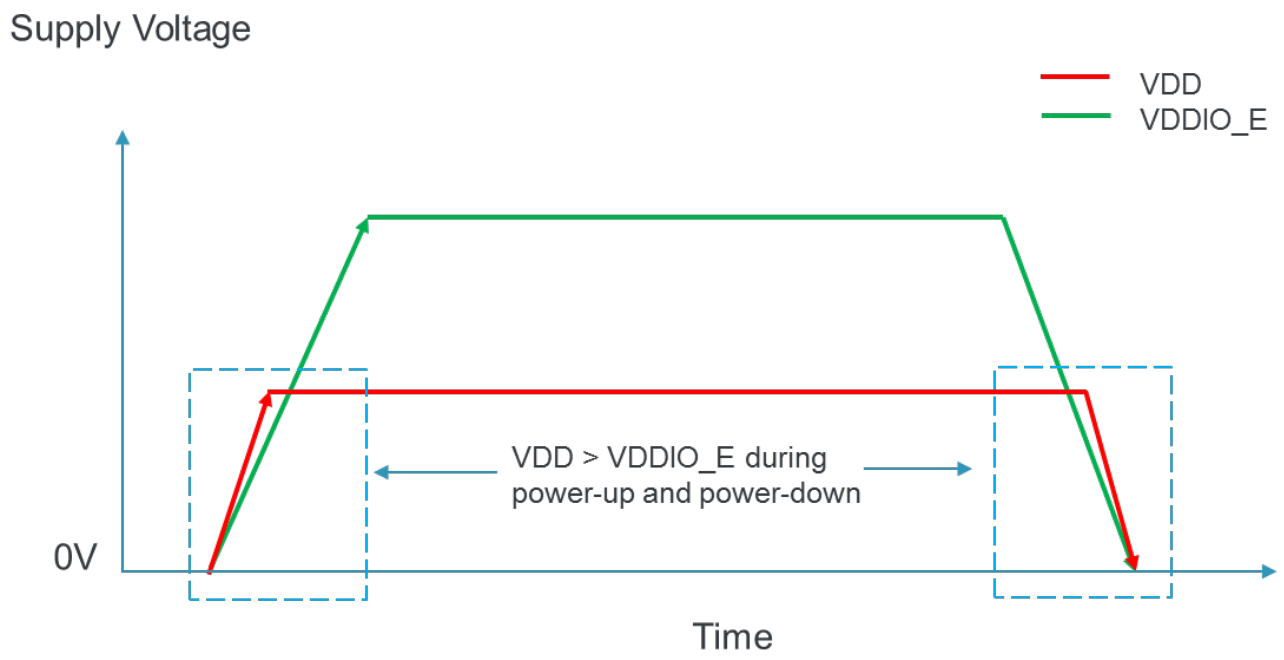


Figure 4. VDD < VDDIO_E

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

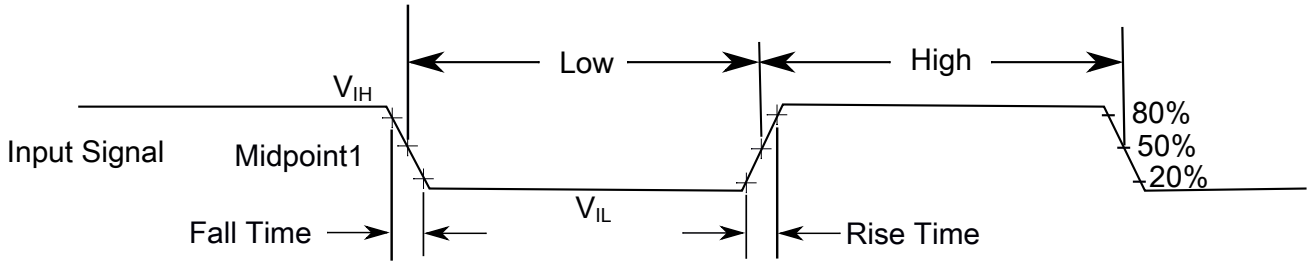


Figure 5. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins

- have C_L=15pF loads,
- are slew rate disabled, and
- are normal drive strength

2. input pins
   - have their passive filter disabled (PORTx_PCRn[PFE]=0)

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDIO_E}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	0.7 × V_{DD} 0.75 × V_{DD}	— —	V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	— —	0.35 × V_{DD} 0.3 × V_{DD}	V V	
V_{IH_E}	Input high voltage • 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V • 1.7 V ≤ V_{DDIO_E} ≤ 2.7 V	0.7 × V_{DDIO_E} 0.75 × V_{DDIO_E}	— —	V V	
V_{IL_E}	Input low voltage • 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V • 1.7 V ≤ V_{DDIO_E} ≤ 2.7 V	— —	0.35 × V_{DDIO_E} 0.3 × V_{DDIO_E}	V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
V_{HYS_E}	Input hysteresis	0.06 × V_{DDIO_E}	—	V	
I_{ICIO}	I/O pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	1

Table continues on the next page...

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Pseudo Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD} or V_{DDIO_E}. If V_{IN} is less than -0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(-0.3-V_{IN})/|I_{ICIO}|$. The actual resistor value should be an order of magnitude higher to tolerate transient voltages.
2. Open drain outputs must be pulled to VDD.

2.2.2 HVD, LVD and POR operating requirements

Table 2. V_{DD} supply HVD, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{HVDH}	High Voltage Detect (High Trip Point)	—	3.72	—	V	
V_{HVDL}	High Voltage Detect (Low Trip Point)	—	3.46	—	V	
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	60	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	40	—	mV	

Table continues on the next page...

Table 2. V_{DD} supply HVD, LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

NOTE

There is no LVD circuit for VDDIO domain

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
V_{OH}	Output high voltage — normal drive strength					2, 3
	IO Group 1					
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -5mA	V_{BAT} – 0.5	—	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -2.5mA	V_{BAT} – 0.5	—	—	V	
	IO Groups 2 and 3					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -10mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -5mA	V_{DD} – 0.5	—	—	V	
	IO Group 4					
	• 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V, I_{OH} = -5mA	V_{DDIO_E} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DDIO_E} ≤ 2.7 V, I_{OH} = -2.5mA	V_{DDIO_E} – 0.5	—	—	V	
	Output high voltage — High drive strength					2
	IO Group 3					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10mA	V_{DD} – 0.5	—	—	V	
	IO Group 4	V_{DDIO_E} – 0.5	—	—	V	
	• 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V, I_{OH} = -15mA	V_{DDIO_E} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DDIO_E} ≤ 2.7 V, I_{OH} = -7.5mA					
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — normal drive strength					2, 4, 5
	IO Group 1					

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = -5mA	—	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = -2.5mA	—	—	0.5	V	
	IO Groups 2 and 3					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = -10mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = -5mA	—	—	0.5	V	
	IO Group 4					
	• 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V, I_{OL} = -5mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DDIO_E} ≤ 2.7 V, I_{OL} = -2.5mA	—	—	0.5	V	
	Output low voltage — High drive strength					2, 4
	IO Group 3					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = -20mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = -10mA	—	—	0.5	V	
	IO Group 4					
	• 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V, I_{OL} = -15mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DDIO_E} ≤ 2.7 V, I_{OL} = -7.5mA	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current					6, 7, 8
	V_{DD} domain pins	—	0.002	0.5	µA	
	• V_{SS} ≤ V_{IN} ≤ V_{DD}	—	0.002	0.5	µA	
	PORTE pins					
	• V_{SS} ≤ V_{IN} ≤ V_{DDIO_E}	—	0.002	0.5	µA	
	V_{BAT} domain pins					
	• V_{SS} ≤ V_{IN} ≤ V_{BAT}					
R_{PU}	Internal pullup resistors(except RTC_WAKEUP pins)	20	—	50	kΩ	9
R_{PD}	Internal pulldown resistors (except RTC_WAKEUP pins)	20	—	50	kΩ	10

1. Typical values characterized at 25°C and V_{DD} = 3.6V unless otherwise noted.
2. IO Group 1 includes V_{BAT} domain pins: RTC_WAKEUP_b. IO Group 2 includes V_{DD} domain pins: PORTA, PORTB, PORTC, and PORTD, except PTA4. IO Group 3 includes V_{DD} domain pins: PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7. IO Group 4 includes V_{DDIO_E} domain pins: PORTE.
3. PTA4 has lower drive strength: I_{OH} = -5mA for high V_{DD} range; I_{OH} = -2.5mA for low V_{DD} range.
4. Open drain outputs must be pulled to V_{DD}.
5. PTA4 has lower drive strength: I_{OL} = 5mA for high V_{DD} range; I_{OL} = 2.5mA for low V_{DD} range.
6. V_{DD} domain pins include ADC, CMP, and RESET_b inputs. Measured at V_{DD} = 3.6V.
7. PORTE analog input voltages cannot exceed V_{DDIO_E} supply when V_{DD} ≥ V_{DDIO_E}. PORTE analog input voltages cannot exceed V_{DD} supply when V_{DD} < V_{DDIO_E}.
8. V_{BAT} domain pins include EXTAL32, XTAL32, and RTC_WAKEUP_b pins.
9. Measured at minimum supply voltage and V_{IN} = V_{SS}
10. Measured at minimum supply voltage and V_{IN} = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx –> RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100MHz
- Bus clock = 50MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode=FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	µs	
	• VLLS0 –> RUN	—	154	µs	
	• VLLS1 –> RUN	—	154	µs	
	• VLLS2 –> RUN	—	92	µs	
	• VLLS3 –> RUN	—	92	µs	
	• LLS2 –> RUN	—	6.3	µs	
	• LLS3 –> RUN	—	6.3	µs	
	• VLPS –> RUN	—	5.3	µs	
	• STOP –> RUN	—	5.3	µs	

Table 6. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							nA
	VLLS1	440	490	540	560	570	580	
	VLLS3	440	490	540	560	570	580	
	LLS2	490	490	540	560	570	680	
	LLS3	490	490	540	560	570	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	234	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	µA

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 7. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from internal flash @ 3.0V					2
	• @ 25°C	—	28	31.55	mA	
	• @ 105°C	—	39.6	50.10		
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from internal flash @ 3.0V					3, 4
	• @ 25°C	—	54	57.55	mA	
	• @ 105°C	—	70	80.50		
I_{DD_RUNCO}	Run mode current in compute operation - 120 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0 V					5
	• @ 25°C	—	25.1	28.65	mA	
	• @ 105°C	—	37.8	48.30		
I_{DD_HSRUN}	Run mode current — all peripheral clocks disabled, code executing from internal flash @ 3.0V					6
	• @ 25°C	—	38	40.70	mA	
	• @ 105°C	—	51.7	65.04		
I_{DD_HSRUN}	Run mode current — all peripheral clocks enabled, code executing from internal flash @ 3.0V					7, 8
	• @ 25°C	—	48	50.70	mA	
	• @ 105°C	—	63.7	77.04		
$I_{DD\_HSRUNCO}$	HSRun mode current in compute operation – 150 MHz core/ 25 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0V					
	• @ 25°C	—	34.5	37.2	mA	
	• @ 105°C	—	50.3	63.64		
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled					9
	• @ 25°C	—	14.2	19.87	mA	
	• @ 105°C	—	26.2	35.66		
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks enabled					9
		—	24.4	30.07	mA	

Table continues on the next page...

Table 7. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 25°C • @ 105°C	— —	36.6 —	46.06 —		
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled • @ 25°C • @ 105°C	 — —	 0.94 3.99	 1.10 7.62	 mA	10
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled • @ 25°C • @ 105°C	 — —	 1.36 4.4	 1.52 8.03	 mA	11
$I_{DD\_VLPRCO\_CM}$	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, LPTMR running with 4 MHz internal reference clock, CoreMark benchmark code executing from internal flash at 3.0 V • @ 25°C • @ 105°C	 — —	 1000 3650	 — —	 µA	12
I_{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 3.0 V • @ 25°C • @ 105°C	 — —	 3.95 17.71	 5.75 27.15	 mA	5
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled • @ 25°C • @ 105°C	 — —	 0.45 3.28	 0.63 6.87	 mA	13
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks enabled • @ 25°C • @ 105°C	 — —	 0.75 3.6	 0.93 7.19	 mA	
I_{DD_STOP}	Stop mode current at 3.0 V • @ 25°C • @ 105°C	 — —	 0.55 5.67	 0.85 9.59	 mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V • @ 25°C • @ 105°C	 — —	 91.48 1798.38	 240.90 3796.94	 µA	
I_{DD_LLS2}	Low leakage stop mode current at 3.0 V • @ 25°C • @ 105°C	 — —	 4.94 73.68	 7.14 121.9	 µA	

Table continues on the next page...

Table 7. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_LLS3}	Low leakage stop mode current at 3.0 V • @ 25°C • @ 105°C	 — —	 7.78 160.91	 13.16 284.31	 µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ 25°C • @ 105°C	 — —	 5.63 117.89	 9.34 202.55	 µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • @ 25°C • @ 105°C	 — —	 3.13 29.49	 4.04 48.7	 µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ 25°C • @ 105°C	 — —	 1.05 15.31	 1.36 18.56	 µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled • @ 25°C • @ 105°C	 — —	 0.62 13.92	 0.84 16.95	 µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled • @ 25°C • @ 105°C	 — —	 0.33 13.42	 0.53 16.44	 µA	
I_{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V • @ 25°C • @ 105°C	 — —	 0.19 2.56	 0.23 3.71	 µA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers @ 1.8V • @ 25°C • @ 105°C	 — —	 0.57 2.52	 0.64 5.82	 µA	14

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 150 MHz core and system clock, 75 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configure for PEE mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. MCG configured for PEE mode.
6. 150 MHz core and system clock, 50 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.

7. 150 MHz core and system clock, 50 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
8. Max values are measured with CPU executing DSP instructions.
9. 120 MHz core and system clock, 60MHz bus clock, and FlexBus. MCG configured for PEE mode.
10. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
11. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
12. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
13. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
14. Includes 32kHz oscillator current and RTC operation.

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE
- V_{DD}=V_{DDA}=V_{DDIO_E}

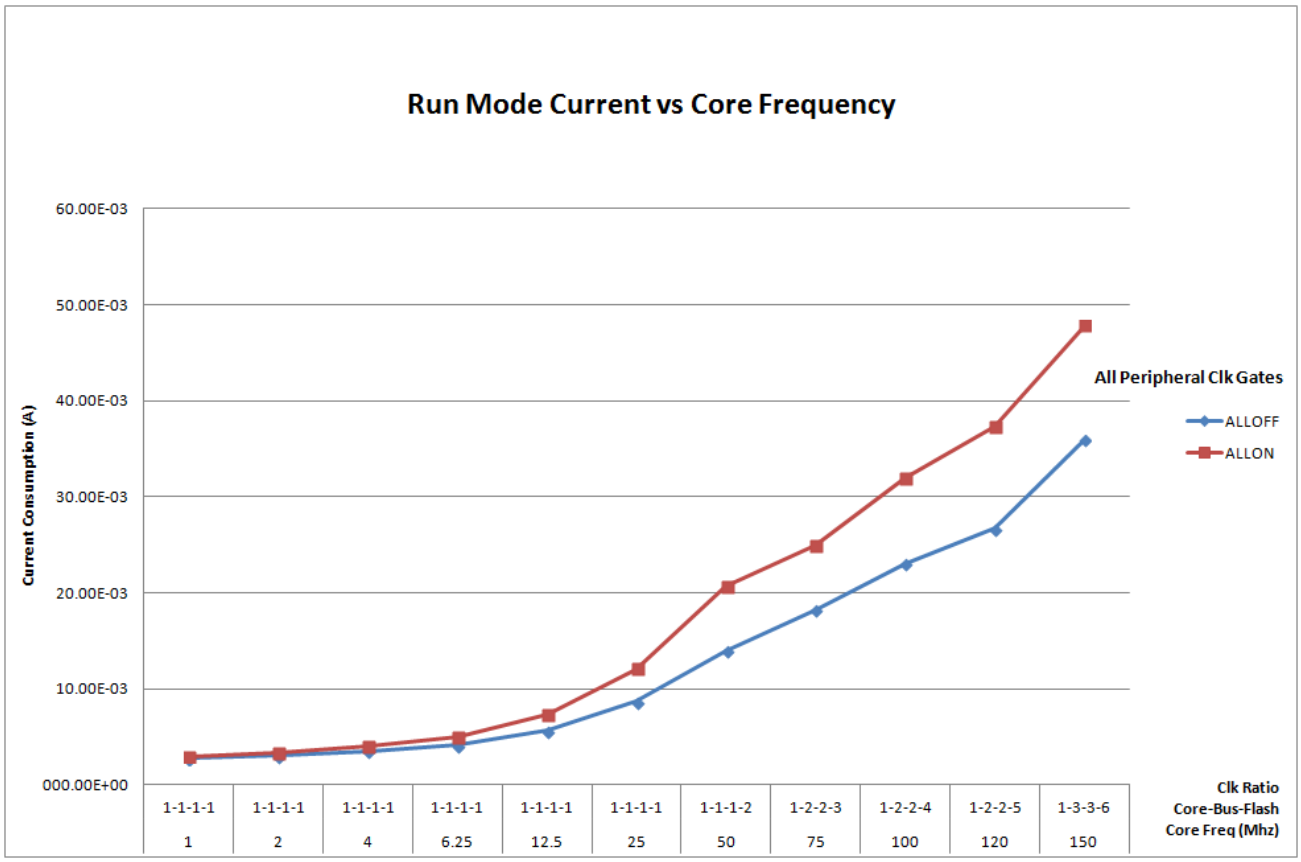


Figure 6. Run mode supply current vs. core frequency

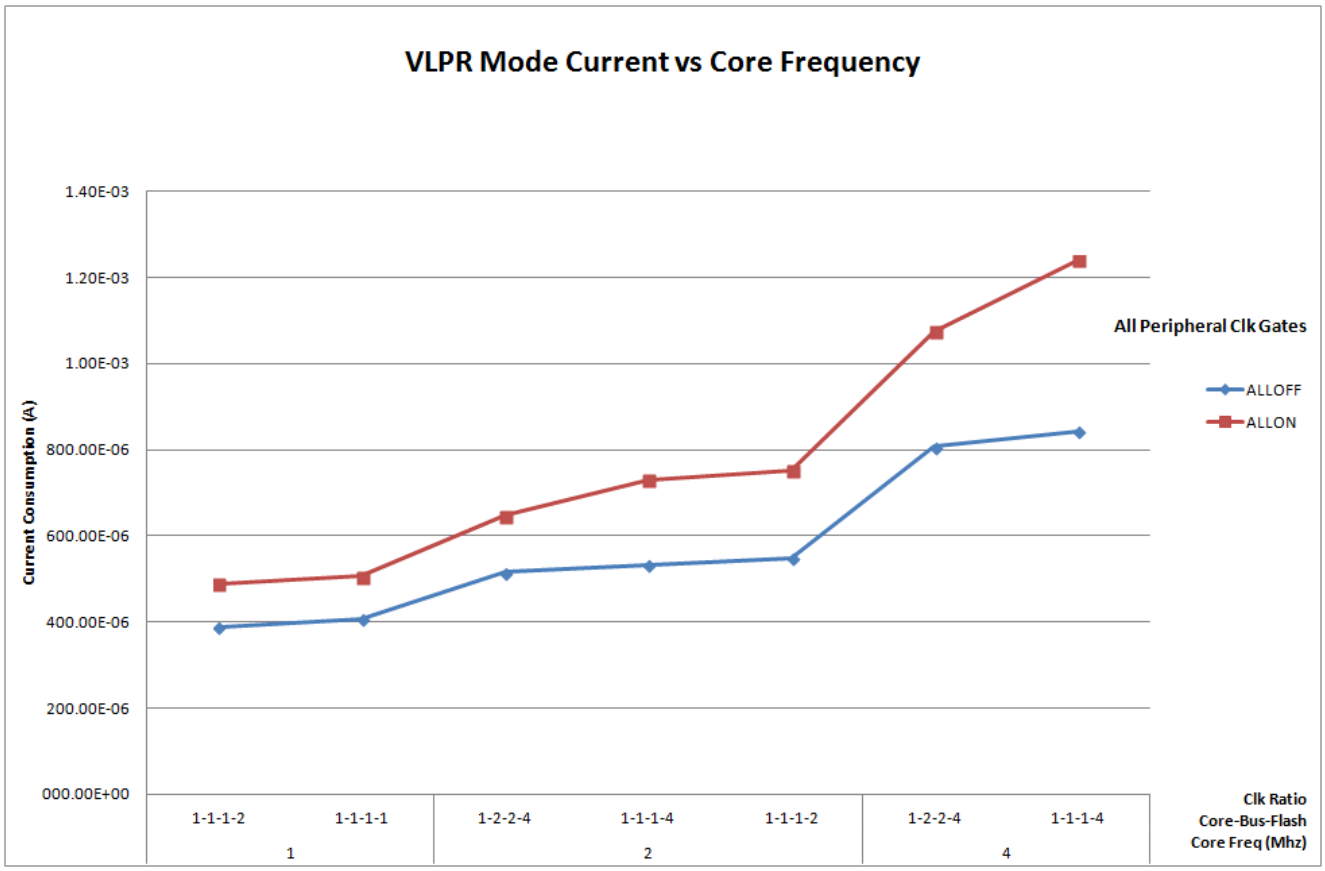


Figure 7. VLPR mode supply current vs. core frequency

2.2.6 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from Freescale on request.

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f_{SYS}	System and core clock	—	150	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f_{SYS}	System and core clock	—	120	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	75	MHz	
FB_CLK	FlexBus clock	—	75	MHz	
f_{FLASH}	Flash clock	—	28	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
$f_{FlexCAN\_ERCLK}$	FlexCAN external reference clock	—	8	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CMT, timers, and I^2C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	NMI_b pin interrupt pulse width (analog filter enabled) — Asynchronous path	100	—	ns	
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External RESET_b input pulse width (digital glitch filter disabled)	100	—	ns	
	Port rise and fall time (high drive strength) • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew disabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	 — — — —	 34 16 10 8	 ns ns ns ns	4, 5
	Port rise and fall time (low drive strength) • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew disabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	 — — — —	 34 16 7 5	 ns ns ns ns	6, 7
	Port rise and fall time (high drive strength) • Slew enabled • $1.71 \le V_{DDIO\_E} \le 2.7V$ • $2.7 \le V_{DDIO\_E} \le 3.6V$ • Slew disabled • $1.71 \le V_{DDIO\_E} \le 2.7V$ • $2.7 \le V_{DDIO\_E} \le 3.6V$	 — — — —	 34 16 7 5	 ns ns ns ns	5, 8
	Port rise and fall time (low drive strength) • Slew enabled	 — —	 34 16	 ns ns	7, 8

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	• 1.71 ≤ V_{DDIO_E} ≤ 2.7V • 2.7 ≤ V_{DDIO_E} ≤ 3.6V • Slew disabled • 1.71 ≤ V_{DDIO_E} ≤ 2.7V • 2.7 ≤ V_{DDIO_E} ≤ 3.6V	— —	7 5	ns ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry in run modes.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7.
5. 75 pF load.
6. Ports A, B, C, and D.
7. 25 pF load.
8. Port E pins only.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1,

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is:

   $T_J = T_A + \theta_{JA}$ x chip power dissipation

2.4.2 Thermal attributes

Table 12. Thermal attributes

Board type	Symbol	Description	100 LQFP	121 XFBGA	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	52	71	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	39	36.8	°C/W	1

Table continues on the next page...

Table 12. Thermal attributes (continued)

Board type	Symbol	Description	100 LQFP	121 XFBGA	Unit	Notes
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	42	55	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	33	32.2	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	18	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	11	12.2	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	0.25	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 Debug trace timing specifications

Table 13. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	1.5	—	ns
T_h	Data hold	1.0	—	ns

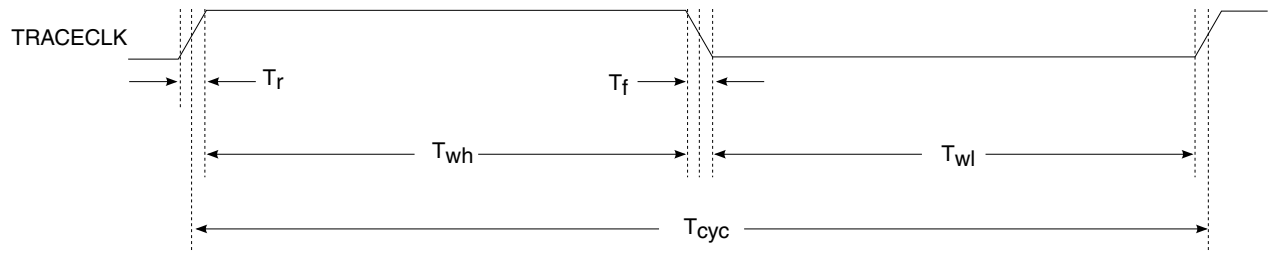


Figure 8. TRACE_CLKOUT specifications

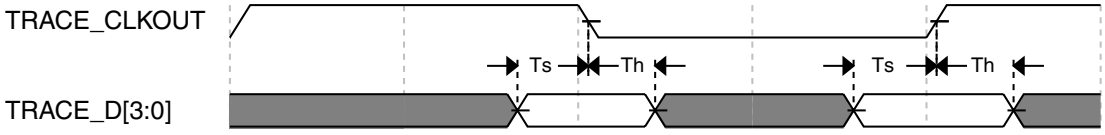


Figure 9. Trace data specifications

3.1.2 JTAG electricals

Table 14. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	28	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns

Table continues on the next page...

Table 14. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 15. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
	• Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	30.6	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	19.0	ns
J12	TCLK low to TDO high-Z	—	17.0	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

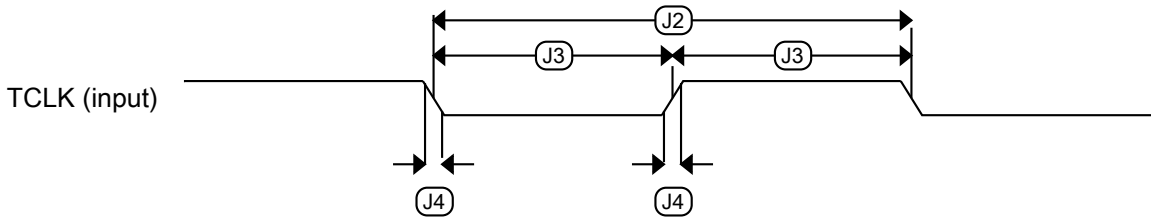


Figure 10. Test clock input timing

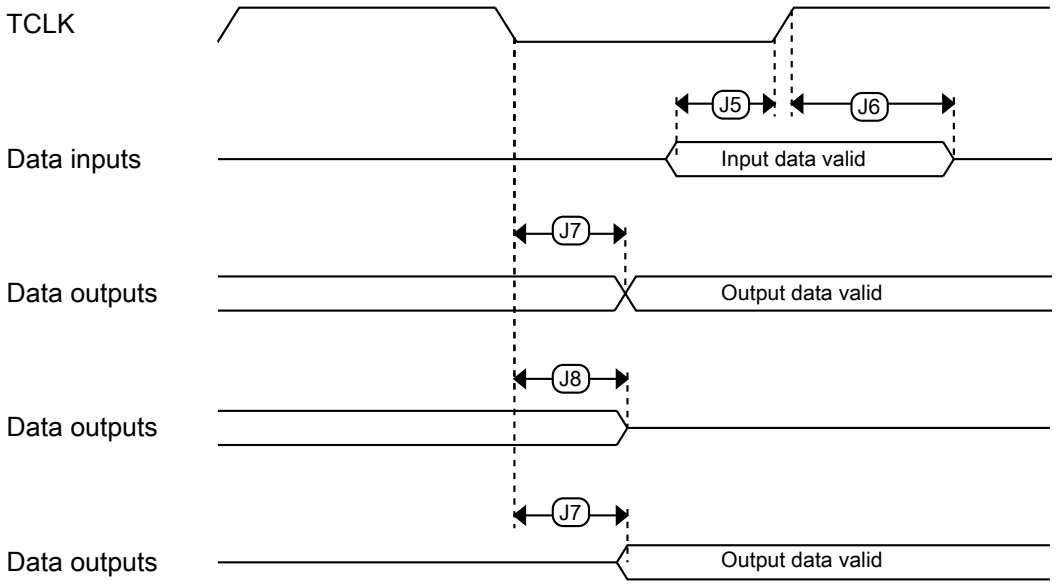


Figure 11. Boundary scan (JTAG) timing

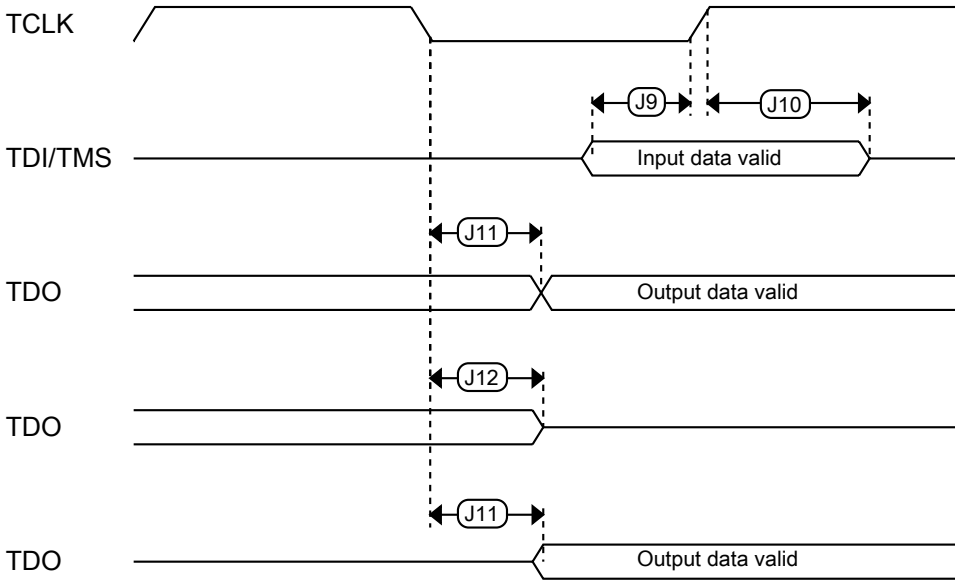


Figure 12. Test Access Port timing

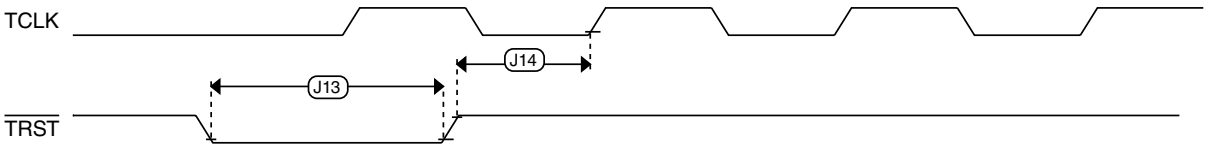


Figure 13. TRST timing

3.2 Clock modules

3.2.1 MCG specifications

Table 16. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
I_{ints}	Internal reference (slow clock) current	—	20	—	µA	
$t_{irefsts}$	[O:] Internal reference (slow clock) startup time	—	32	—	µs	
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	±1	± 2	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.5	± 1	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
I_{intf}	Internal reference (fast clock) current	—	25	—	µA	
$t_{irefsts}$	[L:] Internal reference startup time (fast clock)	—	10	15	µs	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00 ext clk freq: above (3/5)f_{int} never reset	(3/5) x f_{ints_t}	—	—	kHz	

Table continues on the next page...

Table 16. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
	ext clk freq: between (2/5)fint and (3/5)f_{int} maybe reset (phase dependency) ext clk freq: below (2/5)f_{int} always reset						
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11 ext clk freq: above (16/5)f_{int} never reset ext clk freq: between (15/5)f_{int} and (16/5)f_{int} maybe reset (phase dependency) ext clk freq: below (15/5)f_{int} always reset		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco_ut}	DCO output frequency range — untrimmed	Low range (DRS=00, DMX32=0) 640 × f_{ints_ut}	16.0	23.04	26.66	MHz	2
		Mid range (DRS=01, DMX32=0) 1280 × f_{ints_ut}	32.0	46.08	53.32		
		Mid-high range (DRS=10, DMX32=0) 1920 × f_{ints_ut}	48.0	69.12	79.99		
		High range (DRS=11, DMX32=0) 2560 × f_{ints_ut}	64.0	92.16	106.65		
		Low range (DRS=00, DMX32=1) 732 × f_{ints_ut}	18.3	26.35	30.50		
		Mid range (DRS=01, DMX32=1) 1464 × f_{ints_ut}	36.6	52.70	60.99		
		Mid-high range (DRS=10, DMX32=1) 2197 × f_{ints_ut}	54.93	79.09	91.53		
		High range (DRS=11, DMX32=1) 2929 × f_{ints_ut}	73.23	105.44	122.02		
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01)	40	41.94	50	MHz	

Table continues on the next page...

Table 16. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
		1280 × f_{fll_ref}					
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	7
PLL							
f_{pll_ref}	PLL reference frequency range		8	—	16	MHz	
f_{vcoclk_2x}	VCO output frequency		180	—	360	MHz	
f_{vcoclk}	PLL output frequency		90	—	180	MHz	
f_{vcoclk_90}	PLL quadrature output frequency		90	—	180	MHz	
I_{pll}	PLL operating current • VCO @ 176 MHz (f_{pll_ref} = 8 MHz, VDIV multiplier = 22, PRDIV divide=1)		—	1.1	—	mA	8
I_{pll}	PLL operating current • VCO @ 360 MHz (f_{pll_ref} = 8 MHz, VDIV multiplier = 45, PRDIV divide=1)		—	2	—	mA	8
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 180 MHz • f_{vco} = 360 MHz		— —	100 75	— —	ps ps	9
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 180 MHz • f_{vco} = 360 MHz		— —	600 300	— —	ps ps	9
D_{unl}	Lock exit frequency tolerance		± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time		—	—	150×10^{-6} + 1075(1/f_{pll_ref})	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. This applies when SCTRIM at value (0x80) and SCFTRIM control bit at value (0x0).
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.2.2 IRC48M specifications

Table 17. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DD48M}	Supply current	—	520	—	µA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature • Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0) • Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	— —	± 0.5 ± 0.5	± 1.0 ± 1.5	$\%f_{irc48m}$	
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature • Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.5	± 1.0	$\%f_{irc48m}$	
Δf_{irc48m_cl}	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	± 0.1	$\%f_{host}$	1
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	µs	2

1. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1).
2. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
   - USB_CLK_RECOVER_IRC_EN[IRC_EN]=1, or
   - MCG_C7[OSCSEL]=10, or
   - SIM_SOPT2[PLLFLLSEL]=11

3.2.3 Oscillator electrical specifications

3.2.3.1 Oscillator DC electrical specifications

Table 18. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	600	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	7.5	—	µA	
	• 4 MHz	—	500	—	µA	
	• 8 MHz (RANGE=01)	—	650	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3.25	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					

Table continues on the next page...

Table 18. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
		—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C, Internal capacitance = 20 pf
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.2.3.2 Oscillator frequency specifications

Table 19. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	1, 2
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Proper PC board layout procedures must be followed to achieve specifications.

2. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.2.4 32 kHz oscillator electrical characteristics

3.2.4.1 32 kHz oscillator DC electrical specifications

Table 20. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.2.4.2 32 kHz oscillator frequency specifications

Table 21. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

3.3 Memories and memory interfaces

3.3.1 QuadSPI AC specifications

- All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing diagrams in this section.
- Measurements are with a load of 15pf (1.8V) and 35pf (3V) on output pins. Input slew: 1ns
- Timings assume a setting of 0x0000_000x for QuadSPI _SMPR register (see the reference manual for details).

The following table lists the QuadSPI delay chain read/write settings. Refer the device reference manual for register and bit descriptions.

Table 22. QuadSPI delay chain read/write settings

Mode	QuadSPI registers				Notes
	QuadSPI_MCR[DQS_EN]	QuadSPI_SOCCR[SOCCFG]	QuadSPI_MCR[SCLKCFG]	QuadSPI_FLSHCR[TDH]	
SDR	Yes	3Fh	5	No	Delay of 63 buffer and 64 mux
DDR	Yes	3Fh	1	2	Delay of 63 buffer and 64 mux
Hyperflash	RDS driven from Flash	0h	No	2	Delay of 1 mux

SDR mode

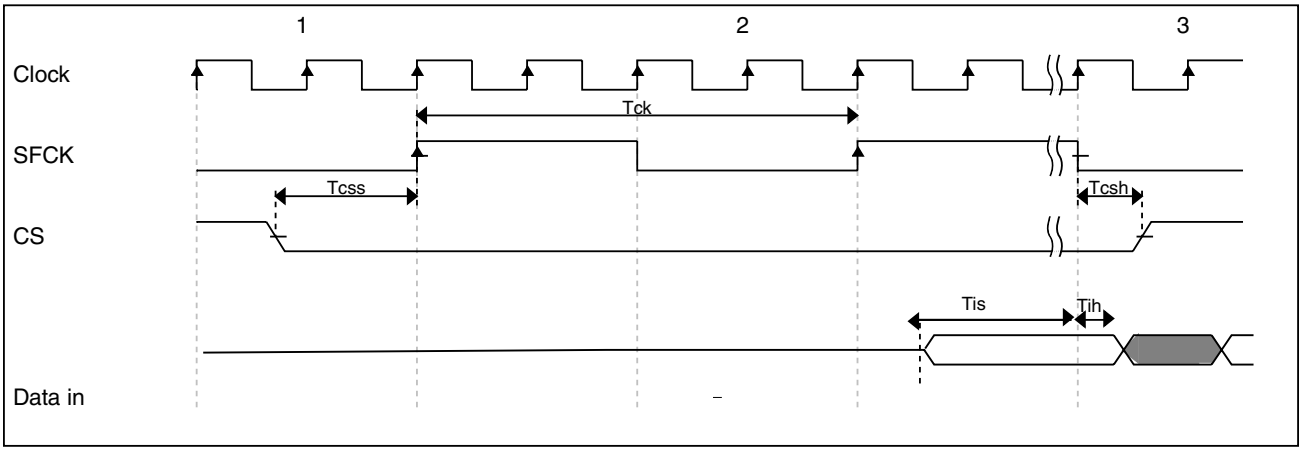


Figure 14. QuadSPI input timing (SDR mode) diagram

NOTE

- The below timing values are with default settings for sampling registers like QuadSPI_SMPR.

- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.
- The below timing are for a load of 15pf (1.8V) and 35pf (3V) or output pads
- All board delays need to be added appropriately
- Input hold time being negative does not have any implication or max achievable frequency

Table 23. QuadSPI input timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	4	-	ns
T_{ih}	Hold time requirement for incoming data	1.5	-	ns

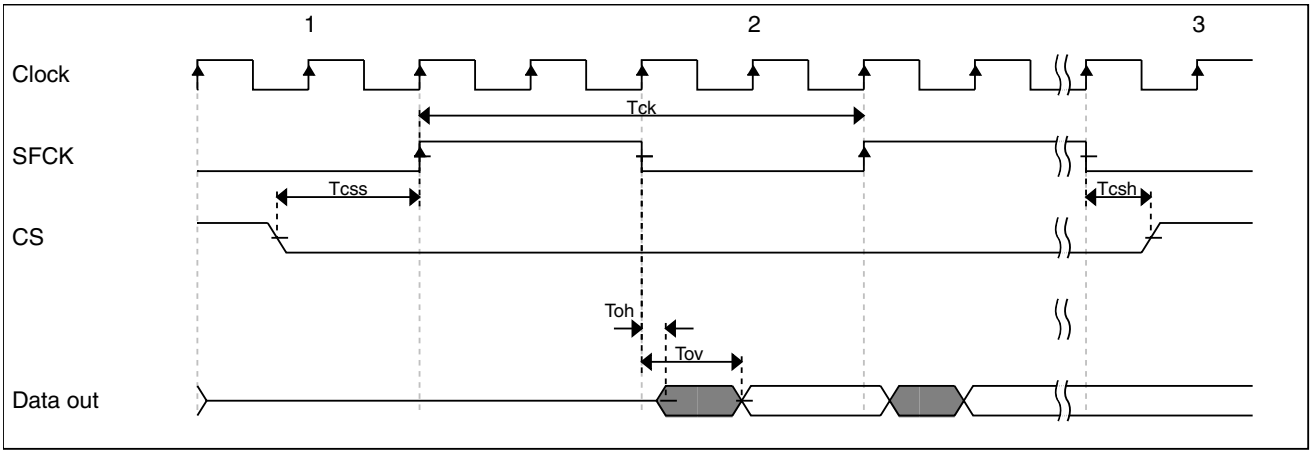


Figure 15. QuadSPI output timing (SDR mode) diagram

Table 24. QuadSPI output timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	-	2.8	ns
T_{oh}	Output Data Hold	-1.4	-	ns
T_{ck}	SCK clock period	-	100	MHz
T_{css}	Chip select output setup time	2	-	ns
T_{csh}	Chip select output hold time	-1	-	ns

NOTE

For any frequency setup and hold specifications of the memory should be met.

DDR Mode

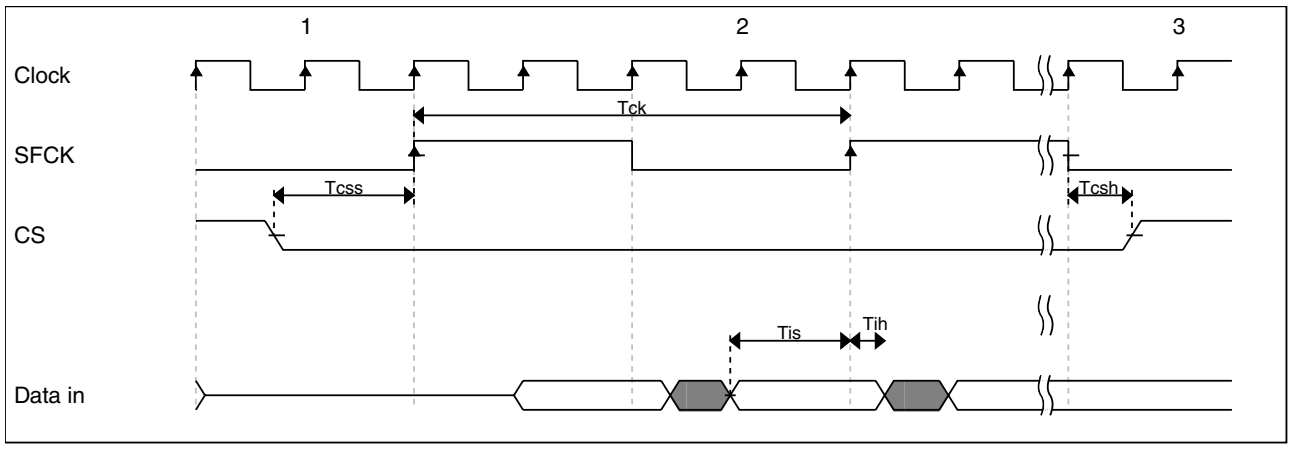


Figure 16. QuadSPI input timing (DDR mode) diagram

NOTE

- Numbers are for a load of 15pf (1.8V) and 35pf (3V)
- The numbers are for setting of hold condition in register QuadSPI_SMPR[DDRSNP]

Table 25. QuadSPI input timing (DDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	4 (Without learning)	-	ns
		1 (With learning)		
T_{ih}	Hold time requirement for incoming data	1.5	-	ns

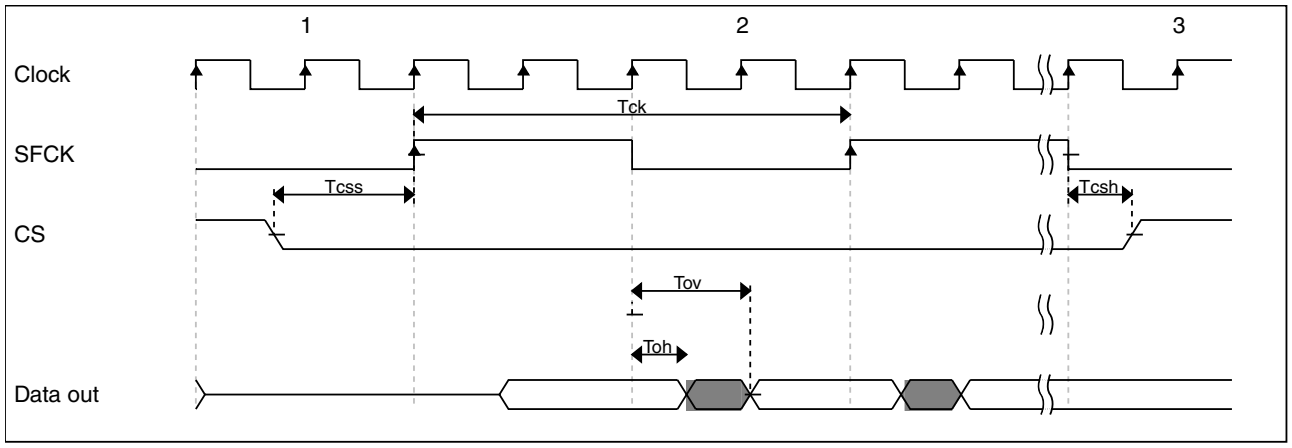


Figure 17. QuadSPI output timing (DDR mode) diagram

Table 26. QuadSPI output timing (DDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	-	4.5	ns
T_{oh}	Output Data Hold	1.5	-	ns
T_{ck}	SCK clock period	-	75 (with learning)	MHz
		-	45 (without learning)	
T_{css}	Chip select output setup time	2	-	Clk(sck)
T_{csh}	Chip select output hold time	-1	-	Clk(sck)

Hyperflash mode

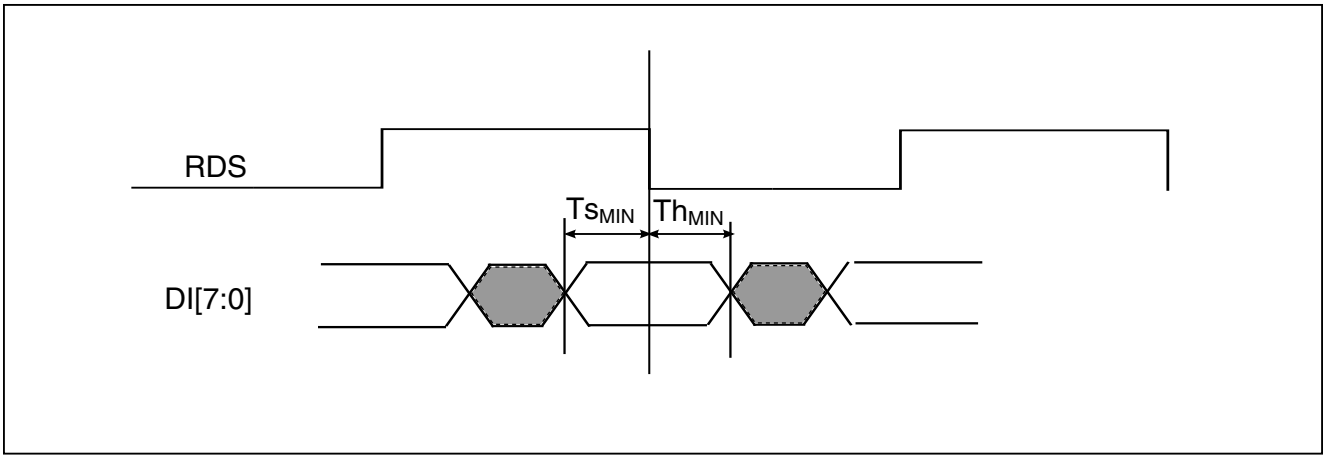


Figure 18. QuadSPI input timing (Hyperflash mode) diagram

Table 27. QuadSPI input timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Ts_{MIN}	Setup time for incoming data	2	-	ns
Th_{MIN}	Hold time requirement for incoming data	2	-	ns

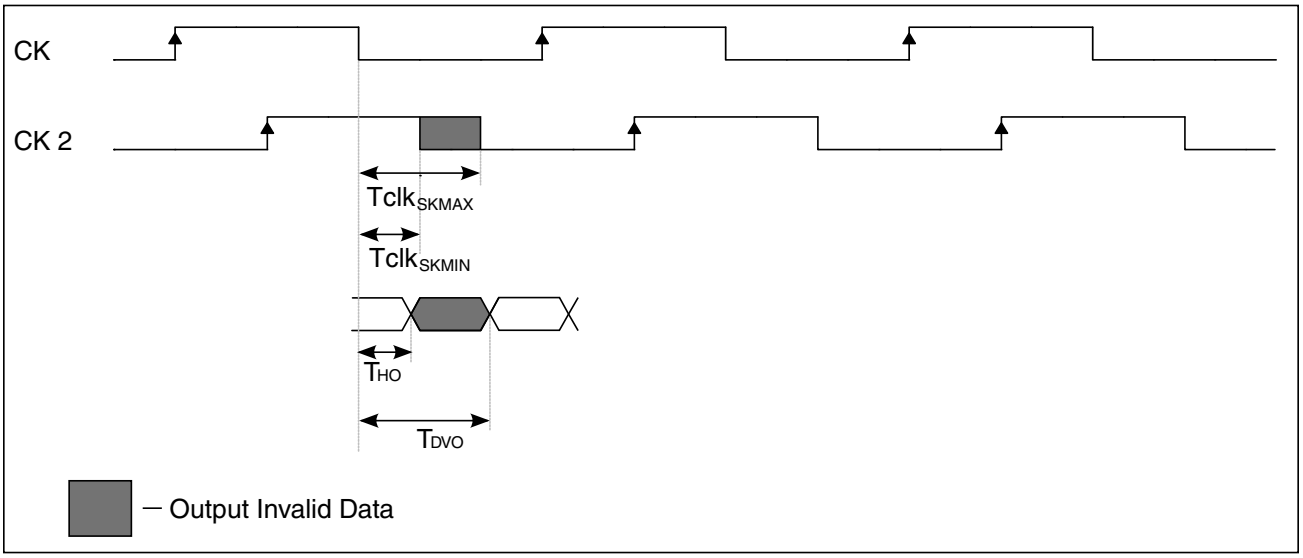


Figure 19. QuadSPI output timing (Hyperflash mode) diagram

Table 28. QuadSPI output timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Tdv_{MAX}	Output Data Valid	-	4.3	ns
Tho	Output Data Hold	1.3	-	ns
$Tclk_{SKMAX}$	Ck to Ck2 skew max	-	T/4 + 0.5	ns
$Tclk_{SKMIN}$	Ck to Ck2 skew min	T/4 - 0.5	-	ns

NOTE

Maximum clock frequency = 75 MHz.

3.3.2 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.3.2.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 29. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—

Table continues on the next page...

Table 29. NVM program/erase timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	208	1808	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.3.2.2 Flash timing specifications — commands

Table 30. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec4k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	100	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	280	2100	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.3.2.3 Flash high voltage current behaviors

Table 31. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.3.2.4 Reliability specifications

Table 32. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—

Table continues on the next page...

Table 32. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ °C.

3.3.3 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 33. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	11.8	ns	
FB3	Address, data, and control output hold	1.0	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	6	—	ns	
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0.0	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BE}}$/BWE*n*, $\overline{\text{FB\_CS}}$*n*, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$,$\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

Table 34. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	12.6	ns	

Table continues on the next page...

Table 34. Flexbus full voltage range switching specifications (continued)

Num	Description	Min.	Max.	Unit	Notes
FB3	Address, data, and control output hold	1.0	—	ns	1
FB4	Data and FB_TA input setup	12.5	—	ns	
FB5	Data and FB_TA input hold	0	—	ns	2

1. Specification is valid for all FB_AD[31:0], FB_BE/BWE*n*, FB_CS*n*, FB_OE, FB_R/W,FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and FB_TA.

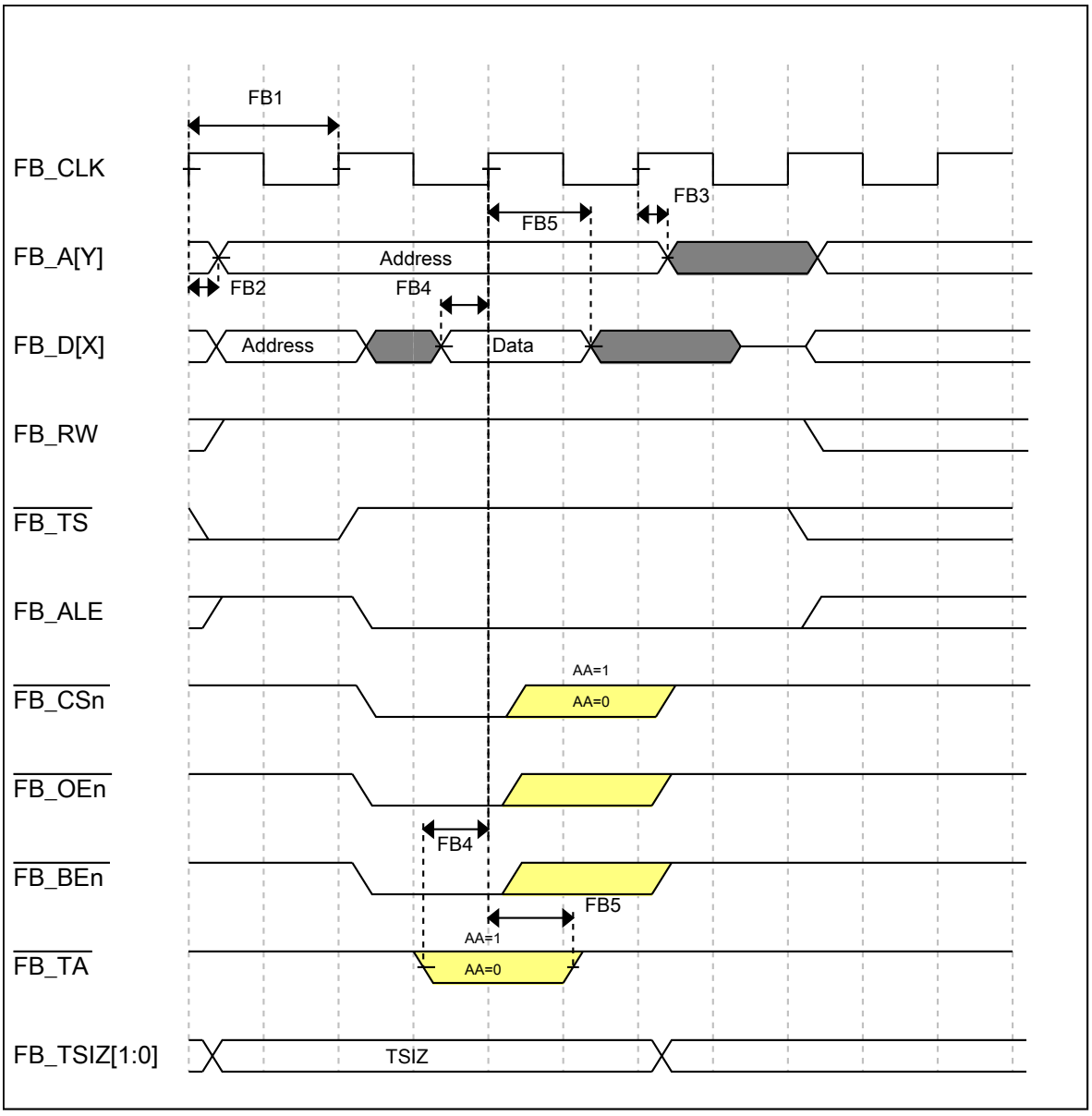


Figure 20. FlexBus read timing diagram

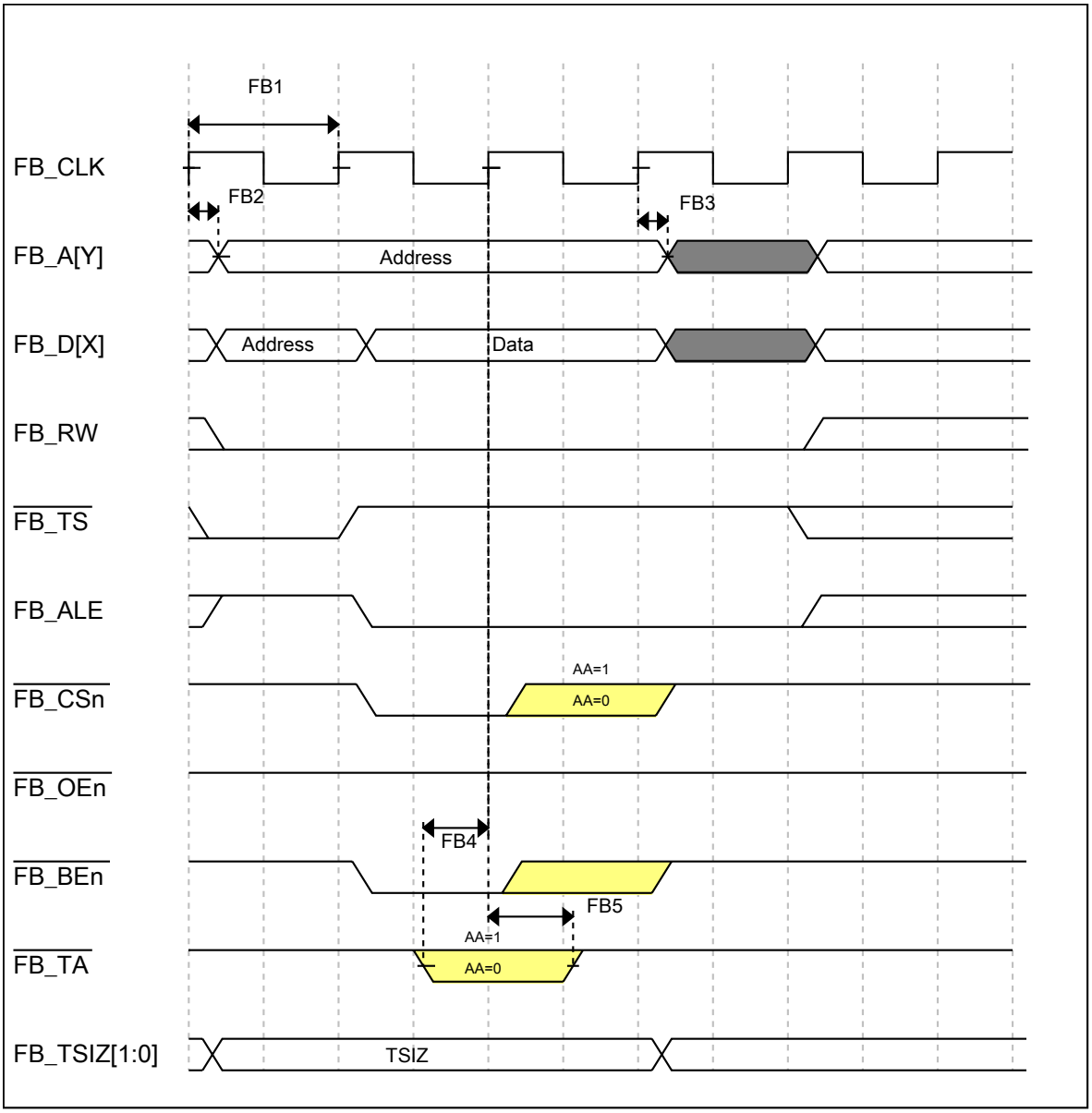
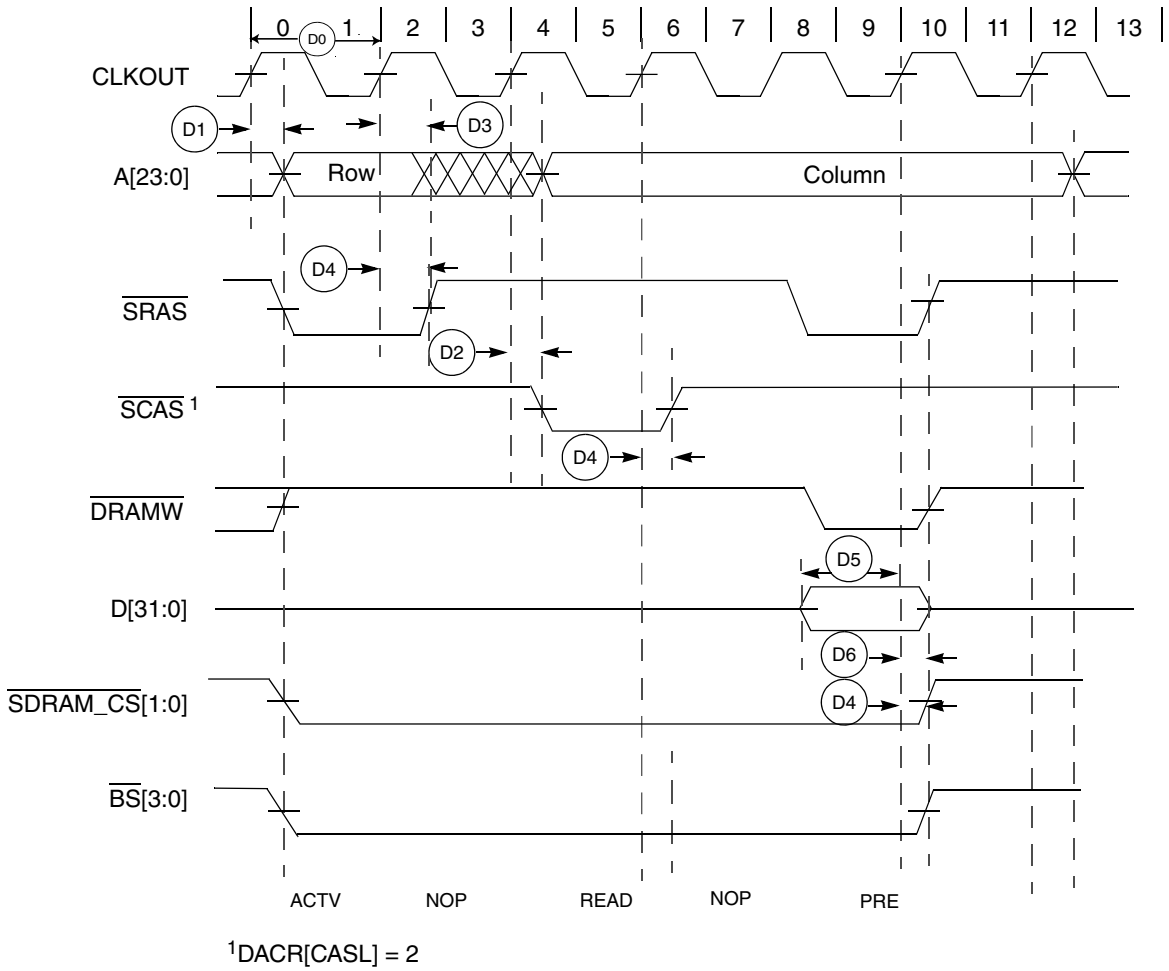


Figure 21. FlexBus write timing diagram

3.3.4 SDRAM controller specifications

Following figure shows SDRAM read cycle.



[1]DACR[CASL] = 2

Figure 22. SDRAM read timing diagram

Table 35. SDRAM Timing (Full voltage range)

NUM	Characteristic [1]	Symbol	Mln	Max	Unit
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	CLKOUT	MHz	
D0	Clock period	1/CLKOUT	—	ns	2
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	-	11.2	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}		11.1	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.0	-	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.0	-	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	12.0	-	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.0	-	ns
D7[3]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	-	12.0	ns
D8[3]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.0	-	ns

1. All timing specifications are based on taking into account, a 25pF load on the SDRAM output pins.
2. CLKOUT is same as FB_CLK, maximum frequency can be 75 MHz

3. D7 and D8 are for write cycles only.

Table 36. SDRAM Timing (Limited voltage range)

NUM	Characteristic [1]	Symbol	Mln	Max	Unit
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	CLKOUT	MHz	
D0	Clock period	1/CLKOUT	—	ns	2
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	-	11.1	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}		11.1	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.0	-	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.0	-	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	7.3	-	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.0	-	ns
D7[3]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	-	11.1	ns
D8[3]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.0	-	ns

1. All timing specifications are based on taking into account, a 25pF load on the SDRAM output pins.
2. CLKOUT is same as FB_CLK, maximum frequency can be 75 MHz
3. D7 and D8 are for write cycles only.

Following figure shows an SDRAM write cycle.

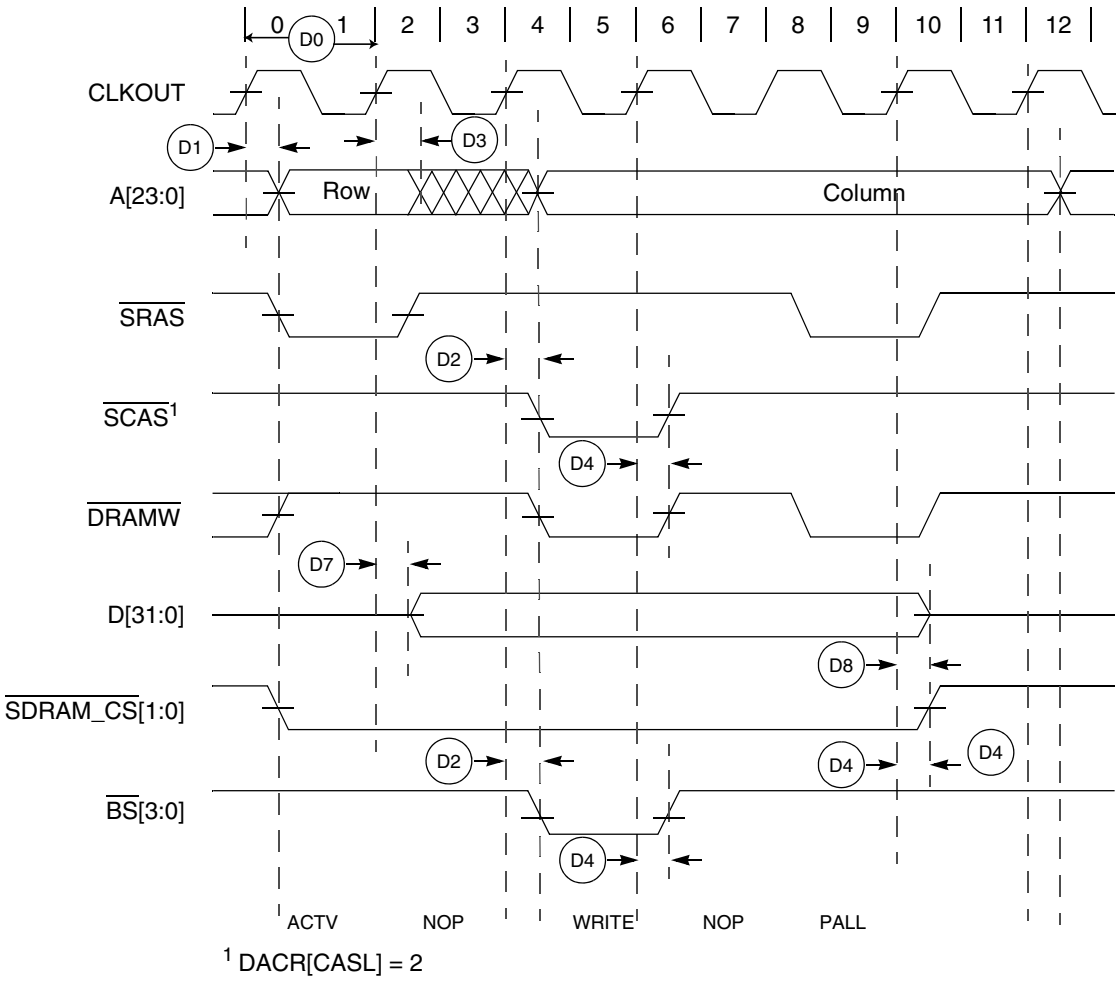


Figure 23. SDRAM write timing diagram

3.4 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.5 Analog

3.5.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 37 and Table 38 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.5.1.1 ADC operating conditions

Table 37. ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 × VREFH VREFH	V	
C_{ADIN}	Input capacitance	• 8-bit / 10-bit / 12-bit modes	—	4	5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

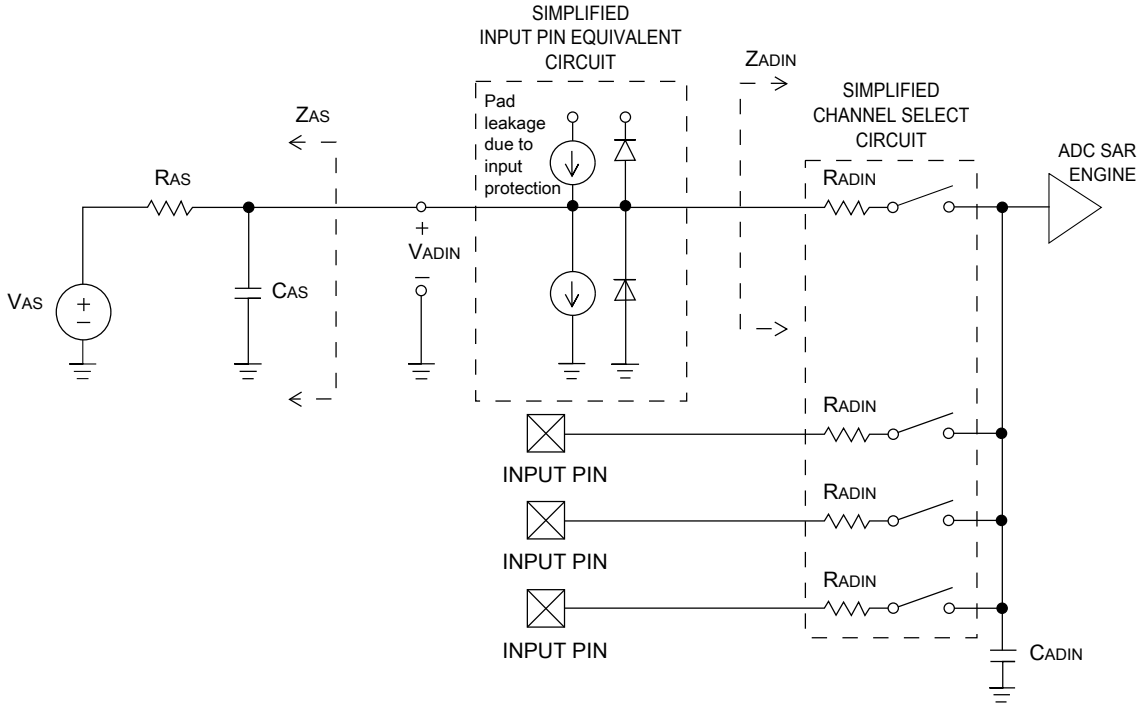


Figure 24. ADC input impedance equivalency diagram

3.5.1.2 ADC electrical characteristics

Table 38. ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t_{ADACK} = 1/ f_{ADACK}
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes	—	±4	±6.8	LSB[4]	5
		• <12-bit modes	—	±1.4	±2.1		
DNL	Differential non-linearity	• 12-bit modes	—	±0.7	–1.1 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.2	–0.3 to 0.5		
INL	Integral non-linearity	• 12-bit modes	—	±1.0	–2.7 to +1.9	LSB[4]	5

Table continues on the next page...

Table 38. ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• <12-bit modes	—	±0.5	–0.7 to +0.5		
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• ≤13-bit modes	—	—	±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	82 78	95 90	— —	dB dB	7
E_{IL}	Input leakage error		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = (V_{REFH} - V_{REFL})/2^N
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.

8. ADC conversion clock < 3 MHz

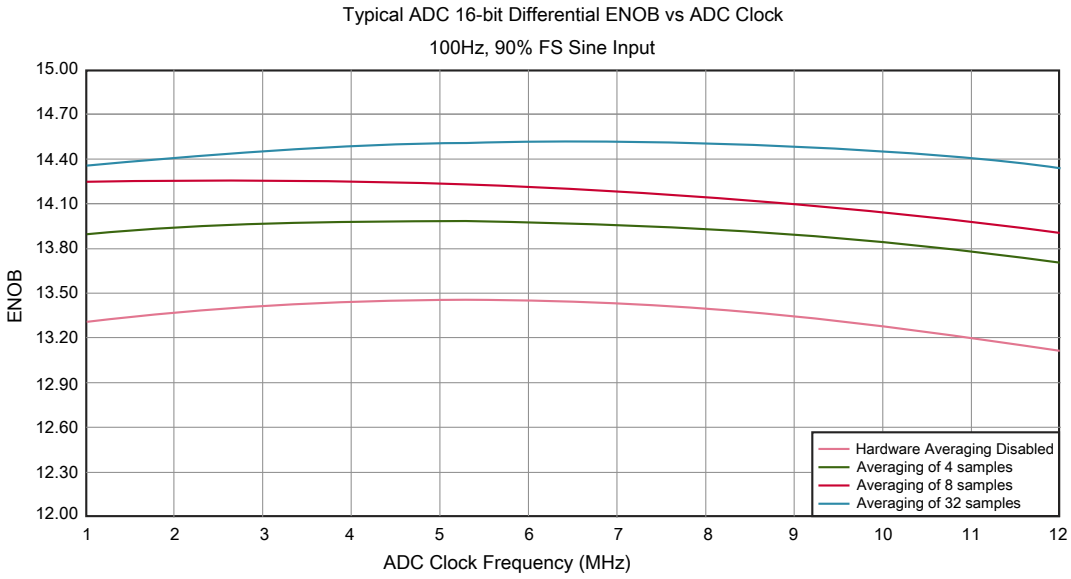


Figure 25. Typical ENOB vs. ADC_CLK for 16-bit differential mode

3.5.2 CMP and 6-bit DAC electrical specifications

Table 39. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA

Table continues on the next page...

Table 39. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

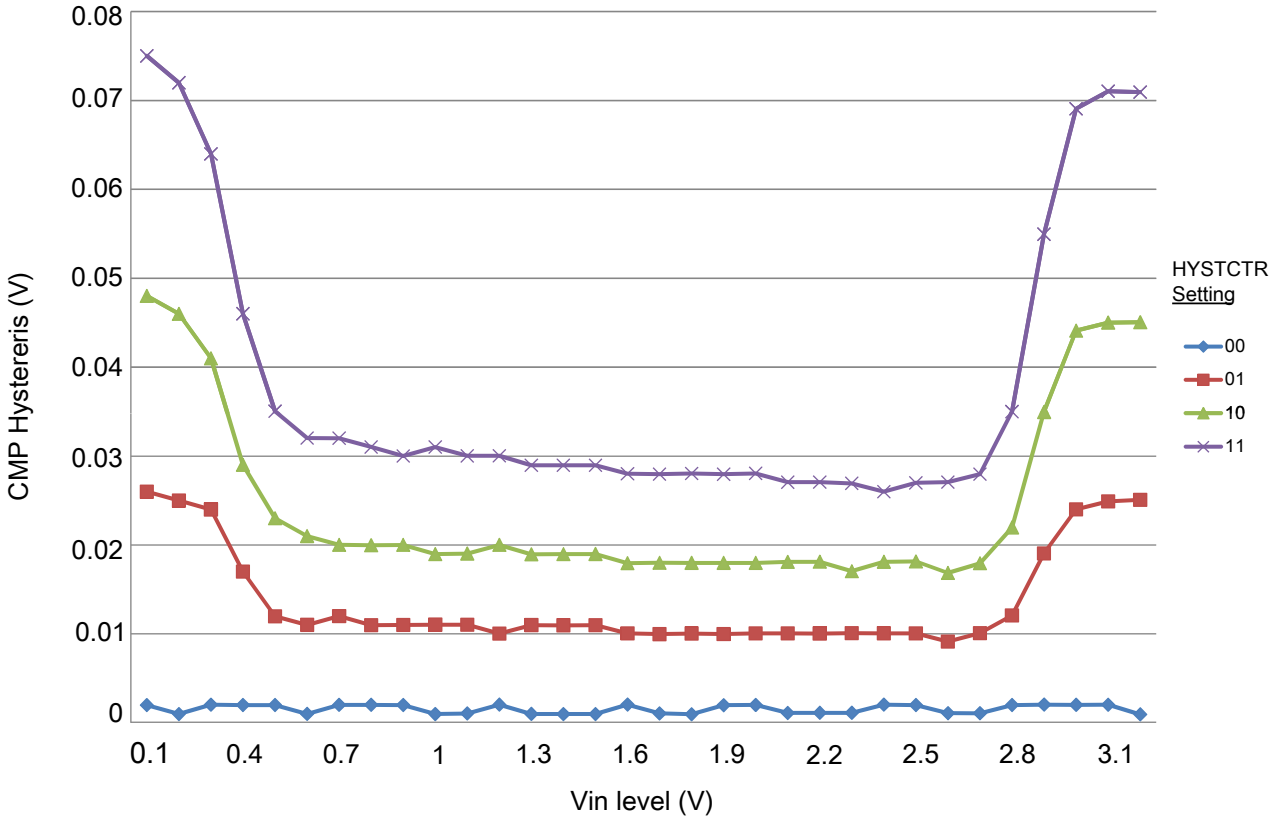


Figure 26. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

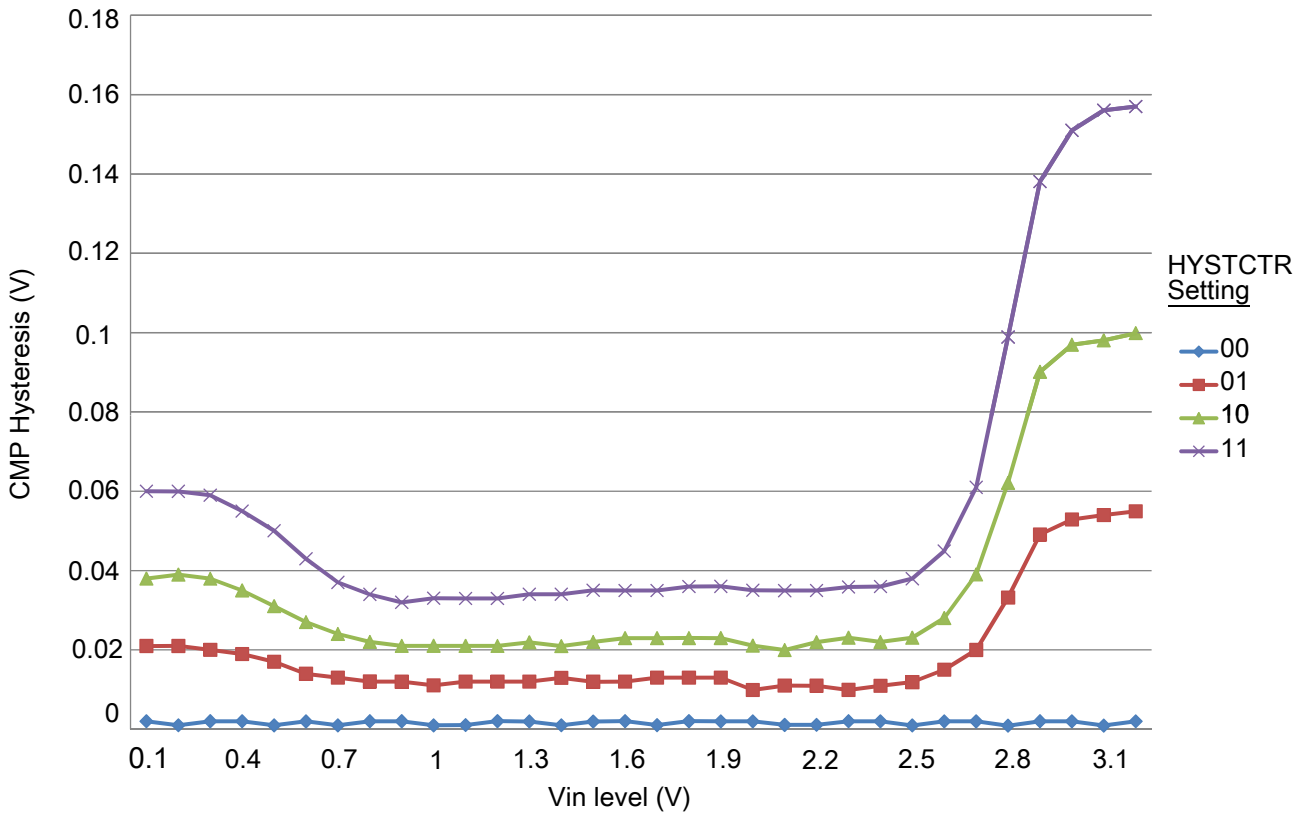


Figure 27. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.5.3 12-bit DAC electrical characteristics

3.5.3.1 12-bit DAC operating requirements

Table 40. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.5.3.2 12-bit DAC operating behaviors

Table 41. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
A_C	Offset aging coefficient	—	—	100	µV/yr	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	• High power (SP_{HP})	1.2	1.7	—		
	• Low power (SP_{LP})	0.05	0.12	—		
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth				kHz	
	• High power (SP_{HP})	550	—	—		
	• Low power (SP_{LP})	40	—	—		

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV

6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

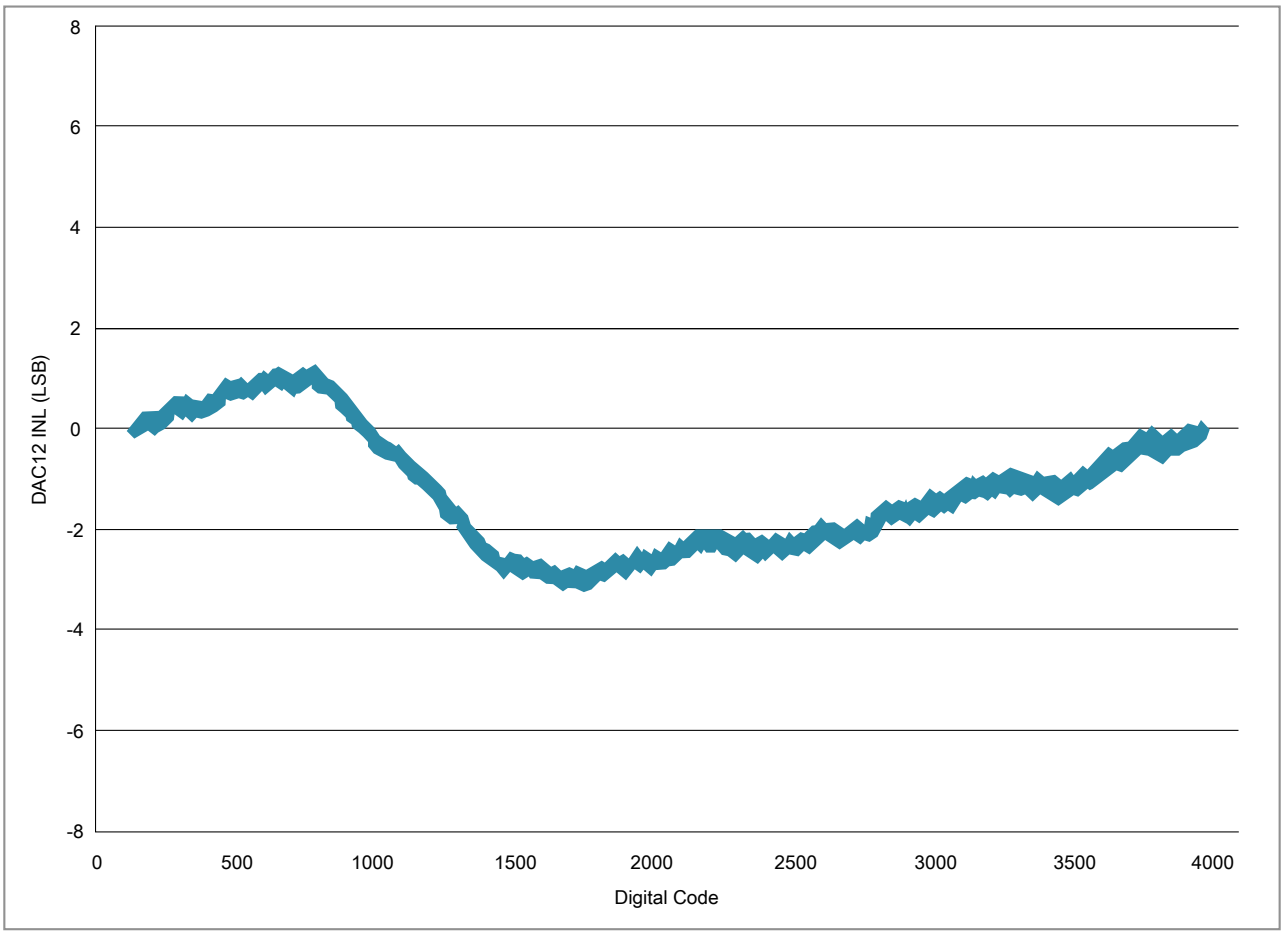


Figure 28. Typical INL error vs. digital code

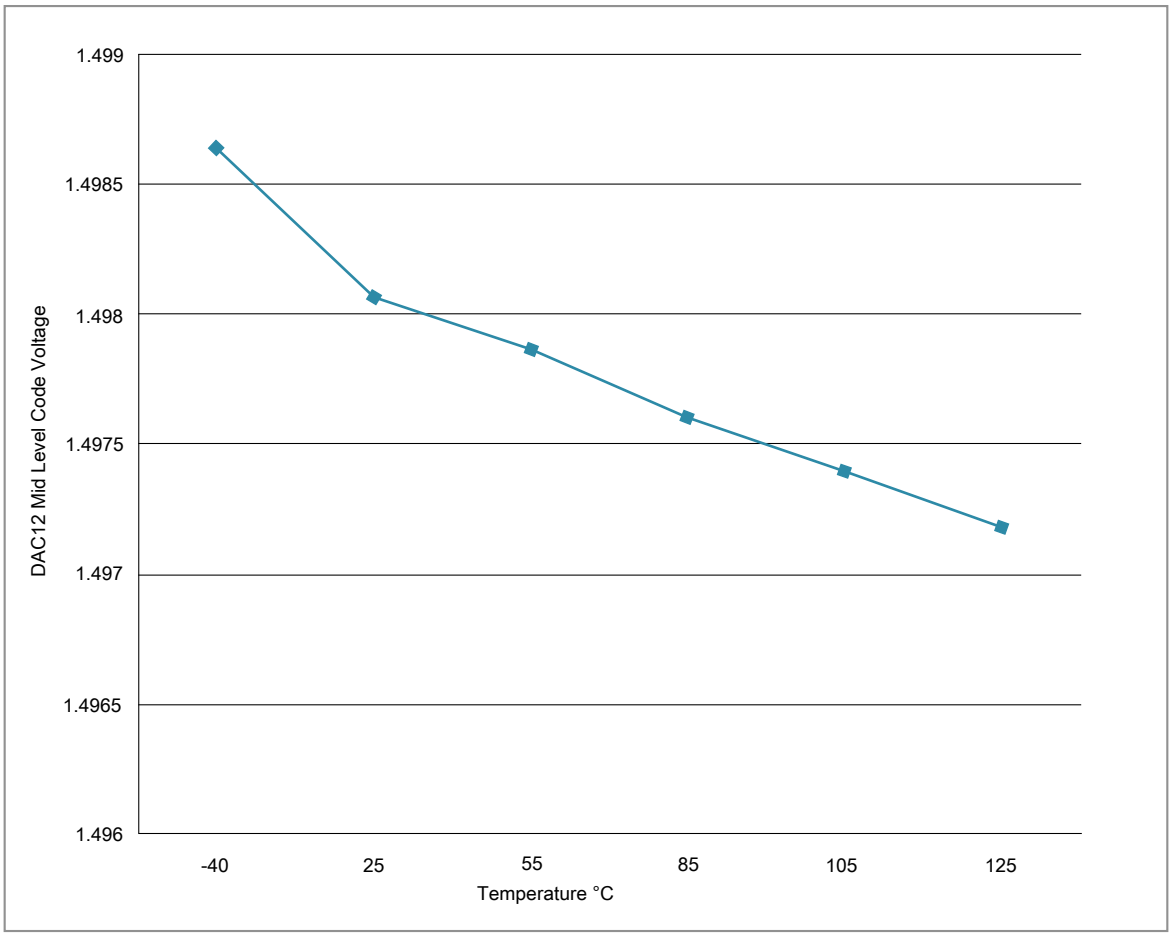


Figure 29. Offset at half scale vs. temperature

3.5.4 Voltage reference electrical specifications

Table 42. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 43. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	1
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	80	mV	1
I_{bg}	Bandgap only current	—	—	80	µA	1
I_{lp}	Low-power buffer current	—	—	360	uA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	µV	1, 2
T_{stup}	Buffer startup time	—	—	100	µs	
$T_{chop\_osc\_stup}$	Internal bandgap start-up delay with chop oscillator enabled	—	—	35	ms	—
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 44. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 45. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

3.6 Timers

See General switching specifications.

3.7 Communication interfaces

3.7.1 EMV SIM specifications

Each EMV SIM module interface consists of a total of five pins.

The interface is designed to be used with synchronous Smart cards, meaning the EMV SIM module provides the clock used by the Smart card. The clock frequency is typically 372 times the Tx/Rx data rate; however, the EMV SIM module can also work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the EMV SIM module provides to the Smart card is used by the Smart card to recover the clock from the data in the same manner as standard UART data exchanges. All five signals of the EMV SIM module are asynchronous with each other.

There are no required timing relationships between signals in normal mode. The smart card is initiated by the interface device; the Smart card responds with Answer to Reset. Although the EMV SIM interface has no defined requirements, the ISO/IEC 7816 defines reset and power-down sequences (for detailed information see ISO/IEC 7816).

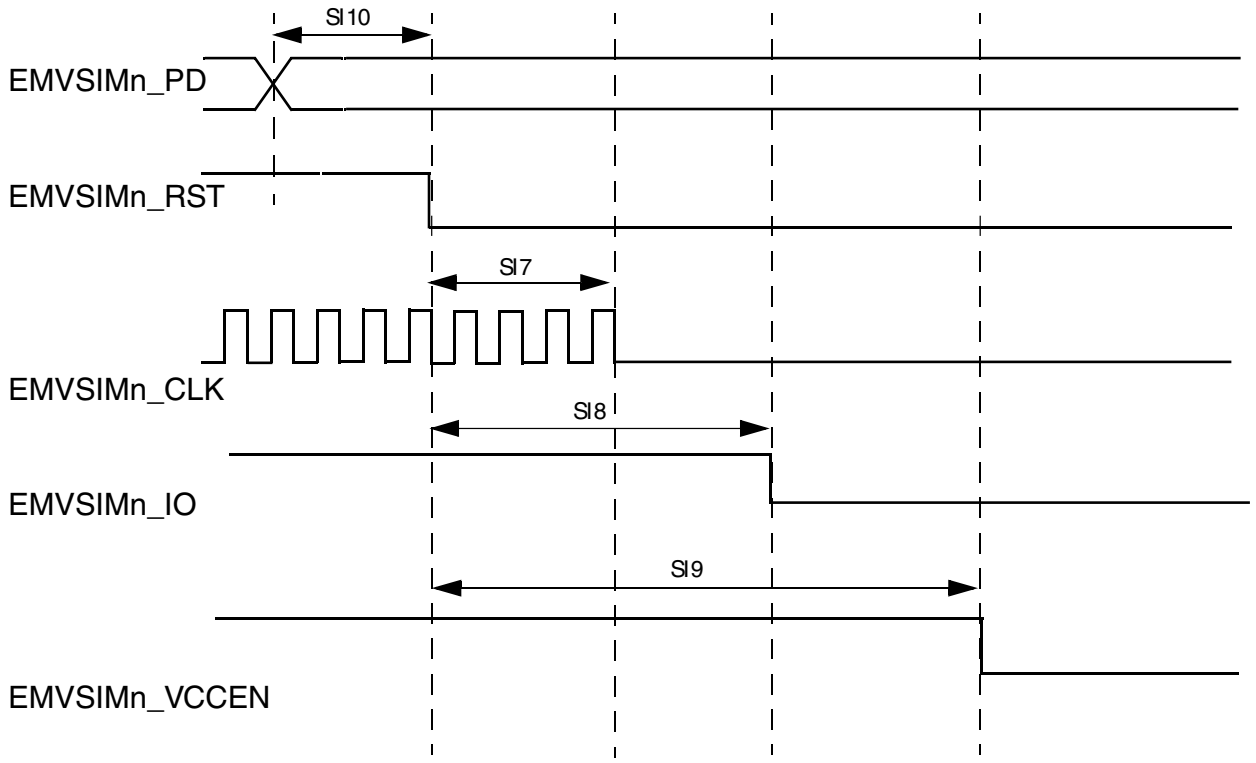


Figure 30. EMV SIM Clock Timing Diagram

The following table defines the general timing requirements for the EMV SIM interface.

Table 46. Timing Specifications, High Drive Strength

ID	Parameter	Symbol	Min	Max	Unit
SI 1	EMV SIM clock frequency (EMVSIMn_CLK)[1]	S_{freq}	1	5	MHz
SI 2	EMV SIM clock rise time (EMVSIMn_CLK)[2]	S_{rise}	—	0.09 × (1/Sfreq)	ns
SI 3	EMV SIM clock fall time (EMVSIMn_CLK)[2]	S_{fall}	—	0.09 × (1/Sfreq)	ns
SI 4	EMV SIM input transition time (EMVSIMn_IO, EMVSIMn_PD)	S_{tran}	20	25	ns
Si 5	EMV SIM I/O rise time / fall time (EMVSIMn_IO)[3]	Tr/Tf	—	1	ns
Si 6	EMV SIM RST rise time / fall time (EMVSIMn_RST)[4]	Tr/Tf	—	1	ns

1. 50% duty cycle clock,
2. With C = 50 pF
3. With Cin = 30 pF, Cout = 30 pF,
4. With Cin = 30 pF,

3.7.1.1 EMV SIM Reset Sequences

Smart cards may have internal reset, or active low reset. The following subset describes the reset sequences in these two cases.

3.7.1.1.1 Smart Cards with Internal Reset

Following figure shows the reset sequence for Smart cards with internal reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- The card must send a response on EMVSIMn_IO acknowledging the reset between 400–40000 clock cycles after T0.

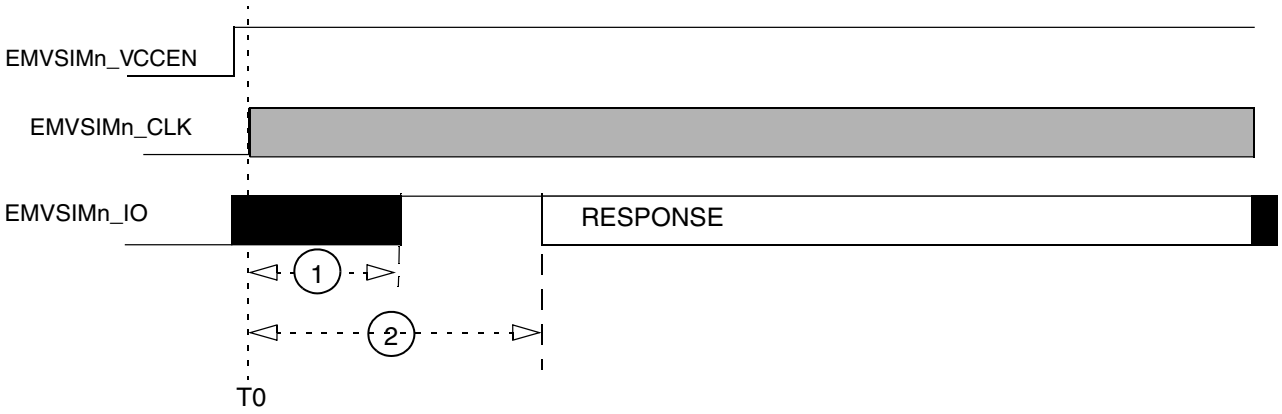


Figure 31. Internal Reset Card Reset Sequence

The following table defines the general timing requirements for the SIM interface.

Table 47. Timing Specifications, Internal Reset Card Reset Sequence

Ref	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles

3.7.1.1.2 Smart Cards with Active Low Reset

Following figure shows the reset sequence for Smart cards with active low reset. The reset sequence comprises the following steps::

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- EMVSIMn_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
- EMVSIMn_RST is asserted (at time T1)
- EMVSIMn_RST must remain asserted for at least 40,000 clock cycles after T1, and a response must be received on EMVSIMn_IO between 400 and 40,000 clock cycles after T1.

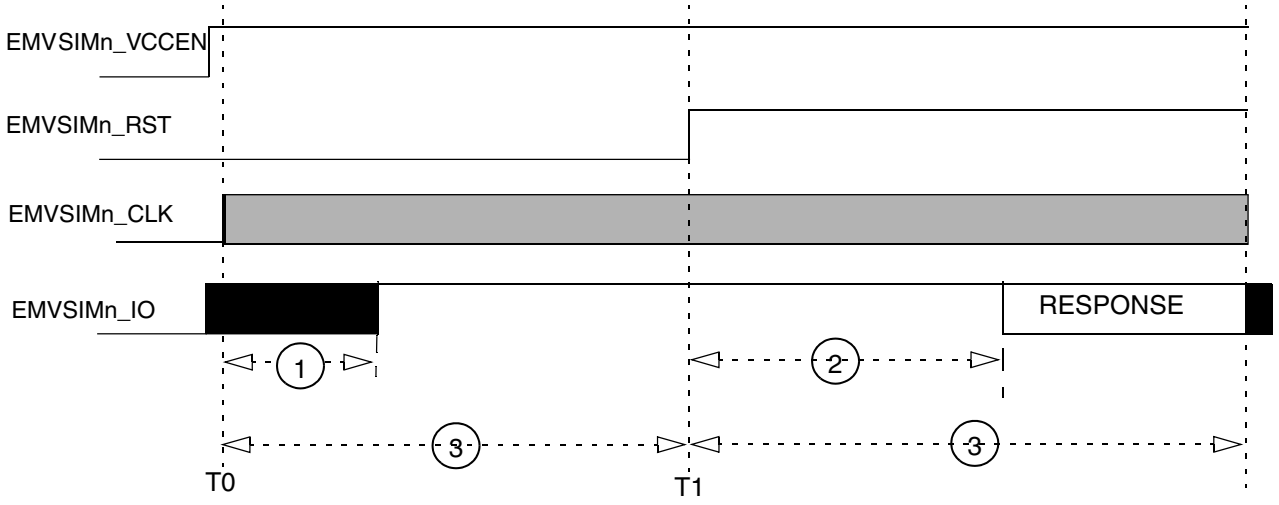


Figure 32. Active-Low-Reset Smart Card Reset Sequence

The following table defines the general timing requirements for the EMVSIM interface..

Table 48. Timing Specifications, Internal Reset Card Reset Sequence

Ref No	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles
3	40,000	—	EMVSIMx_CLK clock cycles

3.7.1.2 EMVSIM Power-Down Sequence

Following figure shows the EMV SIM interface power-down AC timing diagram.Table 49 table shows the timing requirements for parameters (SI7–SI10) shown in the figure. The power-down sequence for the EMV SIM interface is as follows:

- EMVSIMn_SIMPD port detects the removal of the Smart Card
- EMVSIMn_RST is negated
- EMVSIMn_CLK is negated
- EMVSIM_IO is negated
- EMVSIMx_VCCENy is negated

Each of the above steps requires one Frtcclk period (usually 32 kHz and selected by SIM_SOPT1[OSC32KSEL]). Power-down may be initiated by a Smart card removal detection; or it may be launched by the processor.

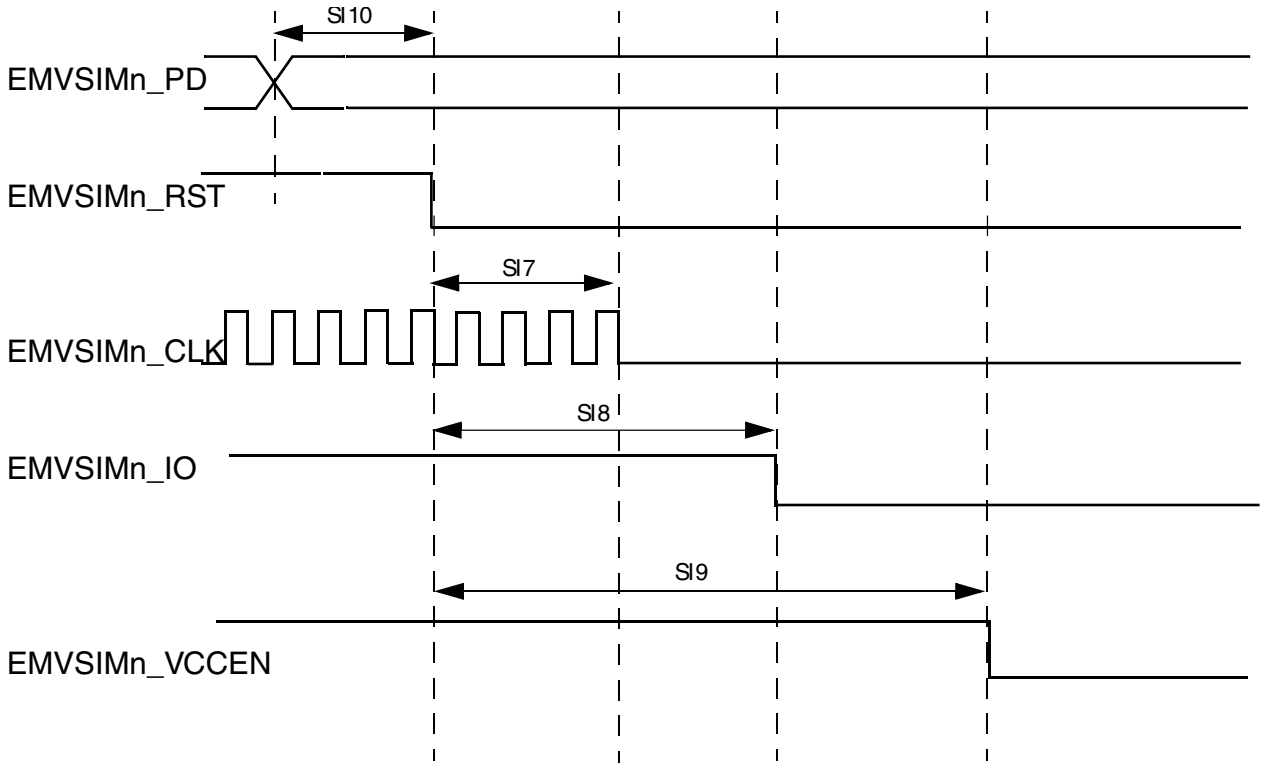


Figure 33. Smart Card Interface Power Down AC Timing

Table 49. Timing Requirements for Power-down Sequence

Ref No	Parameter	Symbol	Min	Max	Units
SI7	EMVSIM reset to SIM clock stop	$S_{rst2clk}$	0.9 × 1/ Frtcclk[1]	1.1 × 1/Frtcclk	µs
SI8	EMVSIM reset to SIM Tx data low	$S_{rst2dat}$	1.8 × 1/ Frtcclk	2.2 × 1/Frtcclk	µs
SI9	EMVSIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 × 1/ Frtcclk	3.3 × 1/Frtcclk	µs
SI10	EMVSIM presence detect to SIM reset low	S_{pd2rst}	0.9 × 1/ Frtcclk	1.1 × 1/Frtcclk	µs

1. Frtcclk is ERCLK32K, and this clock must be enabled during the power down sequence.

NOTE

Same timing is also followed when auto power down is initiated. See Reference Manual for reference.

3.7.2 USB VREG electrical specifications

Table 50. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	— —	650 —	— 4	nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

3.7.3 USB DCD electrical specifications

Table 51. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}, V_{DM_SRC}	USB_DP and USB_DM source voltages (up to 250 µA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	µA
I_{DM_SINK}, I_{DP_SINK}	USB_DM and USB_DP sink currents	50	100	150	µA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

3.7.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 52. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	15.0	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	1.0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15.8	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

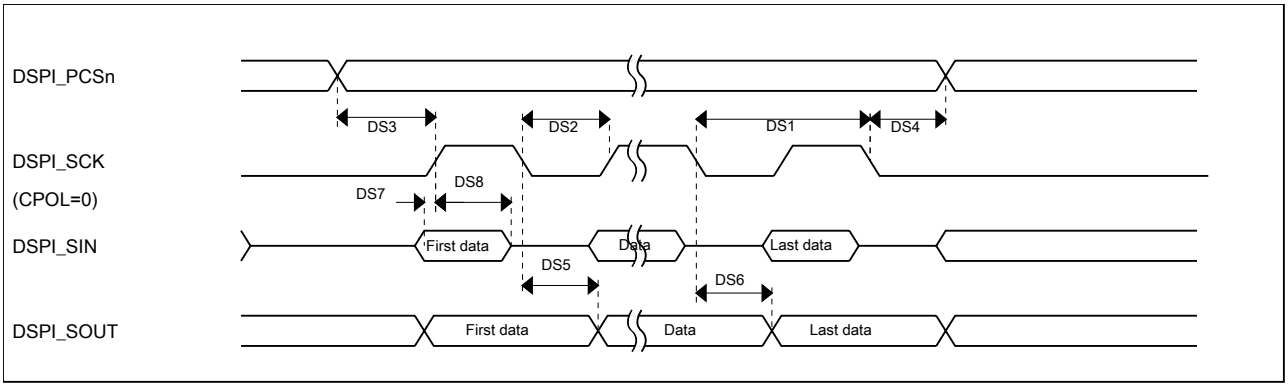


Figure 34. DSPI classic SPI timing — master mode

Table 53. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		15 [1]	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	23.0	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.7	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	13	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	13	ns

1. The maximum operating frequency is measured with non-continuous CS and SCK. When DSPI is configured with continuous CS and SCK, there is a constraint that SPI clock should not be greater than 1/6 of bus clock, for example, when bus clock is 60MHz, SPI clock should not be greater than 10MHz.

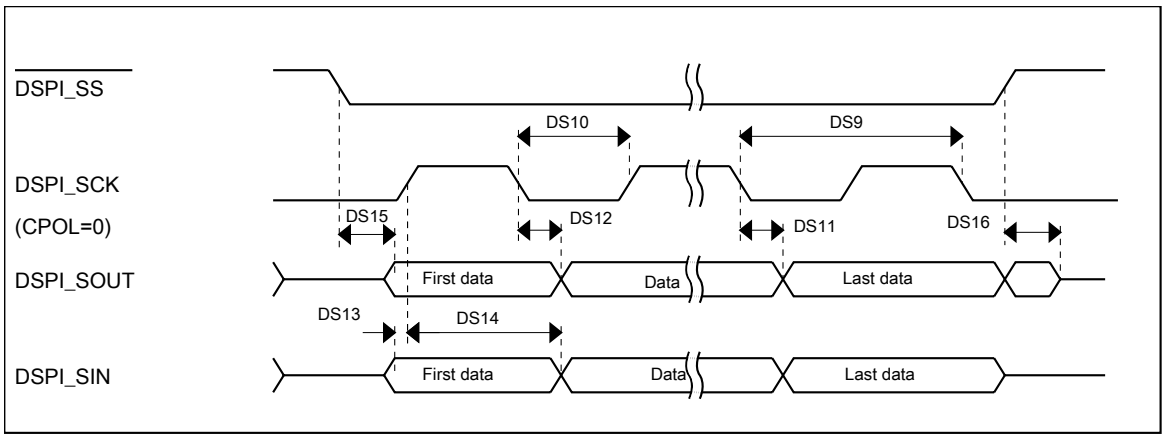


Figure 35. DSPI classic SPI timing — slave mode

3.7.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 54. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	15	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	16	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	1.0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	19.1	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

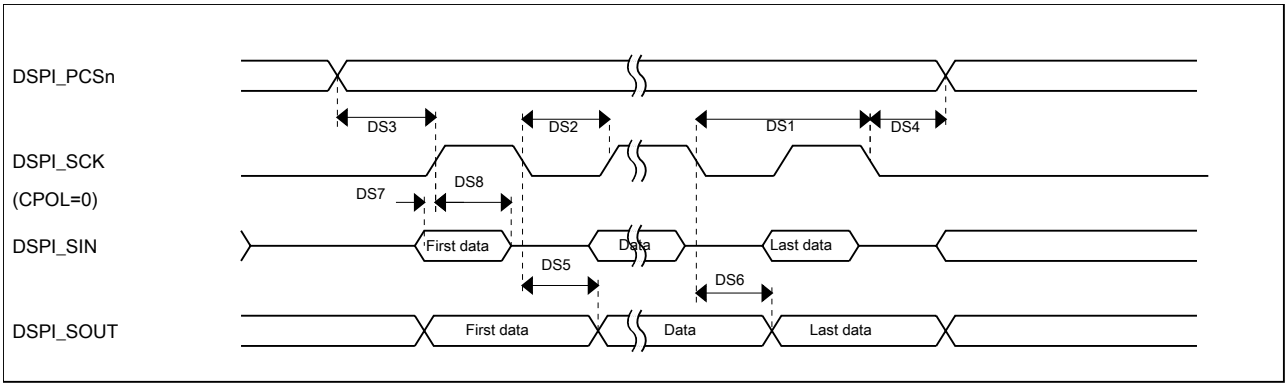


Figure 36. DSPI classic SPI timing — master mode

Table 55. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Table continues on the next page...

Table 55. Slave mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	23.1	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	13.0	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	13.0	ns

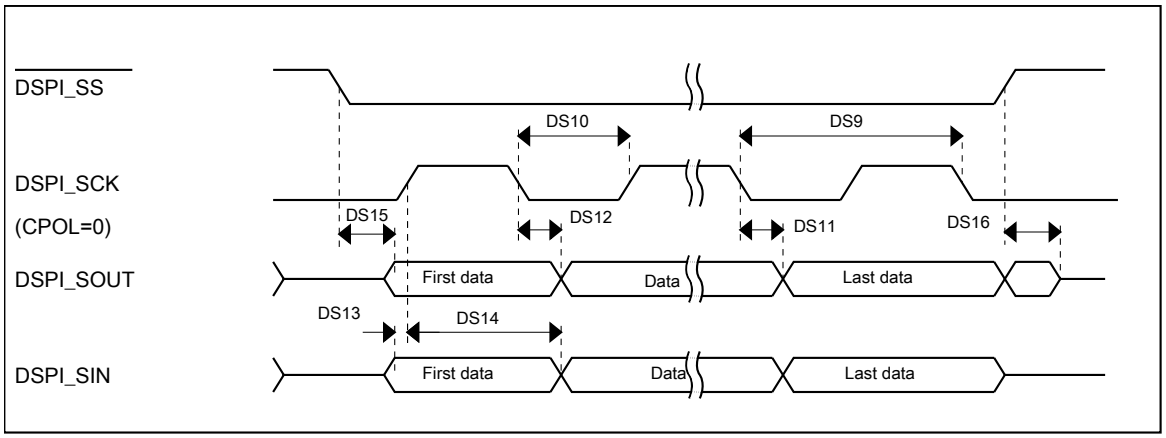


Figure 37. DSPI classic SPI timing — slave mode

3.7.6 I²C switching specifications

See General switching specifications.

3.7.7 UART switching specifications

See General switching specifications.

3.7.8 LPUART switching specifications

See General switching specifications.

3.7.9 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 56. SDHC full voltage range switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	1.71	3.6	V
	Card input clock				
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25/45	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	25/45	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	0	8.1	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

Table 57. SDHC limited voltage range switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	2.7	3.6	V
	Card input clock				
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	0	7	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				

Table continues on the next page...

Table 57. SDHC limited voltage range switching specifications (continued)

Num	Symbol	Description	Min.	Max.	Unit
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

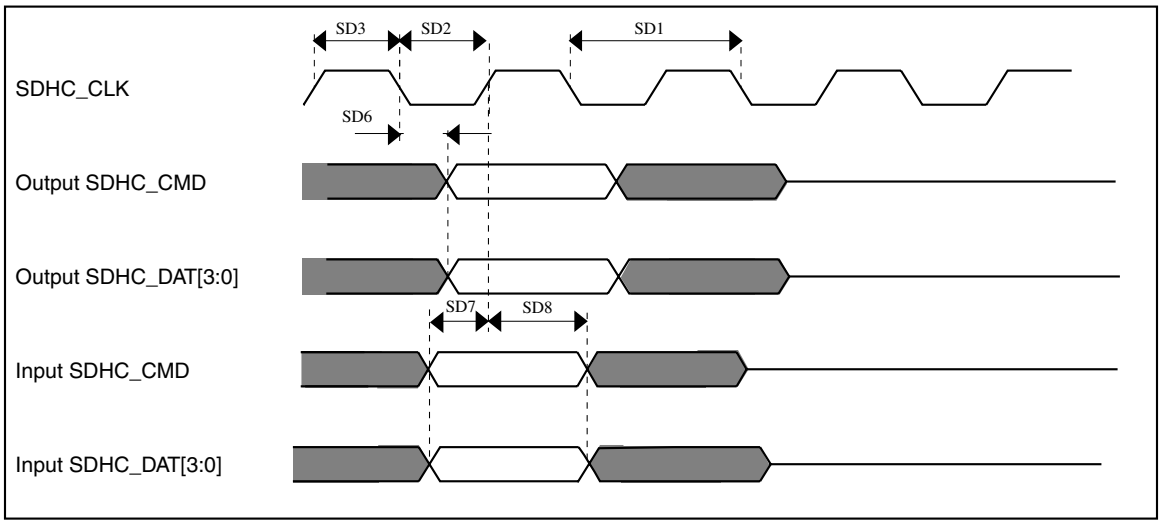


Figure 38. SDHC timing

3.7.10 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 58. I2S master mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	80	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	0	—	ns

Table continues on the next page...

Table 58. I2S master mode timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	15	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

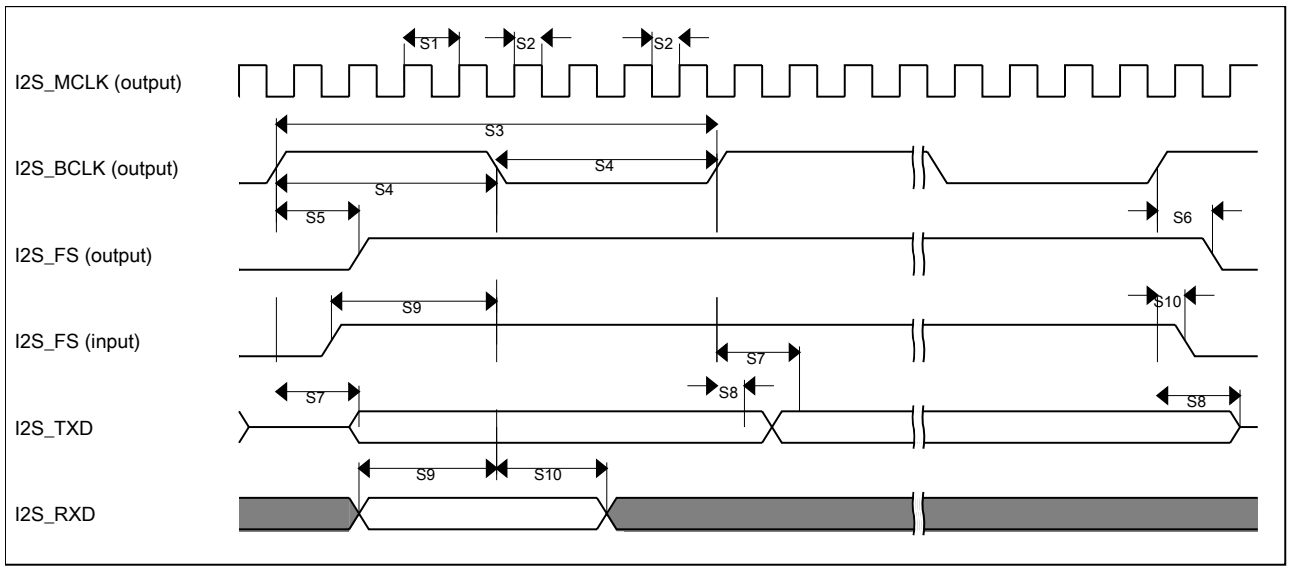


Figure 39. I²S timing — master mode

Table 59. I2S slave mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_BCLK cycle time (input)	80	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	4.5	—	ns
S14	I2S_FS input hold after I2S_BCLK	2	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	20	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]		25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

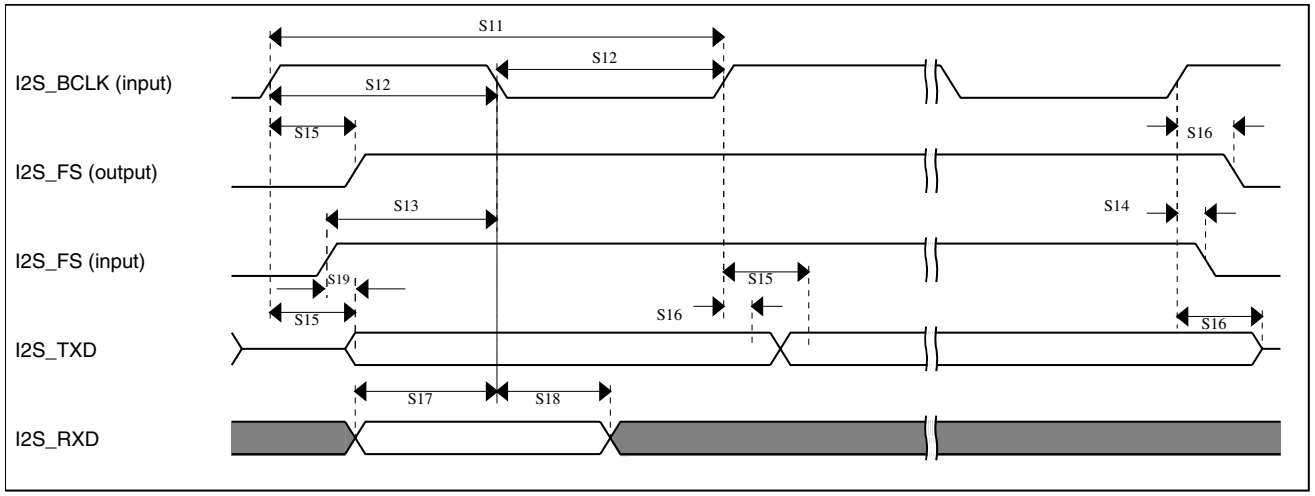


Figure 40. I²S timing — slave modes

3.7.10.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 60. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	15	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

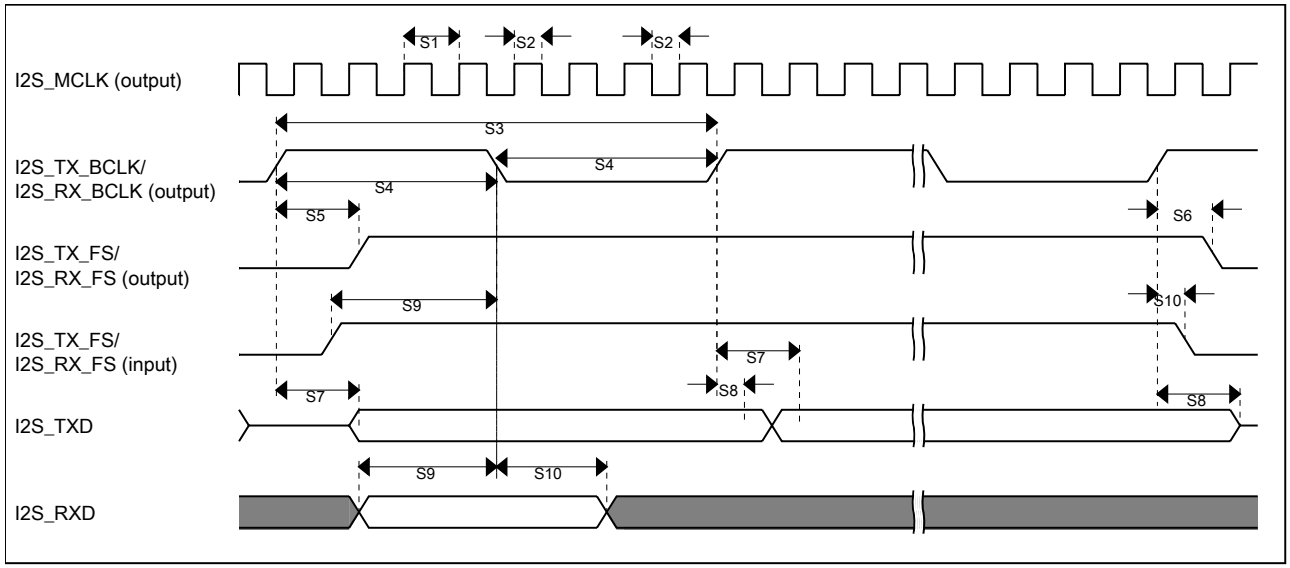


Figure 41. I2S/SAI timing — master modes

Table 61. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	4.5	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	23.1	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

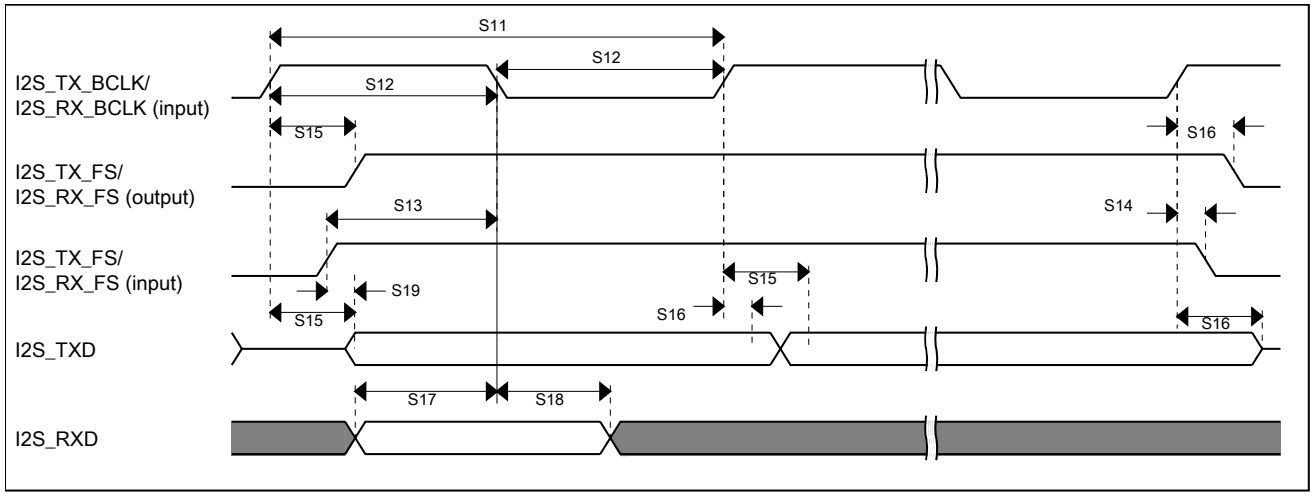


Figure 42. I2S/SAI timing — slave modes

3.7.10.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 62. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

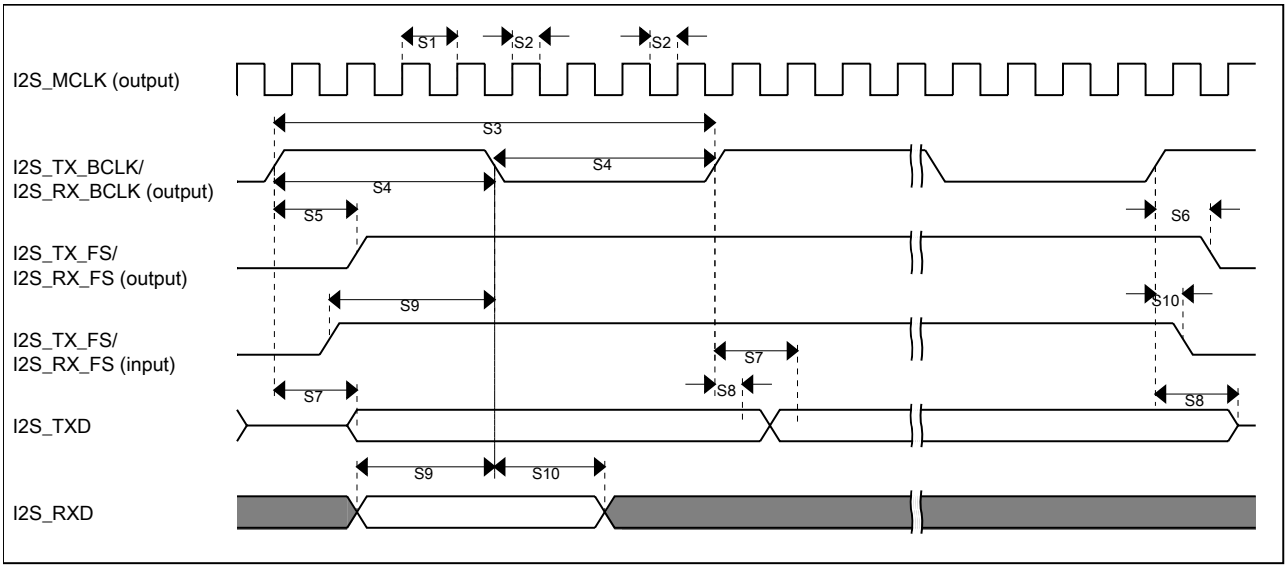


Figure 43. I2S/SAI timing — master modes

Table 63. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	5	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	56.5	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	5	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

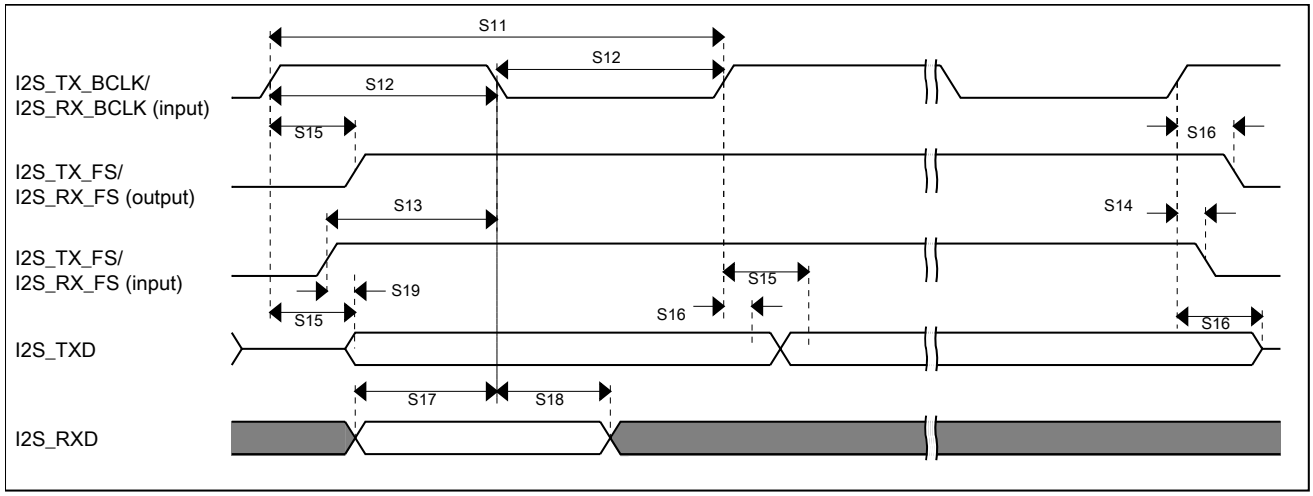


Figure 44. I2S/SAI timing — slave modes

3.8 Human-machine interfaces (HMI)

3.8.1 TSI electrical specifications

Table 64. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	µA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	µA
TSI_EN	Power consumption in enable mode	—	100	—	µA
TSI_DIS	Power consumption in disable mode	—	1.2	—	µA
TSI_TEN	TSI analog enable time	—	66	—	µs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	0.19	—	1.03	V

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
100-pin LQFP	98ASS23308W
121-pin XFBGA	98ASA00595D
144-pin LQFP	98ASS23177W[1]

1. The 144-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

5 Pinout

5.1 K80 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

The 144-pin LQFP and 121-WLCSP packages for this product are not yet available, however they are included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
x	—	H6	K9	NC	NC	NC								
—	—	—	G8	ADC0_SE16	ADC0_SE16	ADC0_SE16								
—	—	A11	—	NC	NC	NC								
—	—	J6	—	NC	NC	NC								
—	—	J4	—	NC	NC	NC								
1	1	B1	C10	PTE0	DISABLED		PTE0	SPI1_PCS1	LPUART1_TX	SDHC0_D1	QSPI0A_DATA3	I2C1_SDA	RTC_CLKOUT	
2	2	C2	D9	PTE1/LLWU_P0	DISABLED		PTE1/LLWU_P0	SPI1_SCK	LPUART1_RX	SDHC0_D0	QSPI0A_SCLK	I2C1_SCL	SPI1_SIN	
3	3	C1	D10	PTE2/LLWU_P1	DISABLED		PTE2/LLWU_P1	SPI1_SOUT	LPUART1_CTS_b	SDHC0_DCLK	QSPI0A_DATA0		SPI1_SCK	
4	4	D2	B11	PTE3	DISABLED		PTE3	SPI1_PCS2	LPUART1_RTS_b	SDHC0_CMD	QSPI0A_DATA2		SPI1_SOUT	

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
5	5	F7	F6	VSS	VSS	VSS								
6	6	E5	F7	VDDIO_E	VDDIO_E	VDDIO_E								
7	7	D1	C11	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_SIN	LPUART3_TX	SDHC0_D3	QSPI0A_DATA1			
8	8	E2	E8	PTE5	DISABLED		PTE5	SPI1_PCS0	LPUART3_RX	SDHC0_D2	QSPI0A_SS0_B	FTM3_CH0	USB0_SOF_OUT	
9	9	E1	E9	PTE6/ LLWU_P16	DISABLED		PTE6/ LLWU_P16	SPI1_PCS3	LPUART3_CTS_b	I2S0_MCLK	QSPI0B_DATA3	FTM3_CH1	SDHC0_D4	
10	10	F3	E10	PTE7	DISABLED		PTE7	SPI2_SCK	LPUART3_RTS_b	I2S0_RXD0	QSPI0B_SCLK	FTM3_CH2	QSPI0A_SS1_B	
11	11	F2	D11	PTE8	DISABLED		PTE8	I2S0_RXD1	SPI2_SOUT	I2S0_RX_FS	QSPI0B_DATA0	FTM3_CH3	SDHC0_D5	
12	12	F1	E11	PTE9/ LLWU_P17	DISABLED		PTE9/ LLWU_P17	I2S0_TXD1	SPI2_PCS1	I2S0_RX_BCLK	QSPI0B_DATA2	FTM3_CH4	SDHC0_D6	
13	13	G2	F8	PTE10/ LLWU_P18	DISABLED		PTE10/ LLWU_P18	I2C3_SDA	SPI2_SIN	I2S0_TXD0	QSPI0B_DATA1	FTM3_CH5	SDHC0_D7	
14	14	G1	F9	PTE11	DISABLED		PTE11	I2C3_SCL	SPI2_PCS0	I2S0_TX_FS	QSPI0B_SS0_B	FTM3_CH6	QSPI0A_DQS	
15	—	—	—	PTE12	DISABLED		PTE12		LPUART2_TX	I2S0_TX_BCLK	QSPI0B_DQS	FTM3_CH7	FXIO0_D2	QSPI0A_DATA3
16	—	—	—	PTE13	DISABLED		PTE13		LPUART2_RX		QSPI0B_SS1_B	SDHC0_CLKIN	FXIO0_D3	QSPI0A_SCLK
17	15	—	F10	VDDIO_E	VDDIO_E	VDDIO_E								
18	16	—	F11	VSS	VSS	VSS								
19	—	—	—	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	LPUART2_TX	FTM_CLKIN0		FTM0_FLT3	FXIO0_D4	QSPI0A_DATA0
20	—	—	—	PTE17/ LLWU_P19	ADC0_SE5a	ADC0_SE5a	PTE17/ LLWU_P19	SPI0_SCK	LPUART2_RX	FTM_CLKIN1		LPTMR0_ALT3/ LPTMR1_ALT3	FXIO0_D5	QSPI0A_DATA2
21	—	—	—	PTE18/ LLWU_P20	ADC0_SE6a	ADC0_SE6a	PTE18/ LLWU_P20	SPI0_SOUT	LPUART2_CTS_b	I2C0_SDA			FXIO0_D6	QSPI0A_DATA1
22	—	—	—	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	LPUART2_RTS_b	I2C0_SCL			FXIO0_D7	QSPI0A_SS0_B
23	16	H3	F11	VSS	VSS	VSS								
24	17	H2	G11	USB0_DP	USB0_DP	USB0_DP								
25	18	H1	H11	USB0_DM	USB0_DM	USB0_DM								
26	19	J1	G10	VOUT33	VOUT33	VOUT33								
27	20	J2	H10	VREGIN	VREGIN	VREGIN								
28	21	—	G9	NC	NC	NC								
29	—	K2	J10	ADC0_DP0	ADC0_DP0	ADC0_DP0								
30	—	K1	K10	ADC0_DM0	ADC0_DM0	ADC0_DM0								
31	—	J3	J11	ADC0_DP3	ADC0_DP3	ADC0_DP3								

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
32	—	K3	K11	ADC0_DM3	ADC0_DM3	ADC0_DM3								
33	22	F5	H8	VDDA	VDDA	VDDA								
34	23	G5	H9	VREFH	VREFH	VREFH								
35	24	G6	J9	VREFL	VREFL	VREFL								
36	25	F6	J8	VSSA	VSSA	VSSA								
37	26	L2	—	ADC0_DP1	ADC0_DP1	ADC0_DP1								
38	27	L1	—	ADC0_DM1	ADC0_DM1	ADC0_DM1								
39	28	L3	L11	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22								
40	29	K4	L10	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
42	30	K5	H7	RTC_WAKEUP_B	RTC_WAKEUP_B	RTC_WAKEUP_B								
43	31	L4	L9	XTAL32	XTAL32	XTAL32								
44	32	L5	L8	EXTAL32	EXTAL32	EXTAL32								
45	33	K6	K8	VBAT	VBAT	VBAT								
46	34	—	G7	VDD	VDD	VDD								
47	35	—	F6	VSS	VSS	VSS								
48	—	H5	L7	PTA20	DISABLED		PTA20	I2C0_SCL	LPUART4_TX	FTM_CLKIN1	FXIO0_D8	EWM_OUT_b	TPM_CLKIN1	
49	—	J5	K7	PTA21/ LLWU_P21	DISABLED		PTA21/ LLWU_P21	I2C0_SDA	LPUART4_RX		FXIO0_D9	EWM_IN		
50	36	L7	J7	PTA0	JTAG_TCLK/ SWD_CLK	TSI0_CH1	PTA0	LPUART0_CTS_b	FTM0_CH5		FXIO0_D10	EMVSIM0_CLK	JTAG_TCLK/ SWD_CLK	
51	37	H8	J6	PTA1	JTAG_TDI	TSI0_CH2	PTA1	LPUART0_RX	FTM0_CH6	I2C3_SDA	FXIO0_D11	EMVSIM0_IO	JTAG_TDI	
52	38	J7	K6	PTA2	JTAG_TDO/ TRACE_SWO	TSI0_CH3	PTA2	LPUART0_TX	FTM0_CH7	I2C3_SCL	FXIO0_D12	EMVSIM0_PD	JTAG_TDO/ TRACE_SWO	
53	39	H9	L6	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	LPUART0_RTS_b	FTM0_CH0		FXIO0_D13	EMVSIM0_RST	JTAG_TMS/ SWD_DIO	
54	40	J8	H6	PTA4/ LLWU_P3	NMI_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1		FXIO0_D14	EMVSIM0_VCCEN	NMI_b	

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
55	41	K7	H5	PTA5	DISABLED		PTA5	USB0_CLKIN	FTM0_CH2		FXIO0_D15	I2S0_TX_BCLK	JTAG_TRST_b	
56	—	L10	G6	VDD	VDD	VDD								
57	—	K10	F5	VSS	VSS	VSS								
58	—	—	—	PTA6	DISABLED		PTA6	I2C2_SCL	FTM0_CH3	EMVSIM1_CLK	CLKOUT		TRACE_CLKOUT	
59	—	—	—	PTA7	ADC0_SE10	ADC0_SE10	PTA7	I2C2_SDA	FTM0_CH4	EMVSIM1_IO			TRACE_D3	
60	—	—	—	PTA8	ADC0_SE11	ADC0_SE11	PTA8		FTM1_CH0	EMVSIM1_PD		FTM1_QD_PHA/TPM1_CH0	TRACE_D2	
61	—	—	—	PTA9	DISABLED		PTA9		FTM1_CH1	EMVSIM1_RST		FTM1_QD_PHB/TPM1_CH1	TRACE_D1	
62	—	J9	L5	PTA10/LLWU_P22	DISABLED		PTA10/LLWU_P22	I2C2_SDA	FTM2_CH0	EMVSIM1_VCCEN	FXIO0_D16	FTM2_QD_PHA/TPM2_CH0	TRACE_D0	
63	—	H7	L4	PTA11/LLWU_P23	DISABLED		PTA11/LLWU_P23	I2C2_SCL	FTM2_CH1		FXIO0_D17	FTM2_QD_PHB/TPM2_CH1		
64	42	K8	K5	PTA12	DISABLED		PTA12		FTM1_CH0	TRACE_CLKOUT	FXIO0_D18	I2S0_TXD0	FTM1_QD_PHA/TPM1_CH0	
65	43	L8	J5	PTA13/LLWU_P4	DISABLED		PTA13/LLWU_P4		FTM1_CH1	TRACE_D3	FXIO0_D19	I2S0_TX_FS	FTM1_QD_PHB/TPM1_CH1	
66	44	K9	L3	PTA14	DISABLED		PTA14	SPI0_PCS0	LPUART0_TX	TRACE_D2	FXIO0_D20	I2S0_RX_BCLK	I2S0_TXD1	
67	45	L9	K4	PTA15	DISABLED		PTA15	SPI0_SCK	LPUART0_RX	TRACE_D1	FXIO0_D21	I2S0_RXD0		
68	46	J10	J4	PTA16	DISABLED		PTA16	SPI0_SOUT	LPUART0_CTS_b	TRACE_D0	FXIO0_D22	I2S0_RX_FS	I2S0_RXD1	
69	47	H10	K3	PTA17	DISABLED		PTA17	SPI0_SIN	LPUART0_RTS_b		FXIO0_D23	I2S0_MCLK		
70	48	E6	L2	VDD	VDD	VDD								
71	49	G7	K2	VSS	VSS	VSS								
72	50	L11	L1	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0			TPM_CLKIN0	
73	51	K11	K1	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1/LPTMR1_ALT1	TPM_CLKIN1	
74	52	J11	J1	RESET_b	RESET_b	RESET_b								
75	—	—	—	PTA24	DISABLED		PTA24	EMVSIM0_CLK				FB_A29		

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
76	—	—	—	PTA25	DISABLED		PTA25	EMVSIM0_IO				FB_A28		
77	—	—	—	PTA26	DISABLED		PTA26	EMVSIM0_PD				FB_A27		
78	—	—	—	PTA27	DISABLED		PTA27	EMVSIM0_RST				FB_A26		
79	—	—	—	PTA28	DISABLED		PTA28	EMVSIM0_VCCEN				FB_A25		
80	—	H11	J2	PTA29	DISABLED		PTA29					FB_A24		
81	53	G11	J3	PTB0/LLWU_P5	ADC0_SE8/TSI0_CH0	ADC0_SE8/TSI0_CH0	PTB0/LLWU_P5	I2C0_SCL	FTM1_CH0		SDRAM_CAS_b	FTM1_QD_PHA/TPM1_CH0	FXIO0_D0	
82	54	G10	H2	PTB1	ADC0_SE9/TSI0_CH6	ADC0_SE9/TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1		SDRAM_RAS_b	FTM1_QD_PHB/TPM1_CH1	FXIO0_D1	
83	55	G9	H1	PTB2	ADC0_SE12/TSI0_CH7	ADC0_SE12/TSI0_CH7	PTB2	I2C0_SCL	LPUART0_RTS_b		SDRAM_WE	FTM0_FLT3	FXIO0_D2	
84	56	G8	H3	PTB3	ADC0_SE13/TSI0_CH8	ADC0_SE13/TSI0_CH8	PTB3	I2C0_SDA	LPUART0_CTS_b		SDRAM_CS0_b	FTM0_FLT0	FXIO0_D3	
85	—	B11	H4	PTB4	DISABLED		PTB4	EMVSIM1_IO			SDRAM_CS1_b	FTM1_FLT0		
86	—	C11	G1	PTB5	DISABLED		PTB5	EMVSIM1_CLK				FTM2_FLT0		
87	—	F11	G2	PTB6	DISABLED		PTB6	EMVSIM1_VCCEN			FB_AD23/SDRAM_D23			
88	—	E11	G3	PTB7	DISABLED		PTB7	EMVSIM1_PD			FB_AD22/SDRAM_D22			
89	—	D11	G4	PTB8	DISABLED		PTB8	EMVSIM1_RST	LPUART3_RTS_b		FB_AD21/SDRAM_D21			
90	57	E10	G5	PTB9	DISABLED		PTB9	SPI1_PCS1	LPUART3_CTS_b		FB_AD20/SDRAM_D20			
91	58	D10	F1	PTB10	DISABLED		PTB10	SPI1_PCS0	LPUART3_RX	I2C2_SCL	FB_AD19/SDRAM_D19	FTM0_FLT1	FXIO0_D4	
92	59	C10	F2	PTB11	DISABLED		PTB11	SPI1_SCK	LPUART3_TX	I2C2_SDA	FB_AD18/SDRAM_D18	FTM0_FLT2	FXIO0_D5	
93	60	L6	F5	VSS	VSS	VSS								
94	61	E7	G6	VDD	VDD	VDD								

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
95	62	B10	E1	PTB16	TSI0_CH9	TSI0_CH9	PTB16	SPI1_SOUT	LPUART0_RX	FTM_CLKIN0	FB_AD17/SDRAM_D17	EWM_IN	TPM_CLKIN0	
96	63	E9	F3	PTB17	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	LPUART0_TX	FTM_CLKIN1	FB_AD16/SDRAM_D16	EWM_OUT_b	TPM_CLKIN1	
97	64	D9	F4	PTB18	TSI0_CH11	TSI0_CH11	PTB18		FTM2_CH0	I2S0_TX_BCLK	FB_AD15/SDRAM_A23	FTM2_QD_PHA/TPM2_CH0	FXIO0_D6	
98	65	C9	E2	PTB19	TSI0_CH12	TSI0_CH12	PTB19		FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_PHB/TPM2_CH1	FXIO0_D7	
99	66	F10	D1	PTB20	DISABLED		PTB20	SPI2_PCS0			FB_AD31/SDRAM_D31	CMP0_OUT	FXIO0_D8	
100	67	F9	E3	PTB21	DISABLED		PTB21	SPI2_SCK			FB_AD30/SDRAM_D30	CMP1_OUT	FXIO0_D9	
101	68	F8	E4	PTB22	DISABLED		PTB22	SPI2_SOUT			FB_AD29/SDRAM_D29		FXIO0_D10	
102	69	E8	D2	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28/SDRAM_D28		FXIO0_D11	
103	70	B9	C1	PTC0	ADC0_SE14/TSI0_CH13	ADC0_SE14/TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG	USB0_SOF_OUT	FB_AD14/SDRAM_A22	I2S0_TXD1	FXIO0_D12	
104	71	D8	D3	PTC1/LLWU_P6	ADC0_SE15/TSI0_CH14	ADC0_SE15/TSI0_CH14	PTC1/LLWU_P6	SPI0_PCS3	LPUART1_RTS_b	FTM0_CH0	FB_AD13/SDRAM_A21	I2S0_TXD0	FXIO0_D13	
105	72	C8	C2	PTC2	ADC0_SE4b/CMP1_IN0/TSI0_CH15	ADC0_SE4b/CMP1_IN0/TSI0_CH15	PTC2	SPI0_PCS2	LPUART1_CTS_b	FTM0_CH1	FB_AD12/SDRAM_A20	I2S0_TX_FS		
106	73	B8	B1	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	LPUART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK		
107	74	—	E5	VSS	VSS	VSS								
108	75	—	G6	VDD	VDD	VDD								
109	76	A8	A1	PTC4/LLWU_P8	DISABLED		PTC4/LLWU_P8	SPI0_PCS0	LPUART1_TX	FTM0_CH3	FB_AD11/SDRAM_A19	CMP1_OUT		
110	77	D7	B2	PTC5/LLWU_P9	DISABLED		PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2/LPTMR1_ALT2	I2S0_RXD0	FB_AD10/SDRAM_A18	CMP0_OUT	FTM0_CH2	
111	78	C7	C3	PTC6/LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK	FB_AD9/SDRAM_A17	I2S0_MCLK	FXIO0_D14	

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
112	79	B7	A2	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB0_SOF_OUT	I2S0_RX_FS	FB_AD8/SDRAM_A16		FXIO0_D15	
113	80	A7	B3	PTC8	CMP0_IN2	CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK	FB_AD7/SDRAM_A15		FXIO0_D16	
114	81	D6	D4	PTC9	CMP0_IN3	CMP0_IN3	PTC9		FTM3_CH5	I2S0_RX_BCLK	FB_AD6/SDRAM_A14	FTM2_FLT0	FXIO0_D17	
115	82	C6	A3	PTC10	DISABLED		PTC10	I2C1_SCL	FTM3_CH6	I2S0_RX_FS	FB_AD5/SDRAM_A13		FXIO0_D18	
116	83	C5	C4	PTC11/LLWU_P11	DISABLED		PTC11/LLWU_P11	I2C1_SDA	FTM3_CH7	I2S0_RXD1	FB_RW_b		FXIO0_D19	
117	84	B6	B4	PTC12	DISABLED		PTC12		LPUART4_RTS_b	FTM_CLKIN0	FB_AD27/SDRAM_D27	FTM3_FLT0	TPM_CLKIN0	
118	85	A6	A4	PTC13	DISABLED		PTC13		LPUART4_CTS_b	FTM_CLKIN1	FB_AD26/SDRAM_D26		TPM_CLKIN1	
119	86	A5	D5	PTC14	DISABLED		PTC14		LPUART4_RX		FB_AD25/SDRAM_D25		FXIO0_D20	
120	87	B5	C5	PTC15	DISABLED		PTC15		LPUART4_TX		FB_AD24/SDRAM_D24		FXIO0_D21	
121	88	—	F6	VSS	VSS	VSS								
122	89	—	E6	VDD	VDD	VDD								
123	—	D5	A5	PTC16	DISABLED		PTC16		LPUART3_RX		FB_CS5_b/FB_TSIZ1/FB_BE23_16_BLS15_8_b/SDRAM_DQM2			
124	90	C4	B5	PTC17	DISABLED		PTC17		LPUART3_TX		FB_CS4_b/FB_TSIZ0/FB_BE31_24_BLS7_0_b/SDRAM_DQM3			
125	—	B4	A6	PTC18	DISABLED		PTC18		LPUART3_RTS_b		FB_TBST_b/FB_CS2_b/FB_BE15_8_BLS23_16_b/			

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
											SDRAM_DQM1			
126	—	A4	B6	PTC19	DISABLED		PTC19		LPUART3_CTS_b		FB_CS3_b/FB_BE7_0_BLS31_24_b/SDRAM_DQM0	FB_TA_b		
127	91	D4	C6	PTD0/LLWU_P12	DISABLED		PTD0/LLWU_P12	SPI0_PCS0	LPUART2_RTS_b	FTM3_CH0	FB_ALE/FB_CS1_b/FB_TS_b		FXIO0_D22	
128	92	D3	D6	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	LPUART2_CTS_b	FTM3_CH1	FB_CS0_b		FXIO0_D23	
129	93	C3	D7	PTD2/LLWU_P13	DISABLED		PTD2/LLWU_P13	SPI0_SOUT	LPUART2_RX	FTM3_CH2	FB_AD4/SDRAM_A12		I2C0_SCL	
130	94	B3	A7	PTD3	DISABLED		PTD3	SPI0_SIN	LPUART2_TX	FTM3_CH3	FB_AD3/SDRAM_A11		I2C0_SDA	
131	95	A3	B7	PTD4/LLWU_P14	DISABLED		PTD4/LLWU_P14	SPI0_PCS1	LPUART0_RTS_b	FTM0_CH4	FB_AD2/SDRAM_A10	EWM_IN	SPI1_PCS0	
132	96	A2	C7	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	LPUART0_CTS_b	FTM0_CH5	FB_AD1/SDRAM_A9	EWM_OUT_b	SPI1_SCK	
133	97	B2	A8	PTD6/LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/LLWU_P15	SPI0_PCS3	LPUART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0	SPI1_SOUT	
134	98	—	F6	VSS	VSS	VSS								
135	99	—	E7	VDD	VDD	VDD								
136	100	A1	B8	PTD7	DISABLED		PTD7	CMT_IRO	LPUART0_TX	FTM0_CH7	SDRAM_CKE	FTM0_FLT1	SPI1_SIN	
137	—	A10	A9	PTD8/LLWU_P24	DISABLED		PTD8/LLWU_P24	I2C0_SCL				FB_A16	FXIO0_D24	
138	—	A9	C8	PTD9	DISABLED		PTD9	I2C0_SDA				FB_A17	FXIO0_D25	
139	—	E4	B9	PTD10	DISABLED		PTD10					FB_A18	FXIO0_D26	
140	—	E3	A10	PTD11/LLWU_P25	DISABLED		PTD11/LLWU_P25	SPI2_PCS0				FB_A19	FXIO0_D27	
141	—	F4	D8	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0			FB_A20	FXIO0_D28	
142	—	G3	C9	PTD13	DISABLED		PTD13	SPI2_SOUT				FB_A21	FXIO0_D29	
143	—	G4	B10	PTD14	DISABLED		PTD14	SPI2_SIN				FB_A22	FXIO0_D30	
144	—	H4	A11	PTD15	DISABLED		PTD15	SPI2_PCS1				FB_A23	FXIO0_D31	

5.2 Recommended connection for unused analog and digital pins

Table 65 shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application

Table 65. Recommended connection for unused analog interfaces

Pin Type		Short recommendation	Detailed recommendation
Analog/non GPIO	ADCx/CMPx	Float	Analog input - Float
Analog/non GPIO	VREF_OUT	Float	Analog output - Float
Analog/non GPIO	DAC0_OUT, DAC1_OUT	Float	Analog output - Float
Analog/non GPIO	RTC_WAKEUP_B	Float	Analog output - Float
Analog/non GPIO	XTAL32	Float	Analog output - Float
Analog/non GPIO	EXTAL32	Float	Analog input - Float
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)
GPIO/Analog	PTx/TSIOx	Float	Float (default is analog input)
GPIO/Digital	PTA0/JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	PTA1/JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA2/JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA3/JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA4/NMI_b	10kΩ pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
USB	USB0_DP	Float	Float
USB	USB0_DM	Float	Float
USB	VOUT33	Tie to input and ground through 10kΩ	Tie to input and ground through 10kΩ
USB	VREGIN	Tie to output and ground through 10kΩ	Tie to output and ground through 10kΩ
USB	USB0_VSS	Always connect to VSS	Always connect to VSS
VBAT	VBAT	Float	Float
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential

Table continues on the next page...

Table 65. Recommended connection for unused analog interfaces (continued)

Pin Type		Short recommendation	Detailed recommendation
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential

5.3 K80 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

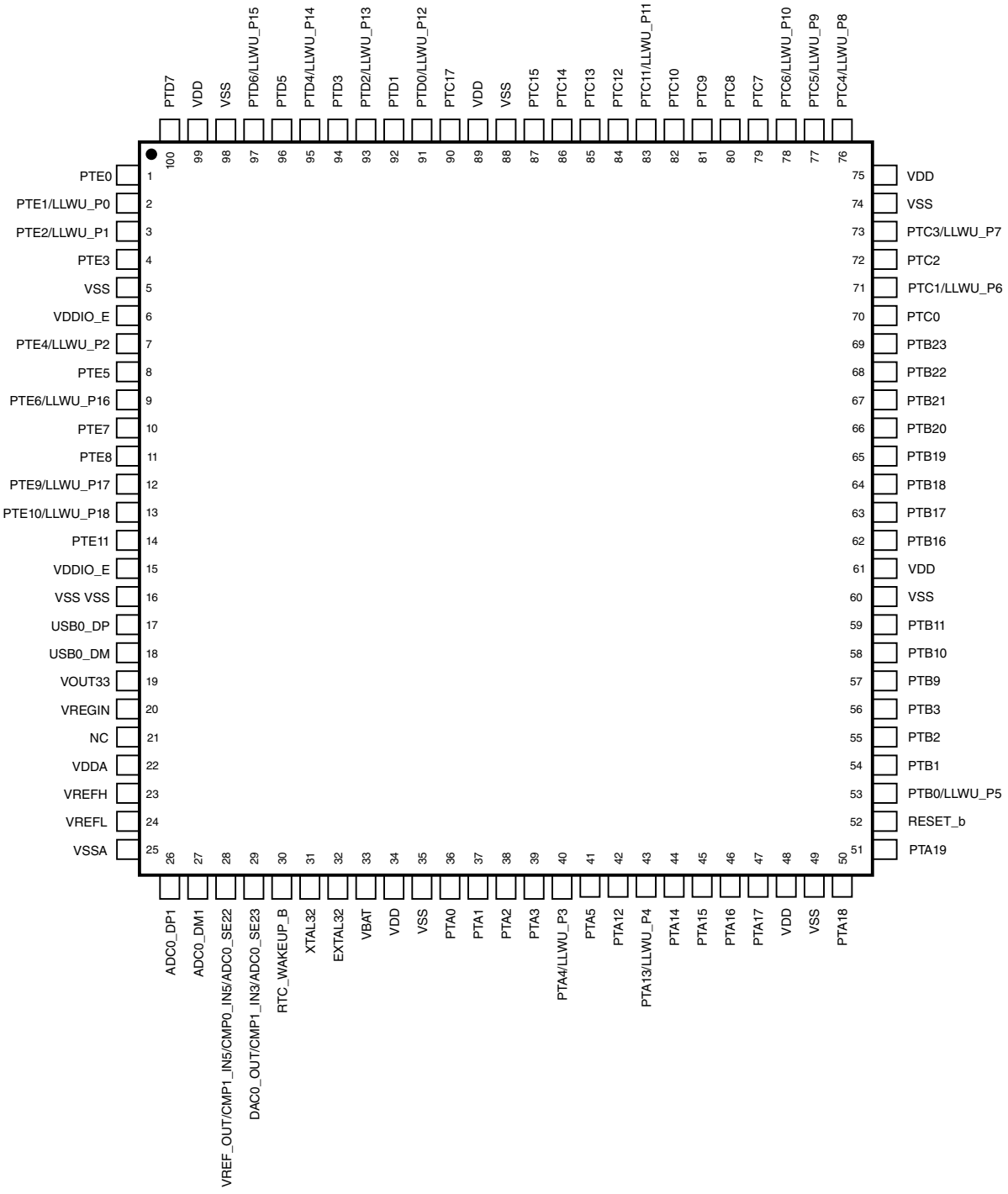


Figure 45. K80 100 LQFP Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	PTC19	PTC14	PTC13	PTC8	PTC4/ LLWU_P8	PTD9	PTD8/ LLWU_P24	NC	A
B	PTE0	PTD6/ LLWU_P15	PTD3	PTC18	PTC15	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	PTB4	B
C	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTD2/ LLWU_P13	PTC17	PTC11/ LLWU_P11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	PTB5	C
D	PTE4/ LLWU_P2	PTE3	PTD1	PTD0/ LLWU_P12	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6	PTB18	PTB10	PTB8	D
E	PTE6/ LLWU_P16	PTE5	PTD11/ LLWU_P25	PTD10	VDDIO_E	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	PTE9/ LLWU_P17	PTE8	PTE7	PTD12	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	PTB6	F
G	PTE11	PTE10/ LLWU_P18	PTD13	PTD14	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	USB0_DM	USB0_DP	VSS	PTD15	PTA20	NC	PTA11/ LLWU_P23	PTA1	PTA3	PTA17	PTA29	H
J	VOUT33	VREGIN	ADC0_DP3	NC	PTA21/ LLWU_P21	NC	PTA2	PTA4/ LLWU_P3	PTA10/ LLWU_P22	PTA16	RESET_b	J
K	ADC0_DM0	ADC0_DP0	ADC0_DM3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	RTC_ WAKEUP_B	VBAT	PTA5	PTA12	PTA14	VSS	PTA19	K
L	ADC0_DM1	ADC0_DP1	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22	XTAL32	EXTAL32	VSS	PTA0	PTA13/ LLWU_P4	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 46. K80 121 XFBGA Pinout Diagram

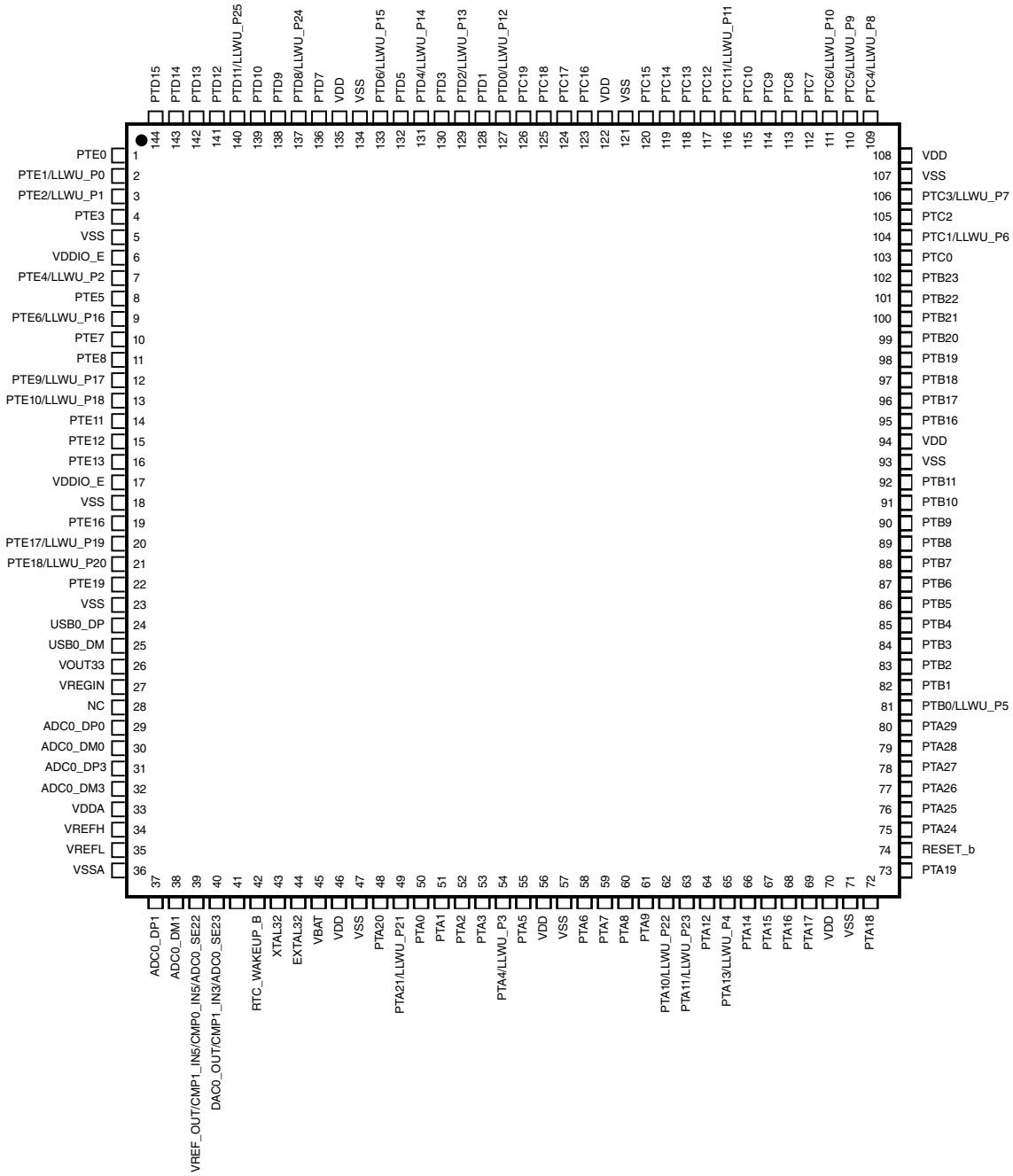
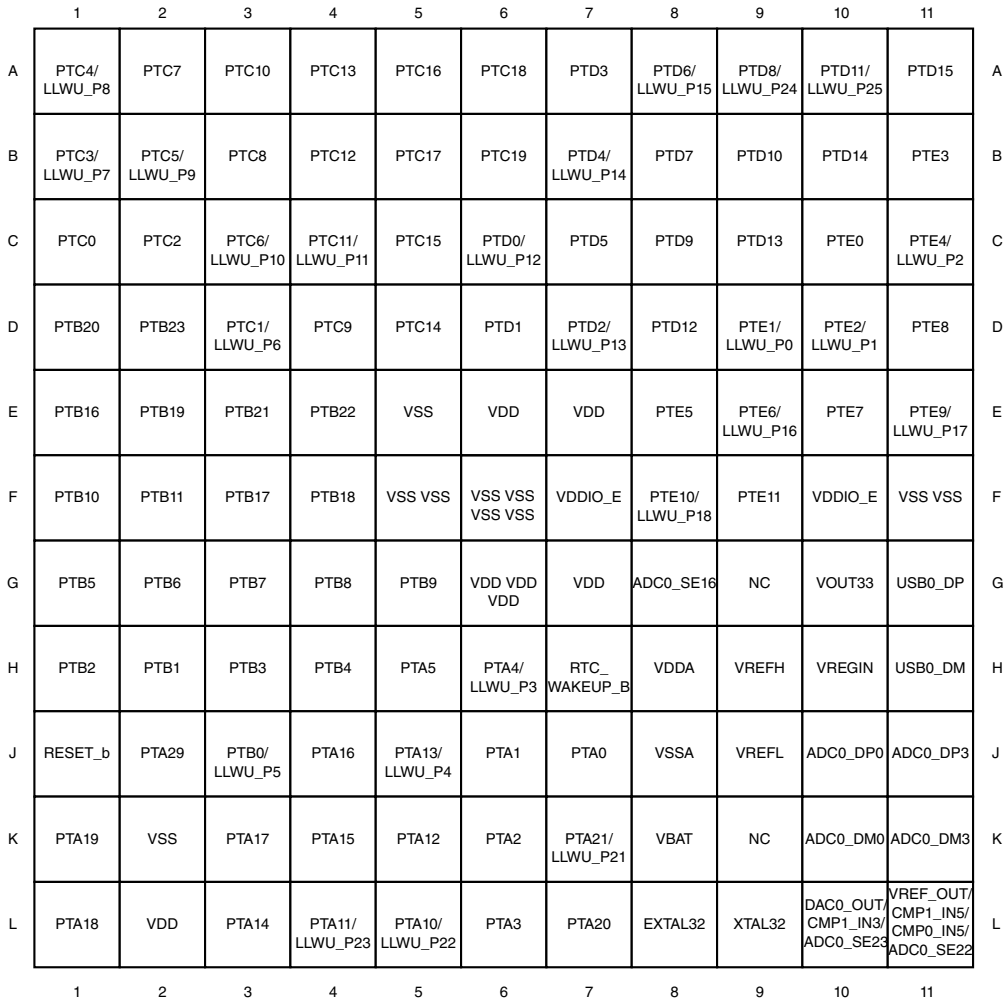


Figure 47. K80 144 LQFP Pinout Diagram

NOTE

The 144-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.



	1	2	3	4	5	6	7	8	9	10	11	
A	PTC4/ LLWU_P8	PTC7	PTC10	PTC13	PTC16	PTC18	PTD3	PTD6/ LLWU_P15	PTD8/ LLWU_P24	PTD11/ LLWU_P25	PTD15	A
B	PTC3/ LLWU_P7	PTC5/ LLWU_P9	PTC8	PTC12	PTC17	PTC19	PTD4/ LLWU_P14	PTD7	PTD10	PTD14	PTE3	B
C	PTC0	PTC2	PTC6/ LLWU_P10	PTC11/ LLWU_P11	PTC15	PTD0/ LLWU_P12	PTD5	PTD9	PTD13	PTE0	PTE4/ LLWU_P2	C
D	PTB20	PTB23	PTC1/ LLWU_P6	PTC9	PTC14	PTD1	PTD2/ LLWU_P13	PTD12	PTE1/ LLWU_P0	PTE2/ LLWU_P1	PTE8	D
E	PTB16	PTB19	PTB21	PTB22	VSS	VDD	VDD	PTE5	PTE6/ LLWU_P16	PTE7	PTE9/ LLWU_P17	E
F	PTB10	PTB11	PTB17	PTB18	VSS VSS	VSS VSS VSS VSS	VDDIO_E	PTE10/ LLWU_P18	PTE11	VDDIO_E	VSS VSS	F
G	PTB5	PTB6	PTB7	PTB8	PTB9	VDD VDD VDD	VDD	ADC0_SE16	NC	VOUT33	USB0_DP	G
H	PTB2	PTB1	PTB3	PTB4	PTA5	PTA4/ LLWU_P3	RTC_ WAKEUP_B	VDDA	VREFH	VREGIN	USB0_DM	H
J	RESET_b	PTA29	PTB0/ LLWU_P5	PTA16	PTA13/ LLWU_P4	PTA1	PTA0	VSSA	VREFL	ADC0_DP0	ADC0_DP3	J
K	PTA19	VSS	PTA17	PTA15	PTA12	PTA2	PTA21/ LLWU_P21	VBAT	NC	ADC0_DM0	ADC0_DM3	K
L	PTA18	VDD	PTA14	PTA11/ LLWU_P23	PTA10/ LLWU_P22	PTA3	PTA20	EXTAL32	XTAL32	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 48. K80 121 WLCSP Pinout Diagram

NOTE

The 121-pin WLCSP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: MK80.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
K##	Kinetis family	• K80
A	Key attribute	• D = Cortex-M4 w/ DSP • F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB • 1M0 = 1 MB • 2M0 = 2 MB

Table continues on the next page...

Field	Description	Values
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • DC = 121 XFBGA (8 mm x 8 mm x 0.5 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz • 18 = 180 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MK80FN256VLL15

8 Terminology and guidelines

8.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered.

Table continues on the next page...

Term	Definition
	NOTE: The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

8.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

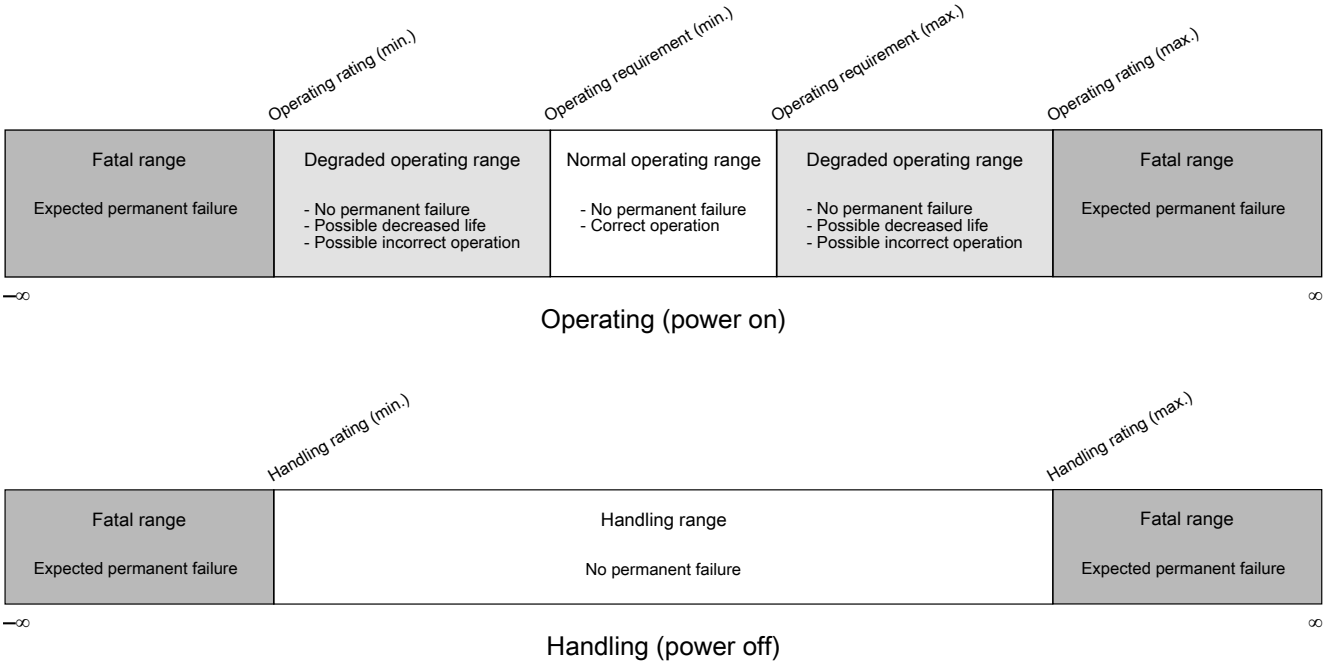
Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

8.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

8.4 Relationship between ratings and operating requirements



8.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9 Revision History

The following table provides a revision history for this document.

Table 66. Revision History

Rev. No.	Date	Substantial Changes
0	08/2014	Initial Release
1	09/2014	• Updated dimensions of 121 WLCSP package drawing • Updated instances of I2S module to one • Updated the maximum number of I/Os • Removed DDR specs all over the datasheet • Updated Voltage and Current Operating behaviors table • Updated QuadSPI input timing (SDR mode) diagram • Updated 35 pf load to load of 15pf (1.8V), 35pf (3V) • Updated Notes in QuadSPI AC specifications section
2	03/2015	• Updated frequencies of footnotes of Power Consumption Operating behaviors table • Added entry of VDDIO in Voltage and current operating requirements • Updated the footnotes of Voltage and current operating ratings • Updated the description of of I_{pll} in MCG specs • Updated the minimum value of FB4 in Flexbus limited voltage range switching specifications table • Updated the minimum value of D5 in SDRAM Timing (Limited voltage range) table • Added SD1 clock frequencies for high speed • Updated the package size of 121 XFBGA to 8x8x0.5mm with a 0.65mm pitch • Added Recommended POR sequencing topic • Updated the typical values of Power consumption operating behaviors table • Updated the Run mode supply current vs. core frequency diagram • Updated the number of I2C instances in front matter and deleted "0" after LPUART • Updated VLPR mode supply current vs. core frequency figure

3	05/2015	• Added maximum number of I/Os in the Ordering Information table.
		• Updated 'Voltage and current operating ratings' table.
		• Updated 'Voltage and current operating requirements' table.
		  ◦ Added rows for V_{IH_E}, V_{IL_E}, and V_{HYS_E}.
		  ◦ Removed I_{ICAIO} parameter description from the table.
		  ◦ Removed positive current injection specifications from I_{ICcont}.
		  ◦ Updated footnotes.
		• Updated 'Voltage and current operating behaviors' table.
		• Updated Max. values in the 'Power mode transition operating behaviors' table.
		• Corrected Typ. values of I_{DD_LLS2} and I_{DD_LLS3} in 'Power consumption operating behaviors' table.
		• Updated 'General switching specifications' table.
		• Updated 'Thermal operating requirements' table to include footnotes.
		• Updated Typ. and Max. values of the f_{dco_t} parameter in the 'MCG Specifications' table.
		• Updated Max. values for SD1 (fpp) and SD6 in the 'SDHC full voltage range switching specifications' table and for SD6 in the 'SDHC limited voltage range switching specifications' table.

4	09/2015	• Updated part numbers.
		• Updated Related Resources table to include package drawing numbers and other relevant resource information.
		• Updated title of section 2.2.2 to 'HVD, LVD and POR operating requirements'.
		• Updated 'V_{DD} supply LVD and POR operating requirements' table.
		  ◦ Added rows for V_{HVDH} and V_{HVDL}.
		• Updated 'Power consumption operating behaviors' table.
		  ◦ Updated Typ. values and Max. values.
		  ◦ Added data for 105°C.
		• Updated IDD charts - Figure 6. Run mode supply current vs. core frequency and Figure 7. VLPR mode supply current vs. core frequency.

Table 66. Revision History

Rev. No.	Date	Substantial Changes

		• Replaced section 2.2.6 'EMC radiated emissions operating behaviors' with 'Electromagnetic Compatibility (EMC) specifications'.
		• Removed EZPort information from 'General switching specifications' table.
		• Updated 100 LQFP and 121 XFBGA values in the 'Thermal attributes' table.
		• Updated 'MCG specifications' table
		  • Updated Typ. value of Δfdco_t from -1 to ±1.
		  • Removed J_{acc_fll} data.
		  • Updated description of I_{pll} and their corresponding Typ. values.
		  • Updated Typ. values of J_{cyc_pll} and J_{acc_pll}.
		• Updated footnote 2 in 'SDRAM Timing (Full voltage range)' table - corrected maximum frequency of FB_CLK to 75MHz.
		• Removed I_{ALKG} data from 'Comparator and 6-bit DAC electrical specifications' table.
		• Updated Min and Max values of S_{freq} in the 'Timing Specifications, High Drive Strength' table.
		• Updated the 'Timing Requirements for Power-down Sequence' table.
		  • Added a footnote - "Frtcclk is ERCLK32K, and this clock must be enabled during the power down sequence."
		  • Updated unit from ns to µs.
		• Added 121 WLCSP pin assignment information and diagram to the Pinout section.

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