

## QUARTZ CRYSTAL OSCILLATOR

### ■ GENERAL DESCRIPTION

The NJU6323 series is a C-MOS quartz crystal oscillator which consists of an oscillation amplifier, 3-stage divider, output frequency selector and 3-state output buffer.

The oscillation frequency is as wide as up to 50MHz and the symmetry of 45-55% is realized over full oscillation frequency range.

The oscillation amplifier incorporates feed-back resistance and oscillation capacitors( $C_g$ ,  $C_d$ ), therefore, it requires no external component except quartz crystal.

The 3-stage divider outputs  $f_0$ ,  $f_0/2$ ,  $f_0/4$  and  $f_0/8$  to the output frequency selector and it determined one output frequency according to the combination of two input-signal.

The 3-state output buffer is C-MOS compatible and capable of 10 LSTTL driving.

### ■ PACKAGE OUTLINE



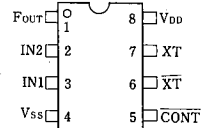
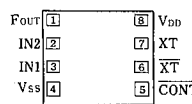
NJU6323XC



NJU6323XE

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### ■ PIN CONFIGURATION/PAD LOCATION



### ■ FEATURES

- Operating Voltage -- 3.0~6.0V
- Maximum Oscillation Frequency -- 50MHz
- Low Operating Current
- High Fan-out -- LSTTL 10
- 3-state Output Buffer
- Selected Frequency Output (mask option)  
Only one frequency out of  $f_0$ ,  $f_0/2$ ,  $f_0/4$  and  $f_0/8$  output
- Oscillation Capacitors  $C_g$  and  $C_d$  on-chip
- Oscillation and/or Output Stand-by Function
- Package Outline -- CHIP/EMP 8
- C-MOS Technology

### ■ COORDINATES

Unit:  $\mu\text{m}$

No.	PAD	X	Y
1	FOUT	165	651
2	IN2	165	484
3	IN1	165	317
4	VSS	165	149
5	CONT	1113	149
6	XT	1113	317
7	XT	1113	484
8	VDD	1113	651

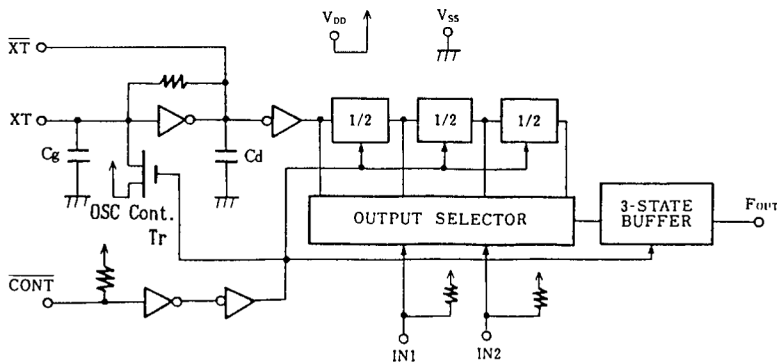
Chip Size : 1.28 X 0.8mm

Chip Thickness :  $400\mu\text{m} \pm 30\mu\text{m}$

### ■ LINE-UP TABLE

Type No.	$C_g$	$C_d$	Osc.Stop Function
NJU6323	21pF	23pF	Yes
NJU6323J	21pF	No	Yes
NJU6323P	No	No	Yes

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N					
5	CONT	Oscillation Stop Control and Divider Reset					
		CONT	F <sub>OUT</sub>				
		H	Output either one frequency from f <sub>o</sub> , f <sub>o</sub> /2, f <sub>o</sub> /4, and f <sub>o</sub> /8				
		L	Oscillation Stop, Output High Impedance and Divider Reset				
6	XT	Quartz Crystal Connecting Terminals					
7	XT						
8	V <sub>DD</sub>	+ 5V					
3	IN1	3-Stage Divider Outputs Selected by IN1 and IN2					
2	IN2				IN1	IN2	F <sub>OUT</sub>
					H	H	f <sub>o</sub>
					L	H	f <sub>o</sub> /2
					H	L	f <sub>o</sub> /4
		L	L	f <sub>o</sub> /8			
1	F <sub>OUT</sub>	Output either one frequency from f <sub>o</sub> , f <sub>o</sub> /2, f <sub>o</sub> /4, and f <sub>o</sub> /8					
4	V <sub>SS</sub>	GND					

■ ABSOLUTE MAXIMUM RATINGS

( Ta=25°C )

P A R A M E T E R	S Y M B O L	R A T I N G S	U N I T
Supply Voltage	V <sub>DD</sub>	-0.5 ~ +7.0	V
Input Voltage	V <sub>IN</sub>	-0.5 ~ V <sub>DD</sub> +0.5	V
Output Voltage	V <sub>O</sub>	-0.5 ~ V <sub>DD</sub> +0.5	V
Input Current	I <sub>IN</sub>	±10	mA
Output Current	I <sub>O</sub>	±25	mA
Power Dissipation (EMP)	P <sub>D</sub>	200	mW
Operating Temperature Range	T <sub>opr</sub>	-40 ~ + 85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 ~ +150	°C

(Note) Decoupling capacitor should be connected between V<sub>DD</sub> and V<sub>SS</sub> due to the stabilized operation for the circuit.

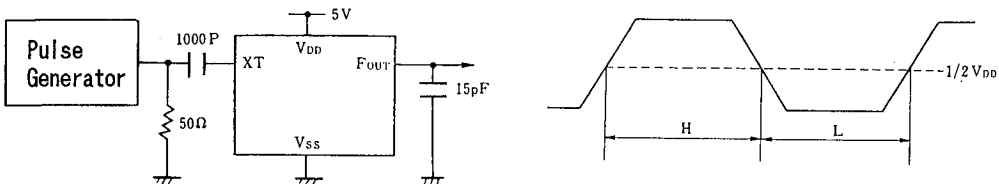
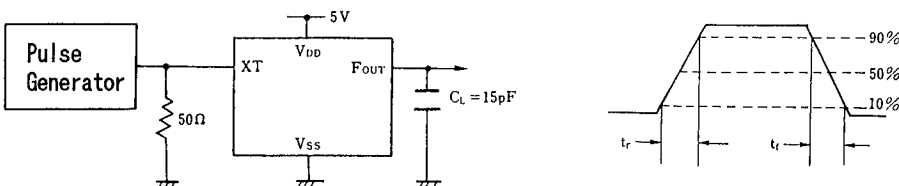
**■ ELECTRICAL CHARACTERISTICS**

 (  $T_a=25^{\circ}\text{C}$ ,  $V_{DD}=5\text{V}$  )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	$V_{DD}$		3		6	V
Operating Current	$I_{DD}$	$f_{osc}=16\text{MHz}$ , No load			10	mA
Stand-by Current	$I_{st}$	CONT, XT= $V_{SS}$ , No load (Note)			1	$\mu\text{A}$
Input Voltage	$V_{IH}$		3.5		5.0	V
	$V_{IL}$		0		1.5	
Output Current	$I_{OH}$	$V_{DD}=5\text{V}$ , $V_{OH}=4.5\text{V}$	4			mA
	$I_{OL}$	$V_{DD}=5\text{V}$ , $V_{OL}=0.5\text{V}$	4			
Input Current	$I_{IN}$	CONT, IN1, IN2 Terminals CONT, IN1, IN2= $V_{SS}$			400	$\mu\text{A}$
Internal Capacitor	$C_g$	Refer to Line-Up Table.				pF
	$C_d$					
Max. Oscillation Freq.	$f_{MAX}$	$V_{DD}=5\text{V}$ , $C_L=15\text{pF}$	50			MHz
Output Signal Symmetry	SYM	$V_{DD}=5\text{V}$ , $C_L=15\text{pF}$ at $1/2V_{DD}$	45	50	55	%
Output Signal Rise Time	$t_r$	$V_{DD}=5\text{V}$ , $C_L=15\text{pF}$ , 10% - 90%			8	ns
Output Signal Fall Time	$t_f$	$V_{DD}=5\text{V}$ , $C_L=15\text{pF}$ , 90% - 10%			8	ns

Note ) Excluding input current on CONT terminal.

**■ MEASUREMENT CIRCUITS**

 (1) Output Signal Symmetry ( $C_L=15\text{pF}$ )

 (2) Output Signal Rise/Fall Time ( $C_L=15\text{pF}$ )


# NJU6323 Series

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MEMO

**[CAUTION]**

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