

QUARTZ CRYSTAL OSCILLATOR

■ GENERAL DESCRIPTION

The NJU6323 series is a C-MOS quartz crystal oscillator which consists of an oscillation amplifier, 3-stage divider, output frequency selector and 3-state output buffer.

The oscillation frequency is as wide as up to 50MHz and the symmetry of 45-55% is realized over full oscillation frequency range.

The oscillation amplifier incorporates feed-back resistance and oscillation capacitors(C_g , C_d), therefore, it requires no external component except quartz crystal.

The 3-stage divider outputs f_0 , $f_0/2$, $f_0/4$ and $f_0/8$ to the output frequency selector and it determined one output frequency according to the combination of two input-signal.

The 3-state output buffer is C-MOS compatible and capable of 10 LSTTL driving.

■ FEATURES

- Operating Voltage -- 3.0~6.0V
- Maximum Oscillation Frequency -- 50MHz
- Low Operating Current
- High Fan-out -- LSTTL 10
- 3-state Output Buffer
- Selected Frequency Output (mask option)
Only one frequency out of f_0 , $f_0/2$, $f_0/4$ and $f_0/8$ output
- Oscillation Capacitors C_g and C_d on-chip
- Oscillation and/or Output Stand-by Function
- Package Outline -- CHIP/EMP 8
- C-MOS Technology

■ LINE-UP TABLE

Type No.	C_g	C_d	Osc.Stop Function
NJU6323	21pF	23pF	Yes
NJU6323J	21pF	No	Yes
NJU6323P	No	No	Yes

■ PACKAGE OUTLINE

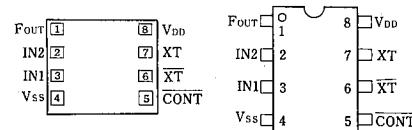


NJU6323XC

NJU6323XE

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■ PIN CONFIGURATION/PAD LOCATION



■ COORDINATES

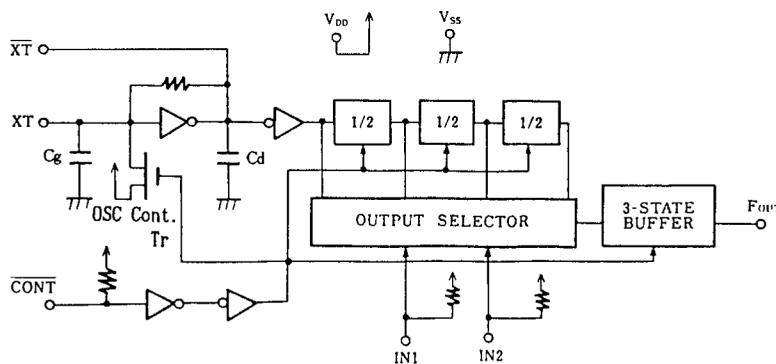
Unit: μ m

No.	PAD	X	Y
1	FOUT	165	651
2	IN2	165	484
3	IN1	165	317
4	V _{ss}	165	149
5	CONT	1113	149
6	XT	1113	317
7	XT	1113	484
8	V _{dd}	1113	651

Chip Size : 1.28 X 0.8mm

Chip Thickness : 400 μ m \pm 30 μ m

■ BLOCK DIAGRAM



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■ TERMINAL DESCRIPTION

NO.	SYMBOL	FUNCTION															
		Oscillation Stop Control and Divider Reset															
5	CONT	<table border="1"> <tr> <td>CONT</td> <td></td> <td>F_{OUT}</td> </tr> <tr> <td>H</td> <td></td> <td>Output either one frequency from f₀, f₀/2, f₀/4, and f₀/8</td> </tr> <tr> <td>L</td> <td></td> <td>Oscillation Stop, Output High Impedance and Divider Reset</td> </tr> </table>	CONT		F _{OUT}	H		Output either one frequency from f ₀ , f ₀ /2, f ₀ /4, and f ₀ /8	L		Oscillation Stop, Output High Impedance and Divider Reset						
CONT		F _{OUT}															
H		Output either one frequency from f ₀ , f ₀ /2, f ₀ /4, and f ₀ /8															
L		Oscillation Stop, Output High Impedance and Divider Reset															
6	XT	Quartz Crystal Connecting Terminals															
7	XT																
8	V _{DD}	+ 5V															
3	IN1	3-Stage Divider Outputs Selected by IN1 and IN2															
2	IN2	<table border="1"> <tr> <th>IN1</th> <th>IN2</th> <th>F_{OUT}</th> </tr> <tr> <td>H</td> <td>H</td> <td>f₀</td> </tr> <tr> <td>L</td> <td>H</td> <td>f₀/2</td> </tr> <tr> <td>H</td> <td>L</td> <td>f₀/4</td> </tr> <tr> <td>L</td> <td>L</td> <td>f₀/8</td> </tr> </table>	IN1	IN2	F _{OUT}	H	H	f ₀	L	H	f ₀ /2	H	L	f ₀ /4	L	L	f ₀ /8
IN1	IN2	F _{OUT}															
H	H	f ₀															
L	H	f ₀ /2															
H	L	f ₀ /4															
L	L	f ₀ /8															
1	F _{OUT}	Output either one frequency from f ₀ , f ₀ /2, f ₀ /4, and f ₀ /8															
4	V _{SS}	GND															

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

P A R A M E T E R	S Y M B O L	R A T I N G S	U N I T
Supply Voltage	V _{DD}	-0.5 ~ +7.0	V
Input Voltage	V _{IN}	-0.5 ~ V _{DD} +0.5	V
Output Voltage	V _O	-0.5 ~ V _{DD} +0.5	V
Input Current	I _{IN}	±10	mA
Output Current	I _O	±25	mA
Power Dissipation (EMD)	P _D	200	mW
Operating Temperature Range	T _{OPR}	-40 ~ + 85	°C
Storage Temperature Range	T _{STG}	-65 ~ +150	°C

(Note) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

■ ELECTRICAL CHARACTERISTICS

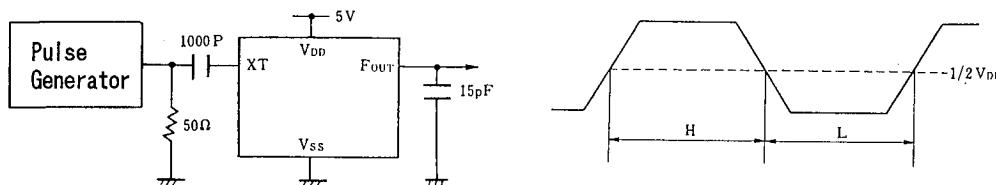
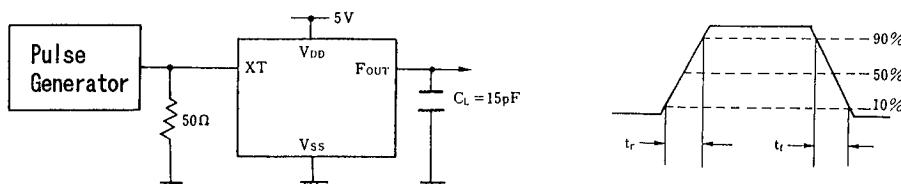
(Ta=25°C, V_{DD}=5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V _{DD}		3		6	V
Operating Current	I _{DD}	f _{osc} =16MHz, No load			10	mA
Stand-by Current	I _{ST}	CONT, XT=V _{SS} , No load (Note)			1	μA
Input Voltage	V _{IH}		3.5		5.0	V
	V _{IL}		0		1.5	
Output Current	I _{OH}	V _{DD} =5V, V _{OH} =4.5V	4			mA
	I _{OL}	V _{DD} =5V, V _{OL} =0.5V	4			
Input Current	I _{IN}	CONT, IN1, IN2 Terminals CONT, IN1, IN2=V _{SS}			400	μA
Internal Capacitor	C _g	Refer to Line-Up Table.				pF
	C _d					
Max. Oscillation Freq.	f _{MAX}	V _{DD} =5V, C _L =15pF	50			MHz
Output Signal Symmetry	SYM	V _{DD} =5V, C _L =15pF at 1/2V _{DD}	45	50	55	%
Output Signal Rise Time	t _r	V _{DD} =5V, C _L =15pF, 10% - 90%			8	ns
Output Signal Fall Time	t _f	V _{DD} =5V, C _L =15pF, 90% - 10%			8	ns

Note) Excluding input current on CONT terminal.

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■ MEASUREMENT CIRCUITS

(1) Output Signal Symmetry (C_L=15pF)(2) Output Signal Rise/Fall Time (C_L=15pF)

NJU6323 Series

MEMO

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