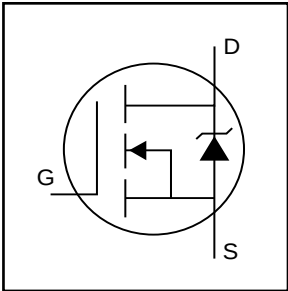


- Logic-Level Gate Drive
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

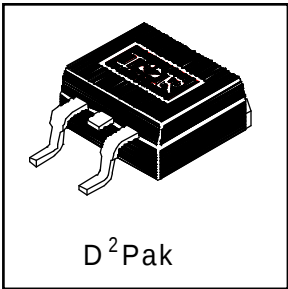
The D²PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



$V_{DS} = 30V$

$R_{DS(on)} = 0.04\Omega$

$I_D = 24A$



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V⑤	24	A
I_D @ $T_C = 100^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V⑤	17	
I_{DM}	Pulsed Drain Current ①	96	
P_D @ $T_C = 25^{\circ}C$	Power Dissipation	45	W
	Linear Derating Factor	0.30	W/°C
V_{GS}	Gate-to-Source Voltage	±16	V
E_{AS}	Single Pulse Avalanche Energy ②⑤	77	mJ
I_{AR}	Avalanche Current①	14	A
E_{AR}	Repetitive Avalanche Energy①	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	3.5	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

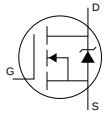
	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady-state)**	—	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.030	—	V/°C	Reference to 25°C, I _D = 1mA⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.040 0.060	Ω	V _{GS} = 10V, I _D = 14A ④ V _{GS} = 4.5V, I _D = 12A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	—	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	6.4	—	—	S	V _{DS} = 25V, I _D = 14A ⑤
I _{DSS}	Drain-to-Source Leakage Current	—	—	25 250	μA	V _{DS} = 30V, V _{GS} = 0V V _{DS} = 24V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V _{GS} = -16V
Q _g	Total Gate Charge	—	—	15	nC	I _D = 14A
Q _{gs}	Gate-to-Source Charge	—	—	4.6	nC	V _{DS} = 24V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	9.3	nC	V _{GS} = 4.5V, See Fig. 6 and 13 ④⑤
t _{d(on)}	Turn-On Delay Time	—	8.5	—	ns	V _{DD} = 15V
t _r	Rise Time	—	140	—		I _D = 14A
t _{d(off)}	Turn-Off Delay Time	—	12	—		R _G = 12Ω, V _{GS} = 4.5V
t _f	Fall Time	—	20	—		R _D = 1.0Ω, See Fig. 10 ④⑤
L _S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C _{iss}	Input Capacitance	—	450	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	210	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	110	—		f = 1.0MHz, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	24	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	96		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 14A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	65	97	ns	T _J = 25°C, I _F = 14A
Q _{rr}	Reverse Recovery Charge	—	140	210	nC	di/dt = 100A/μs ④⑤
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 15V, starting T_J = 25°C, L = 570μH
R_G = 25Ω, I_{AS} = 14A. (See Figure 12)

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

③ I_{SD} ≤ 14A, di/dt ≤ 140A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ Uses IRL2703 data and test conditions.

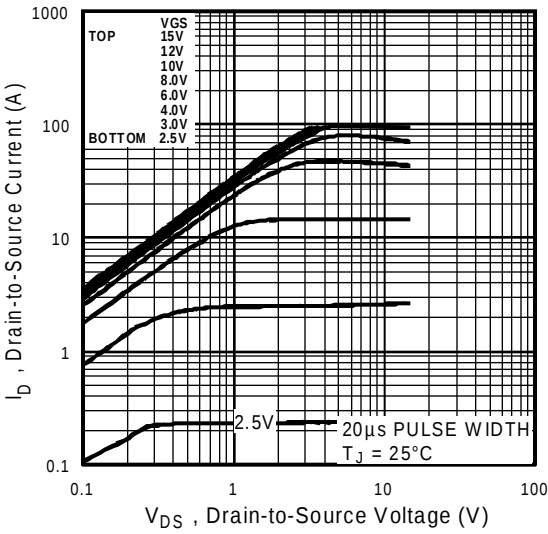


Fig 1. Typical Output Characteristics

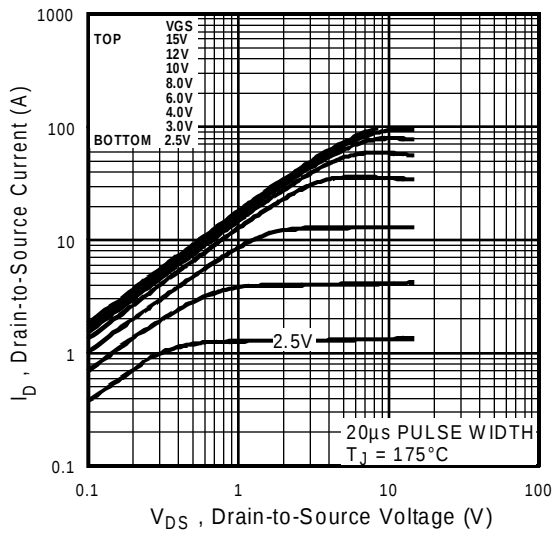


Fig 2. Typical Output Characteristics

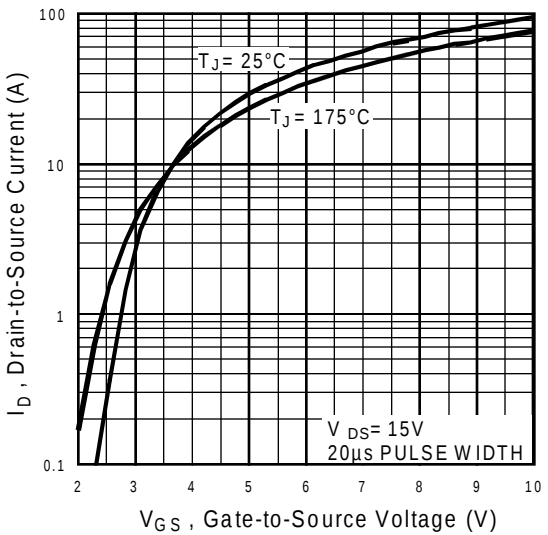


Fig 3. Typical Transfer Characteristics

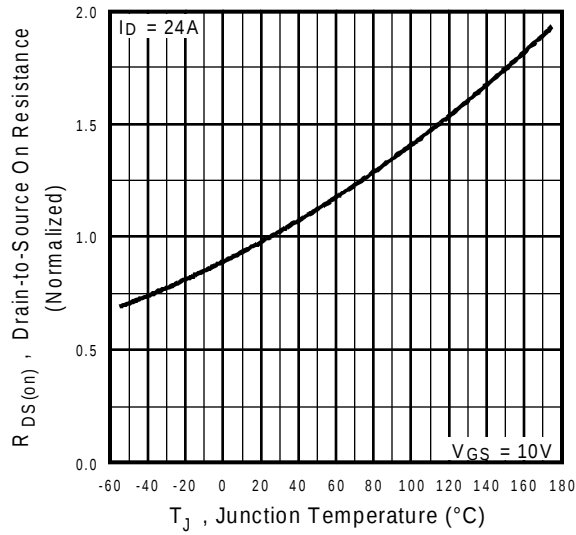


Fig 4. Normalized On-Resistance
Vs. Temperature

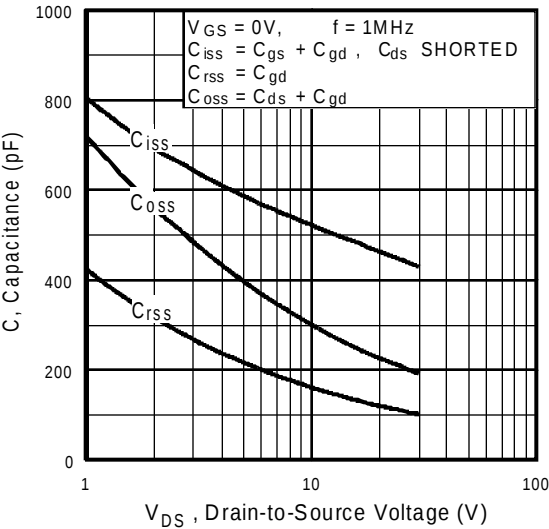


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

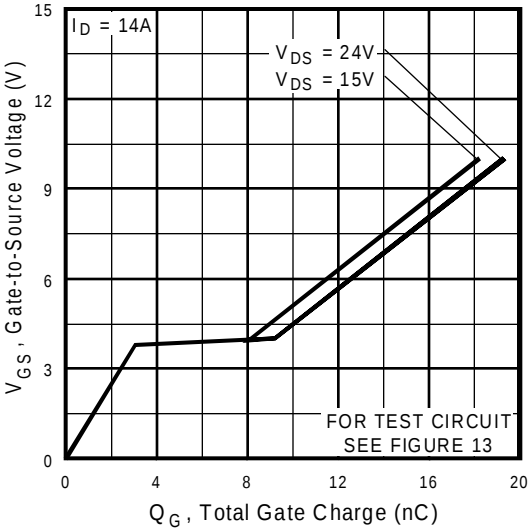


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

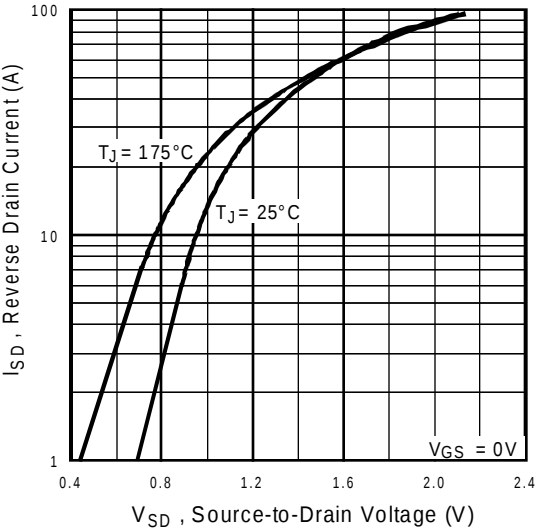


Fig 7. Typical Source-Drain Diode Forward Voltage

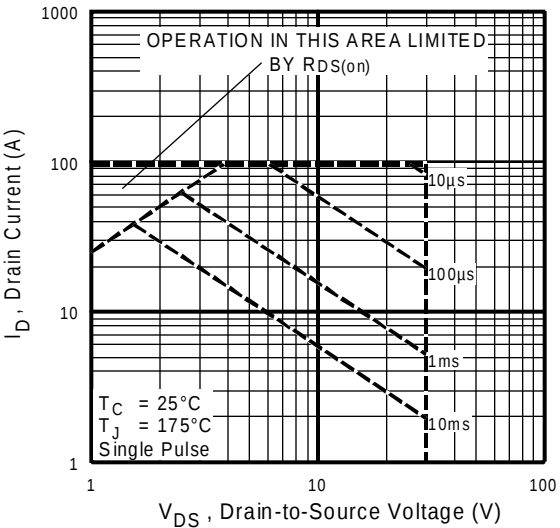


Fig 8. Maximum Safe Operating Area

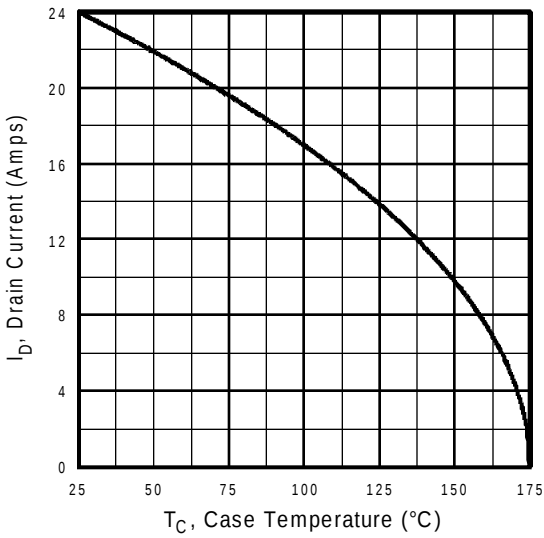


Fig 9. Maximum Drain Current Vs. Case Temperature

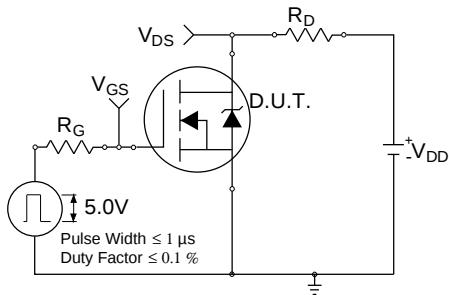


Fig 10a. Switching Time Test Circuit

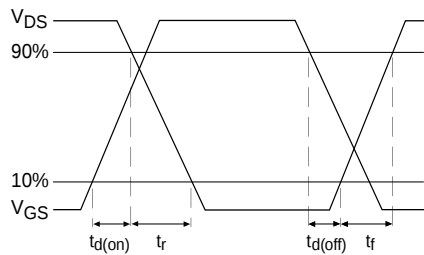


Fig 10b. Switching Time Waveforms

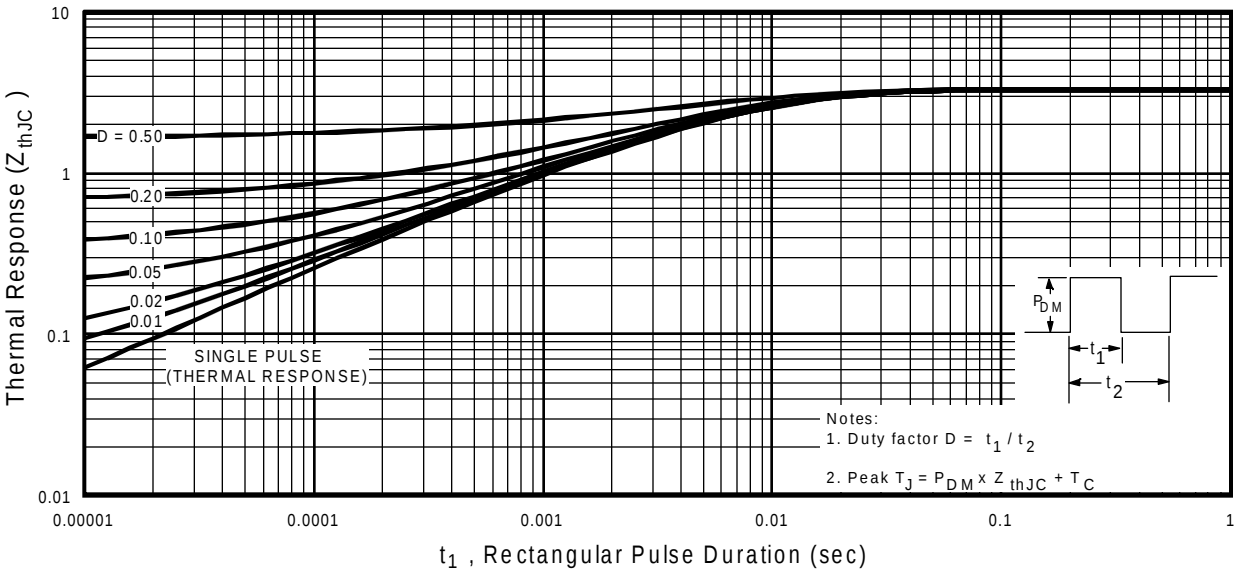


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

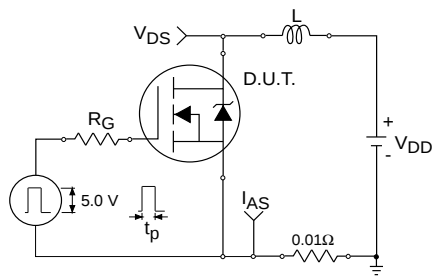


Fig 12a. Unclamped Inductive Test Circuit

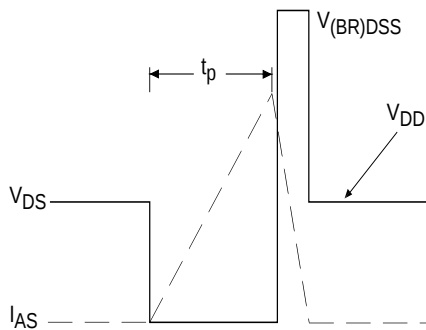


Fig 12b. Unclamped Inductive Waveforms

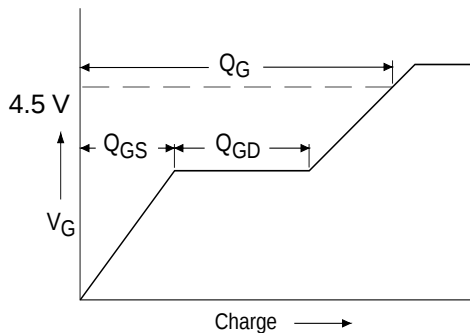


Fig 13a. Basic Gate Charge Waveform

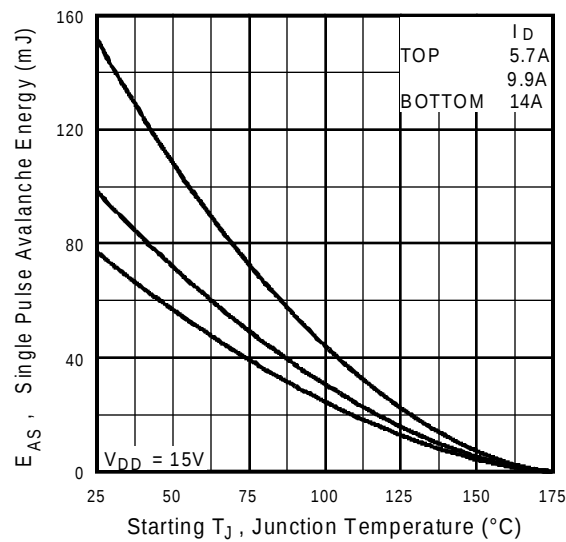


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

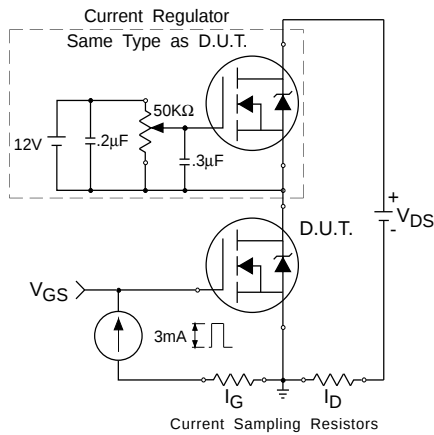
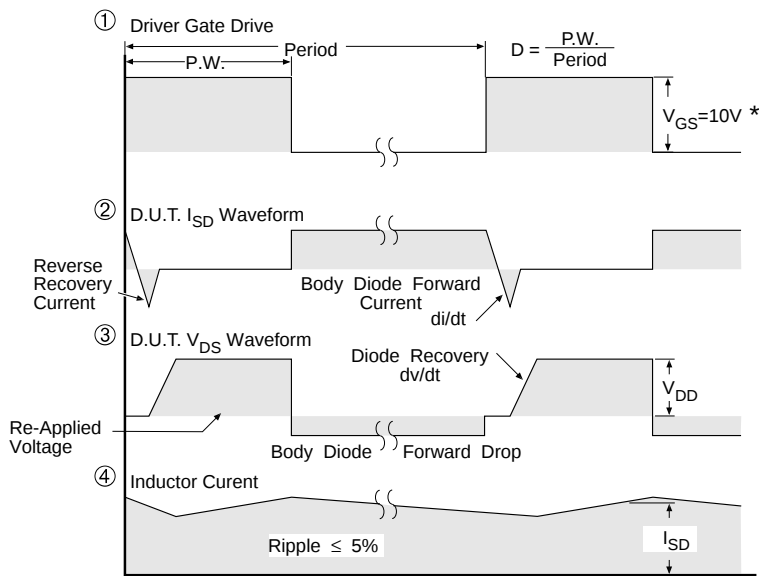
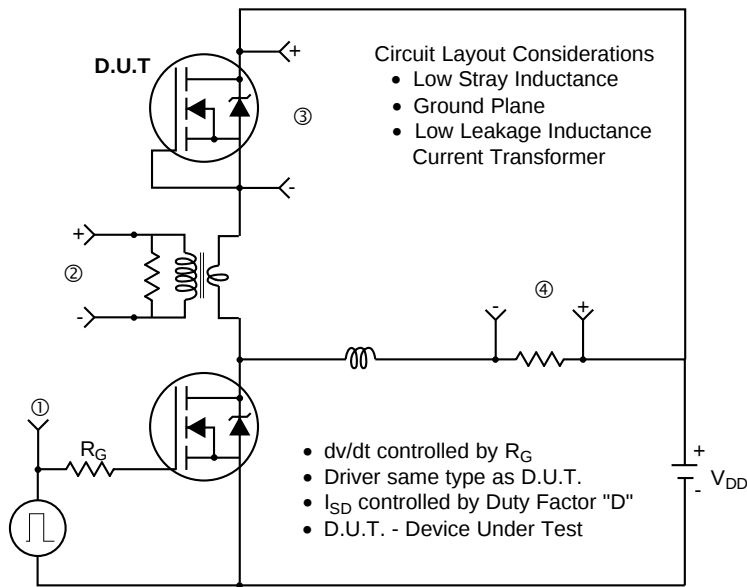


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



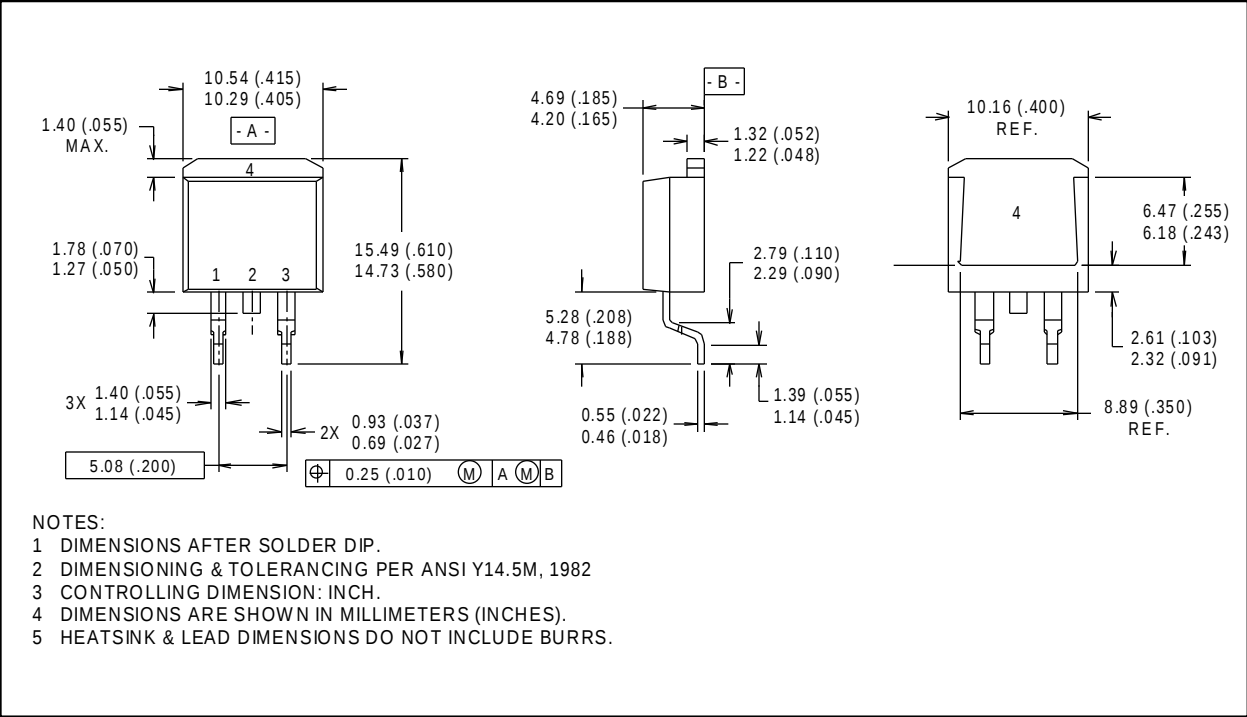
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

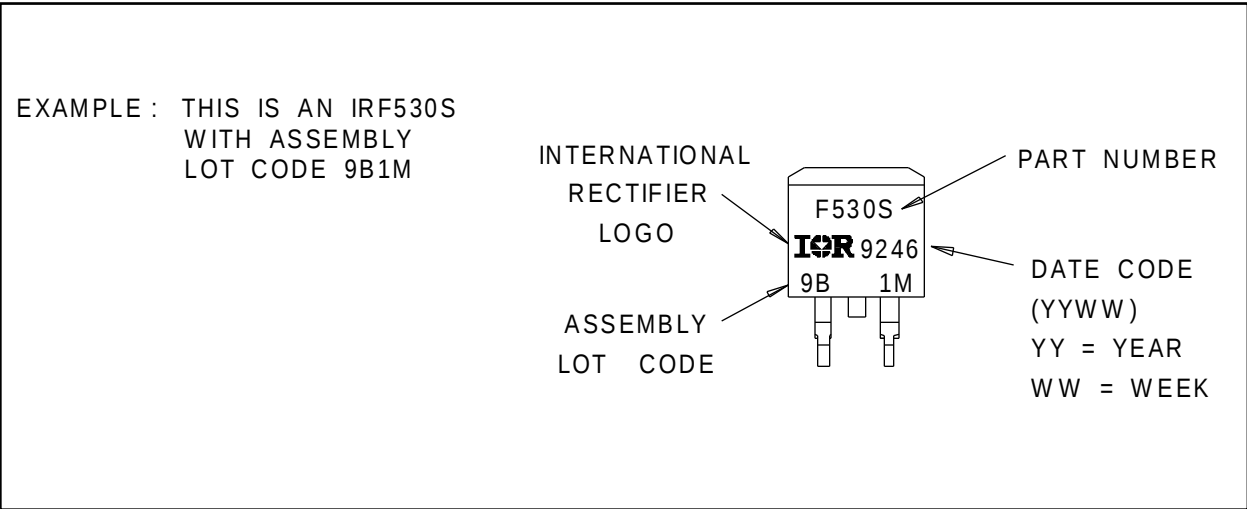
D²Pak Outline

Dimensions are shown in millimeters (inches)



Part Marking Information

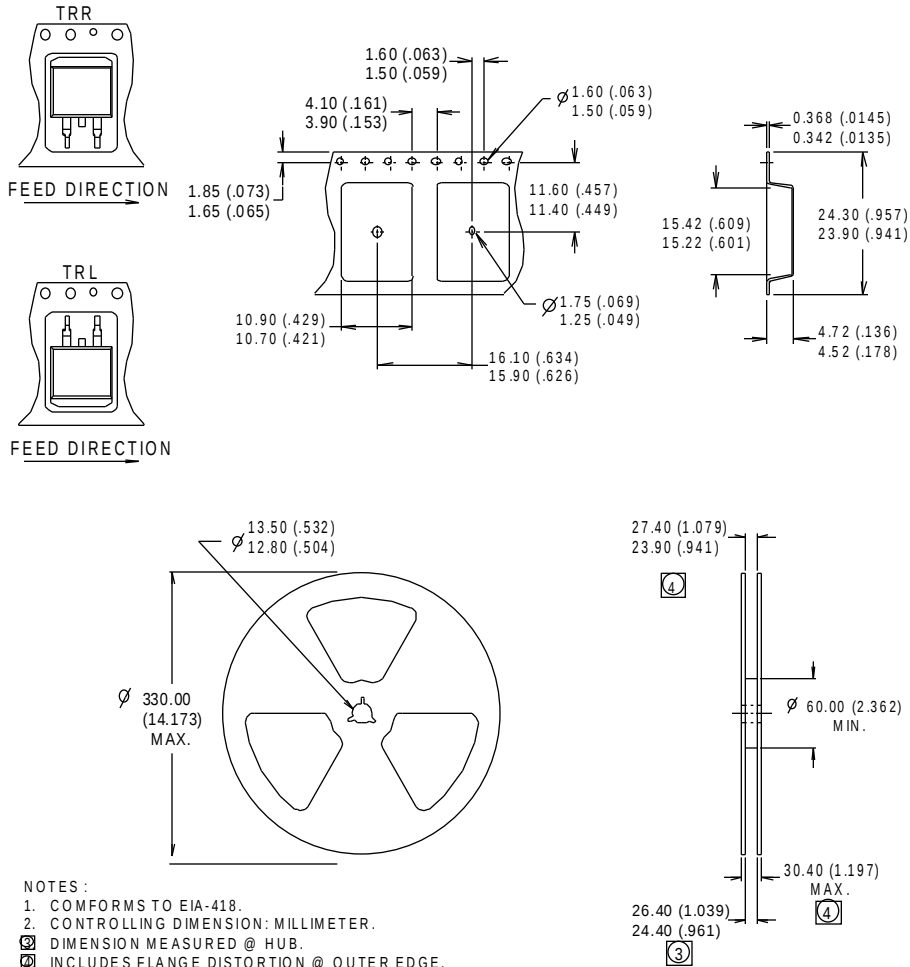
D²Pak



Tape & Reel Information

D²Pak

Dimensions are shown in millimeters (inches)



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Data and specifications subject to change without notice.

11/96

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>