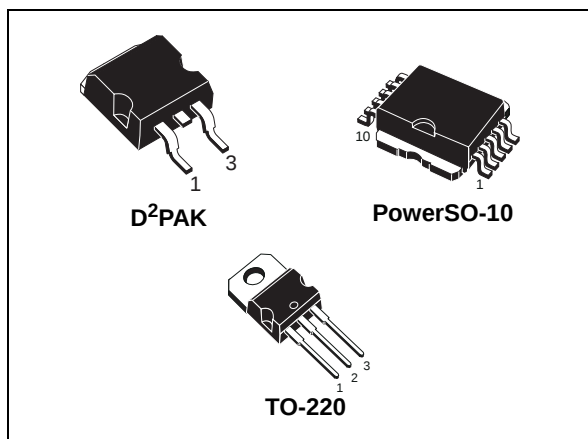




- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET

Description

The VNB35NV04-E, VNP35NV04-E and VNV35NV04-E are monolithic devices designed in STMicroelectronics® VIPower® M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 25 kHz applications.

Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments. Fault feedback can be detected by monitoring the voltage at the input pin.

Features

Type	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNB35NV04-E VNP35NV04-E VNV35NV04-E	10 mΩ ⁽¹⁾	30 A	40 V

1. For PowerSO-10 only

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
D²PAK	VNB35NV04-E	VNB35NV04TR-E
TO-220	VNP35NV04-E	—
PowerSO-10	VNV35NV04-E	VNV35NV04TR-E

Contents

1	Block diagram and pin connection	5
2	Electrical specification	6
2.1	Absolute maximum ratings	6
2.2	Thermal data	7
2.3	Electrical characteristics	7
2.4	Protection features	9
2.5	Electrical characteristics curves	13
3	Package information	17
3.1	ECOPACK®	17
3.2	TO-220 mechanical data	17
3.3	PowerSO-10 mechanical data	19
3.4	D2PAK mechanical data	21
3.5	TO-220 packing information	23
3.6	PowerSO-10 packing information	24
3.7	D ² PAK packing information	25
4	Revision history	26

List of tables

Table 1.	Device summary	1
Table 2.	Absolute maximum ratings	6
Table 3.	Thermal data.	7
Table 4.	Off	7
Table 5.	On	7
Table 6.	Dynamic	8
Table 7.	Switching	8
Table 8.	Source drain diode	8
Table 9.	Protections ($-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise specified)	8
Table 10.	TO-220 mechanical data	17
Table 11.	PowerSO-10 mechanical data	19
Table 12.	D2PAK mechanical data.	21
Table 13.	Document revision history	26

List of figures

Figure 1.	Block diagram	5
Figure 2.	Pin connection	5
Figure 3.	Current and voltage conventions	6
Figure 4.	Switching time test circuit for resistive load	10
Figure 5.	Test circuit for diode recovery times	10
Figure 6.	Unclamped inductive load test circuits	11
Figure 7.	Unclamped inductive waveforms	11
Figure 8.	Input charge test circuit.	12
Figure 9.	Thermal impedance for TO-220	12
Figure 10.	Source-drain diode forward characteristics	13
Figure 11.	Static drain source on resistance	13
Figure 12.	PowerSO-10 static drain-source on resistance vs. input voltage	13
Figure 13.	D ² PAK and TO-220 static drain-source on resistance vs. input voltage.	13
Figure 14.	PowerSO-10 static drain-source on resistance vs. i_D	13
Figure 15.	D ² PAK and TO-220 static drain-source on resistance vs. i_D	13
Figure 16.	Transconductance	14
Figure 17.	Transfer characteristics	14
Figure 18.	Output characteristics	14
Figure 19.	Normalized on resistance vs. temperature	14
Figure 20.	Turn-on current slope, $V_{IN} = 5\text{ V}$	14
Figure 21.	Turn-on current slope, $V_{IN} = 3.5\text{ V}$	14
Figure 22.	Input voltage vs. input charge	15
Figure 23.	Turn off drain source voltage slope, $V_{IN} = 5\text{ V}$	15
Figure 24.	Turn off drain-source voltage slope, $V_{IN} = 3.5\text{ V}$	15
Figure 25.	Switching time resistive load (part 1)	15
Figure 26.	Switching time resistive load (part 2)	15
Figure 27.	Normalized input threshold voltage vs. temperature	15
Figure 28.	Current limit vs. junction temperature	16
Figure 29.	Step response current limit	16
Figure 30.	Derating curve	16
Figure 31.	TO-220 package dimensions	18
Figure 32.	PowerSO-10 package dimensions	20
Figure 33.	D2PAK package dimensions	22
Figure 34.	TO-220 tube shipment (no suffix)	23
Figure 35.	PowerSO-10 suggested pad layout	24
Figure 36.	Tube shipment (no suffix)	24
Figure 37.	Tape and reel shipment (suffix "13TR")	24
Figure 38.	D ² PAK footprint	25
Figure 39.	Tube shipment (no suffix)	25
Figure 40.	Tape and reel shipment (suffix "13TR")	25

1 Block diagram and pin connection

Figure 1. Block diagram

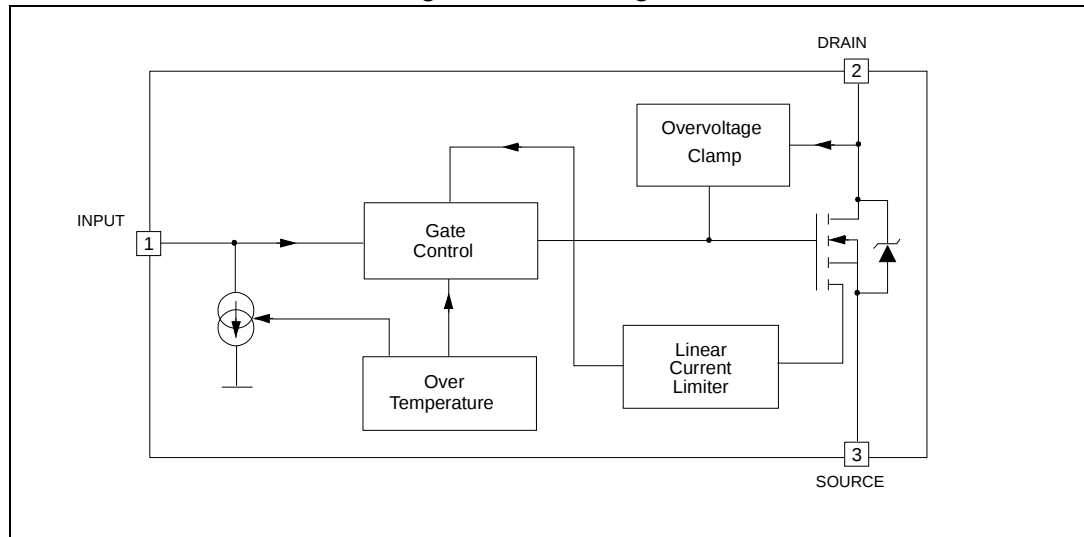
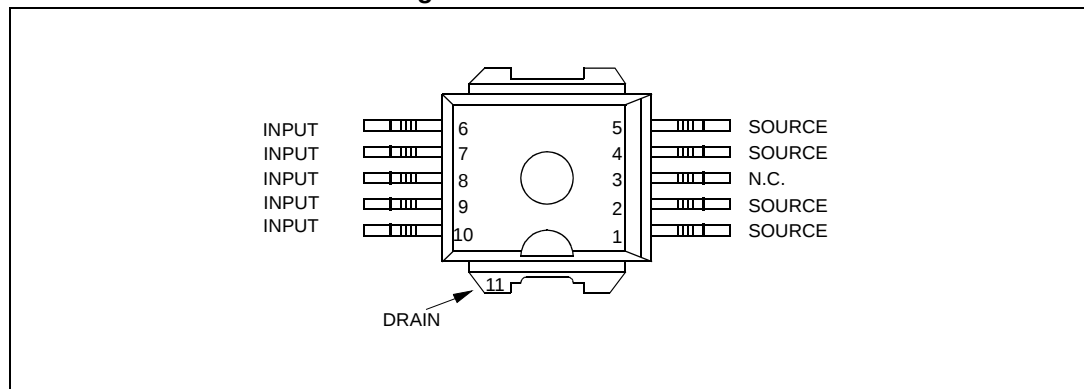


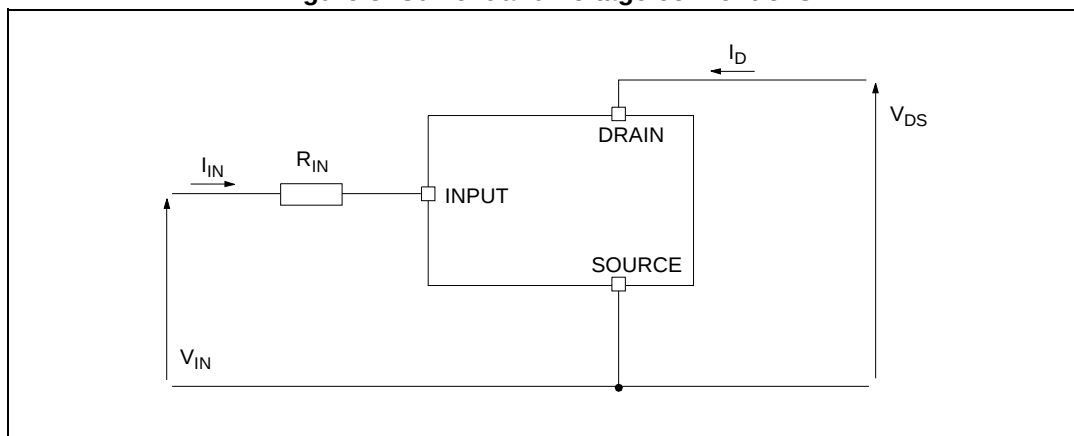
Figure 2. Pin connection



1. For the pins configuration related to TO-220, D²PAK, see [Figure 1](#).

2 Electrical specification

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		PowerSO-10	D ² PAK	TO-220	
V_{DS}	Drain-source voltage ($V_{IN} = 0$ V)	Internally clamped			V
V_{IN}	Input voltage	Internally clamped			V
I_{IN}	Input current	+/-20			mA
$R_{IN\ MIN}$	Minimum input series impedance	4.7			Ω
I_D	Drain current	Internally limited			A
I_R	Reverse DC output current	-30			A
V_{ESD1}	Electrostatic discharge ($R = 1.5$ K Ω , $C = 100$ pF)	4000			V
V_{ESD2}	Electrostatic discharge on output pin only ($R = 330$ Ω , $C = 150$ pF)	16500			V
P_{tot}	Total dissipation at $T_c = 25^\circ\text{C}$	125	125	125	W
T_j	Operating junction temperature	Internally limited			$^\circ\text{C}$
T_c	Case operating temperature	Internally limited			$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150			$^\circ\text{C}$

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		PowerSO-10	D ² PAK	TO-220	
R _{thj-case}	Thermal resistance junction-case (max)	1	1	1	°C/W
R _{thj-amb}	Thermal resistance junction-ambient (max)	50 ⁽¹⁾	50 ⁽¹⁾	50	°C/W

1. When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 mm thick) connected to all DRAIN pins.

2.3 Electrical characteristics

-40°C < T_j < 150°C, unless otherwise specified.

Table 4. Off

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V _{CLAMP}	Drain-source clamp voltage	V _{IN} = 0 V; I _D = 15 A	40	45	55	V
V _{CLTH}	Drain-source clamp threshold voltage	V _{IN} = 0 V; I _D = 2 mA	36			V
V _{INTH}	Input threshold voltage	V _{DS} = V _{IN} ; I _D = 1 mA	0.5		2.5	V
I _{ISS}	Supply current from input pin	V _{DS} = 0 V; V _{IN} = 5 V		100	150	μA
V _{INCL}	Input-source clamp voltage	I _{IN} = 1 mA	6	6.8	8	V
		I _{IN} = -1 mA	-1.0		-0.3	V
I _{DSS}	Zero input voltage drain current (V _{IN} = 0 V)	V _{DS} = 13 V; V _{IN} = 0 V; T _j = 25 °C			30	μA
		V _{DS} = 25 V; V _{IN} = 0 V			75	μA

Table 5. On

Symbol	Parameter	Test conditions	Max		Unit
			PowerSO-10	D ² PAK TO-220	
R _{DS(on)}	Static drain-source on resistance	V _{IN} = 5 V; I _D = 15 A; T _j = 25 °C	10	13	mΩ
		V _{IN} = 5 V; I _D = 15 A; T _j = 150 °C	20	24	mΩ

$T_j = 25^\circ\text{C}$, unless otherwise specified.

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DD} = 13\text{ V}; I_D = 15\text{ A}$	—	35	—	S
C_{OSS}	Output capacitance	$V_{DS} = 13\text{ V}; f = 1\text{ MHz}; V_{IN} = 0\text{ V}$	—	1300	—	pF

1. Pulsed: Pulse duration = 300 ms, duty cycle 1.5%

Table 7. Switching

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}; I_D = 15\text{ A};$ $V_{gen} = 5\text{ V};$ $R_{gen} = R_{IN\text{ MIN}} = 4.7\ \Omega$ (see Figure 3)	—	150	500	ns
t_r	Rise time		—	840	2500	ns
$t_{d(off)}$	Turn-off delay time		—	980	3000	ns
t_f	Fall time		—	600	1500	ns
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}; I_D = 15\text{ A};$ $V_{gen} = 5\text{ V}; R_{gen} = 2.2\text{ K}\Omega$ (see Figure 3)	—	4	12	μs
t_r	Rise time		—	27	100	μs
$t_{d(off)}$	Turn-off delay time		—	34	120	μs
t_f	Fall time		—	31	110	μs
$(di/dt)_{on}$	Turn-on current slope	$V_{DD} = 15\text{ V}; I_D = 15\text{ A}; V_{gen} = 5\text{ V};$ $R_{gen} = R_{IN\text{ MIN}} = 4.7\ \Omega$	—	18		A/ μs
Q_i	Total input charge	$V_{DD} = 12\text{ V}; I_D = 15\text{ A}; V_{IN} = 5\text{ V};$ $I_{gen} = 2.13\text{ mA}$ (see Figure 8)	—	118		nC

Table 8. Source drain diode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 15\text{ A}; V_{IN} = 0\text{ V}$	—	0.8	—	V
t_{rr}	Reverse recovery time	$I_{SD} = 15\text{ A}; di/dt = 100\text{ A}/\mu\text{s};$ $V_{DD} = 30\text{ V}; L = 200\ \mu\text{H}$ (see Figure 4)	—	400	—	ns
Q_{rr}	Reverse recovery charge		—	1.4	—	μC
I_{RRM}	Reverse recovery current		—	7	—	A

1. Pulsed: Pulse duration = 300 ms, duty cycle 1.5%

Table 9. Protections ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	Drain current limit	$V_{IN} = 6\text{ V}; V_{DS} = 13\text{ V}$	30	45	60	A
t_{dlim}	Step response current limit	$V_{IN} = 6\text{ V}; V_{DS} = 13\text{ V}$		50		μs

Table 9. Protections ($-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{jsh}	Overtemperature shutdown		150	175	200	$^{\circ}\text{C}$
T_{jrs}	Overtemperature reset		135			$^{\circ}\text{C}$
I_{gf}	Fault Sink Current	$V_{IN} = 5\text{ V}$; $V_{DS} = 13\text{ V}$; $T_j = T_{jsh}$	10	15	20	mA
E_{as}	Single pulse avalanche energy	Starting $T_j = 25^{\circ}\text{C}$; $V_{DD} = 24\text{ V}$; $V_{IN} = 5\text{ V}$; $R_{gen} = R_{IN\text{ MIN}} = 4.7\text{ }\Omega$; $L = 24\text{ mH}$ (see Figure 6 and Figure 7)	1.7			J

2.4 Protection features

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 25 KHz. The only difference from the user's standpoint is that a small DC current I_{ISS} (typ. 100 μA) flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

- **Overtoltage clamp protection:**
internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- **Linear current limiter circuit:**
limits the drain current I_D to I_{lim} whatever the INPUT pin voltages is. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .
- **Overtemperature and short circuit protection:**
these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overttemperature cutout occurs in the range 150°C to 190°C , a typical value being 170°C . The device is automatically restarted when the chip temperature falls of about 15°C below shutdown temperature.
- **Status feedback:**
in the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the INPUT pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the INPUT pin driver is not able to supply the current I_{gf} , the INPUT pin falls to 0 V. This does not however affect the device operation: no requirement is put on the current capability of the INPUT pin driver except to be able to supply the normal operation drive current I_{ISS} .

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

Figure 4. Switching time test circuit for resistive load

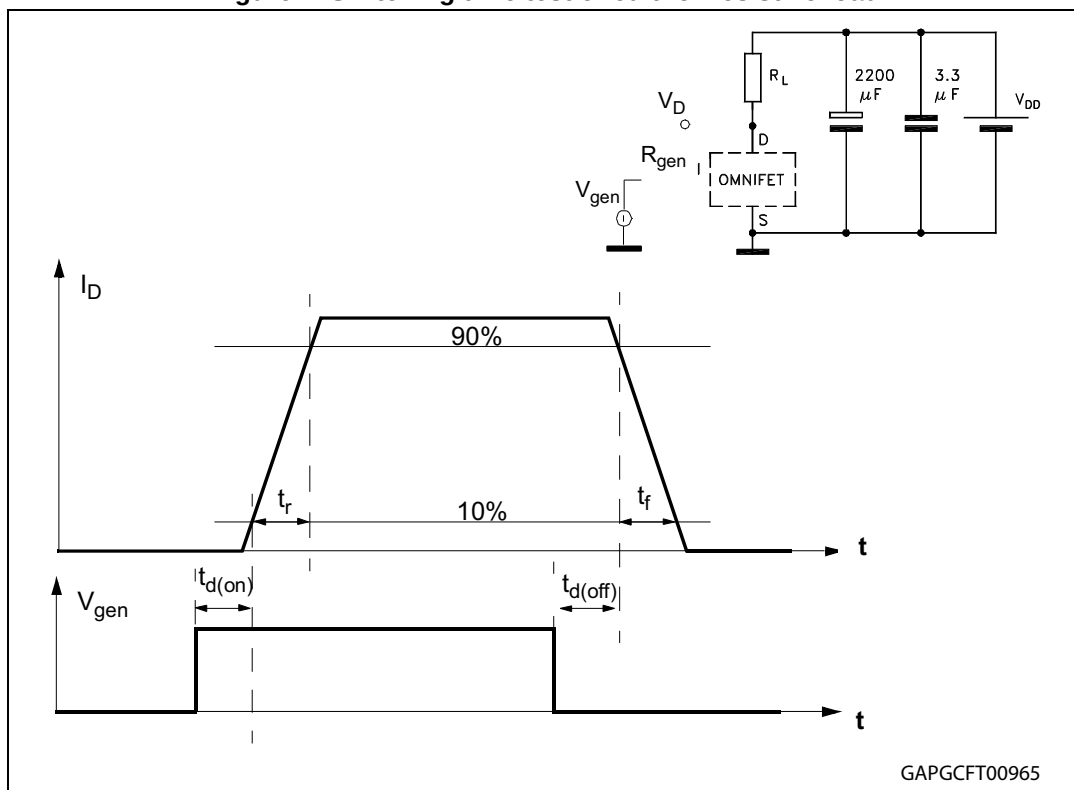


Figure 5. Test circuit for diode recovery times

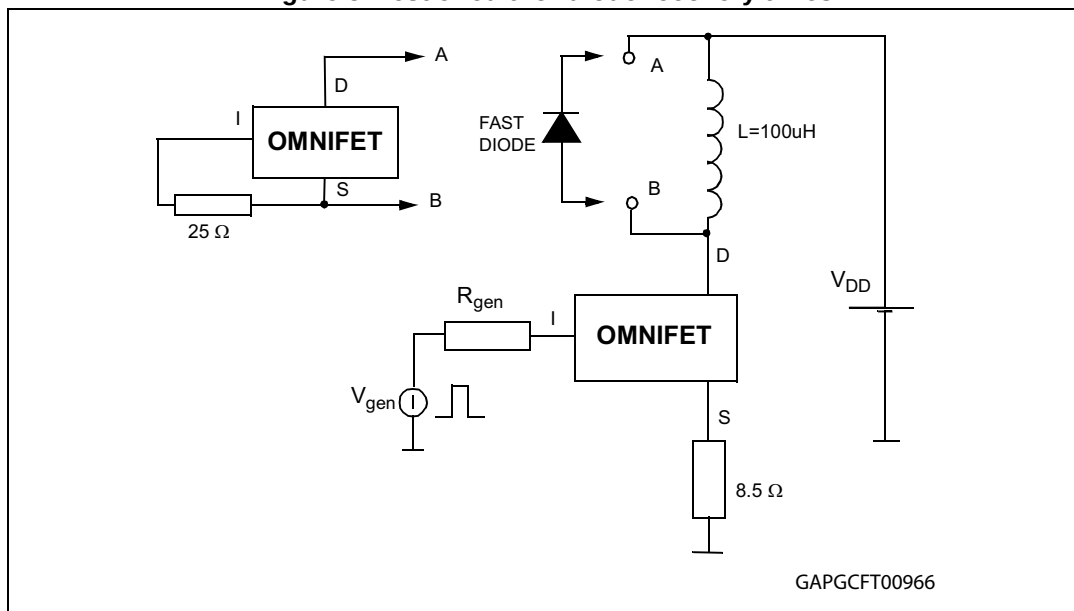


Figure 6. Unclamped inductive load test circuits

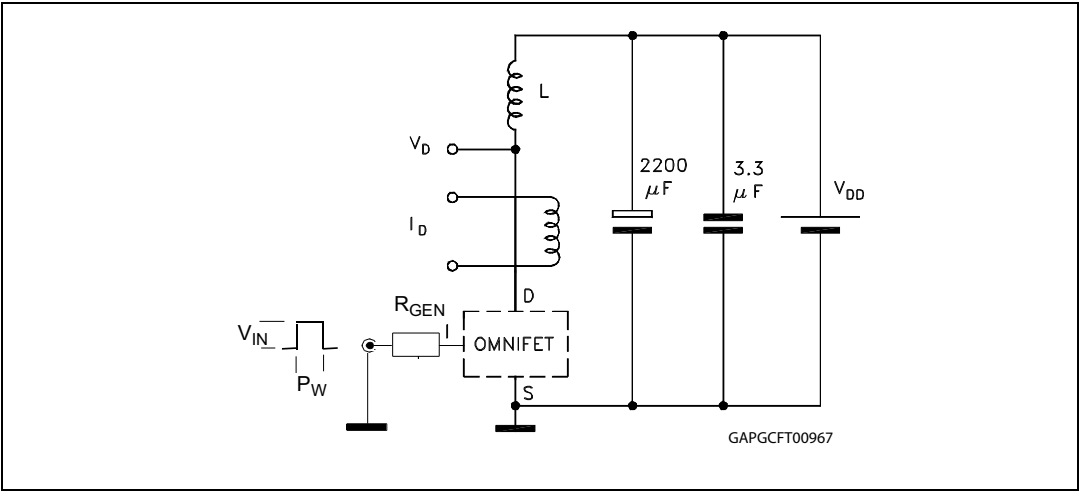


Figure 7. Unclamped inductive waveforms

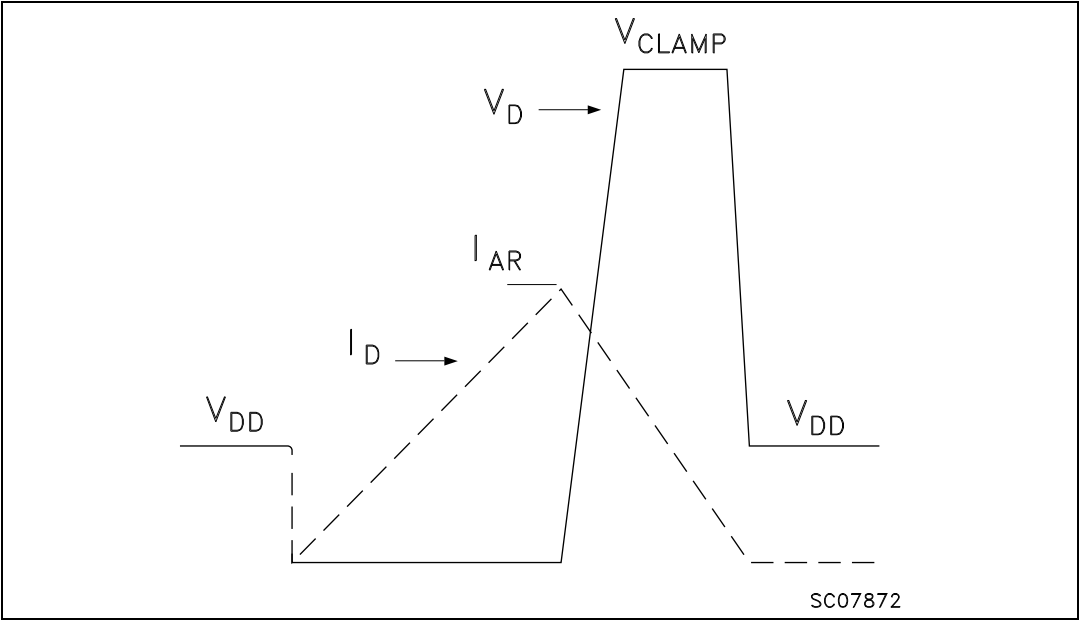


Figure 8. Input charge test circuit

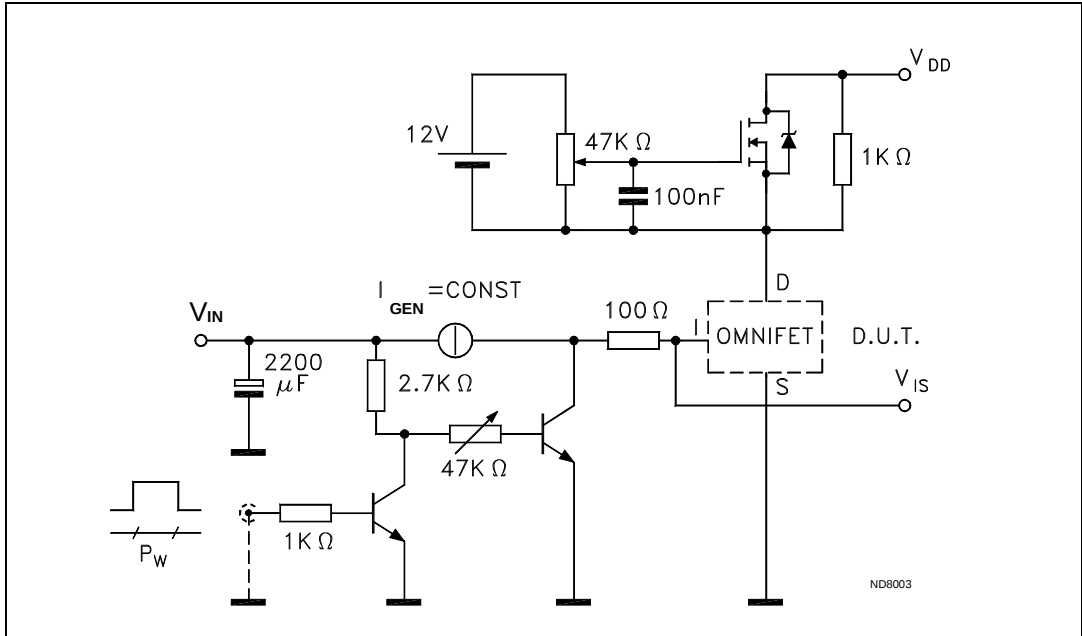
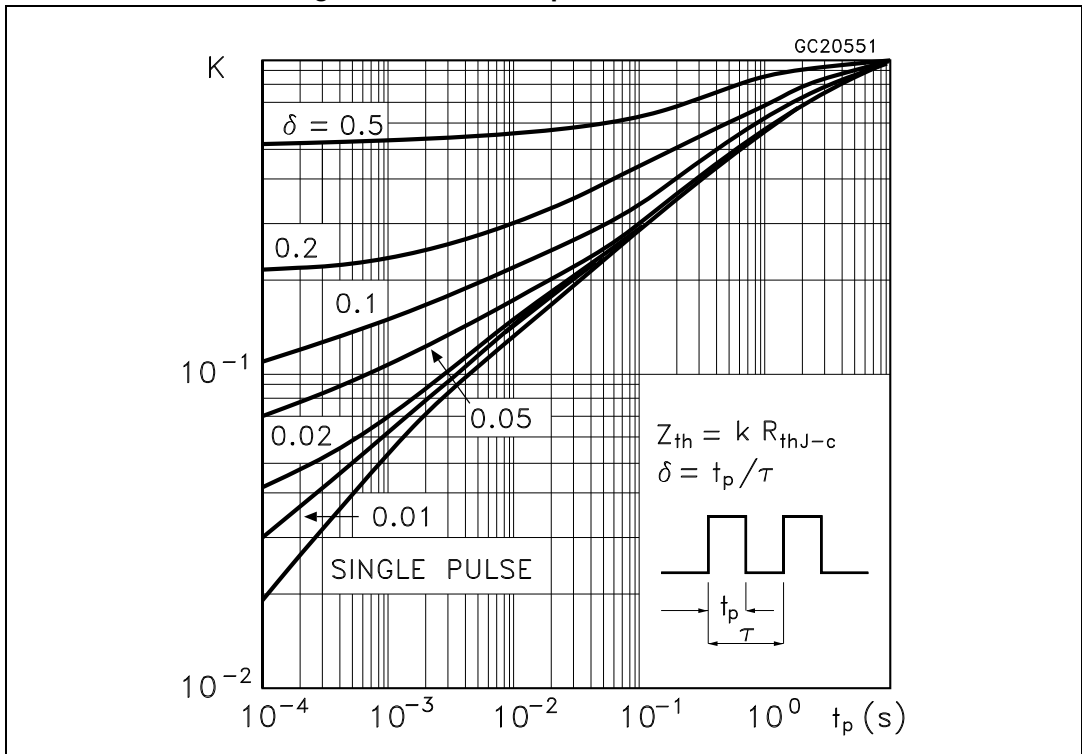


Figure 9. Thermal impedance for TO-220



2.5 Electrical characteristics curves

Figure 10. Source-drain diode forward characteristics

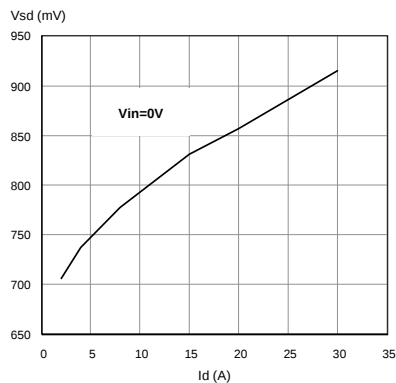


Figure 11. Static drain source on resistance

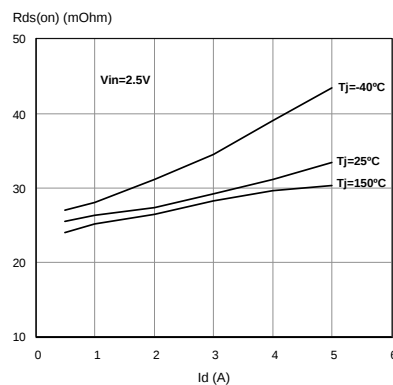


Figure 12. PowerSO-10 static drain-source on resistance vs. input voltage

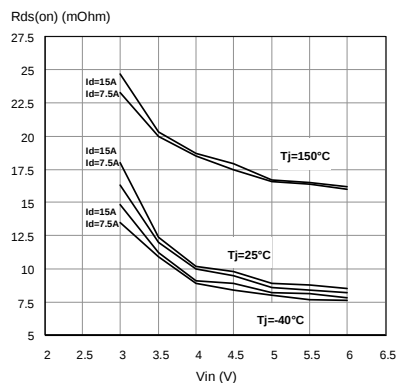


Figure 13. D²PAK and TO-220 static drain-source on resistance vs. input voltage

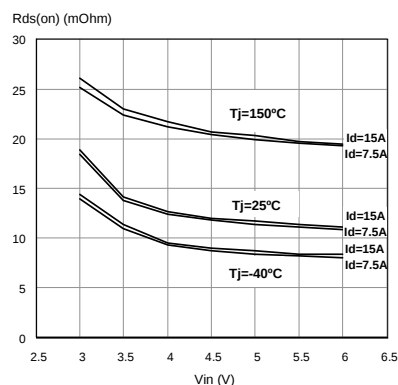


Figure 14. PowerSO-10 static drain-source on resistance vs. id

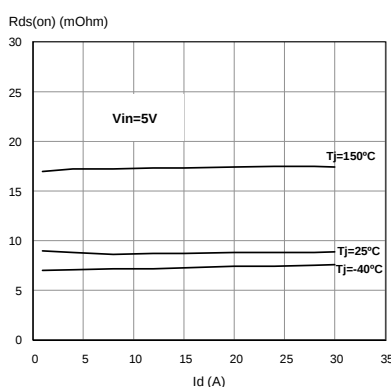


Figure 15. D²PAK and TO-220 static drain-source on resistance vs. id

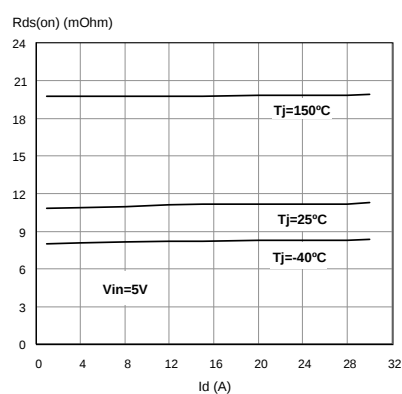


Figure 16. Transconductance

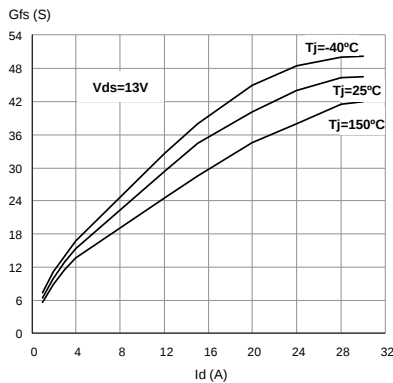


Figure 17. Transfer characteristics

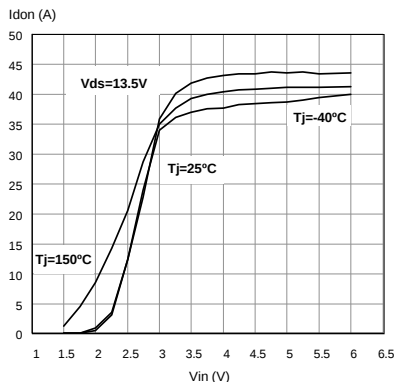


Figure 18. Output characteristics

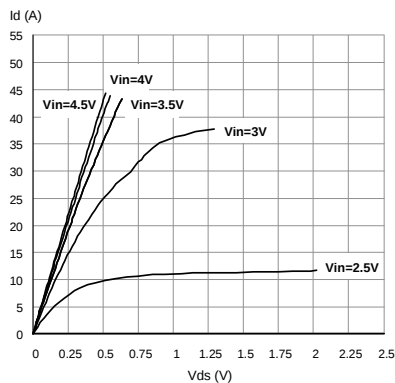


Figure 19. Normalized on resistance vs. temperature

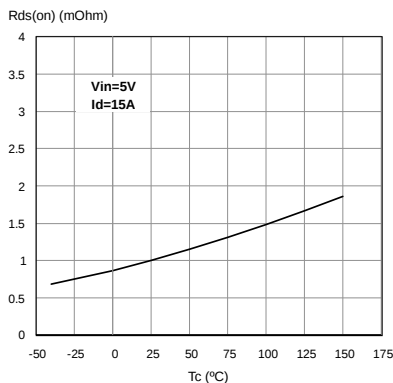


Figure 20. Turn-on current slope, $V_{IN} = 5\text{ V}$

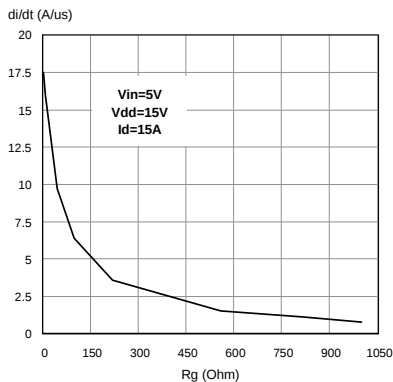


Figure 21. Turn-on current slope, $V_{IN} = 3.5\text{ V}$

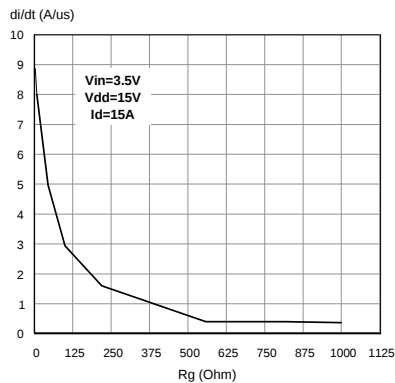


Figure 22. Input voltage vs. input charge

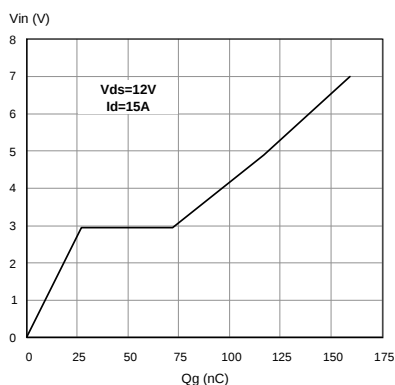
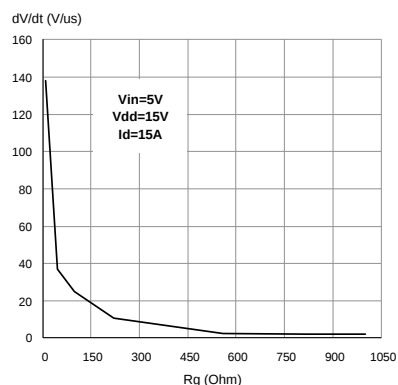
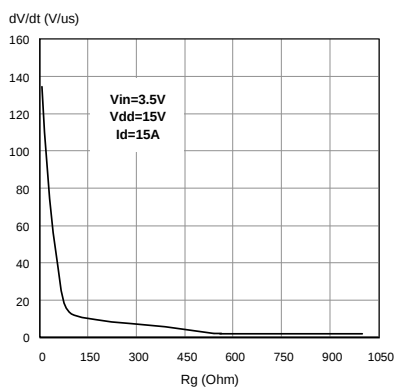
Figure 23. Turn off drain source voltage slope, $V_{IN} = 5 V$ Figure 24. Turn off drain-source voltage slope, $V_{IN} = 3.5 V$ 

Figure 25. Switching time resistive load (part 1)

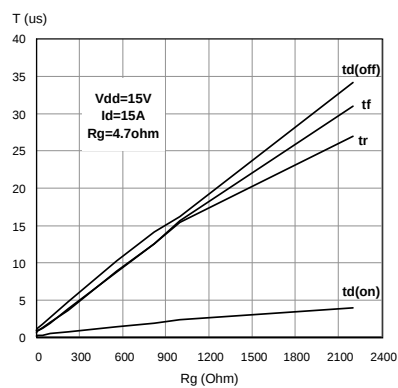


Figure 26. Switching time resistive load (part 2)

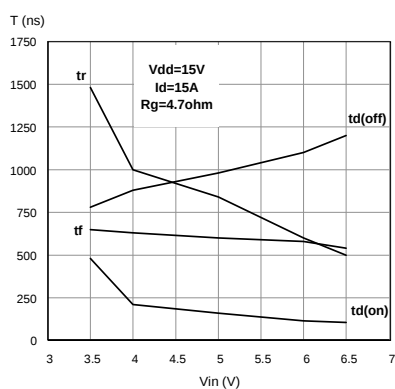


Figure 27. Normalized input threshold voltage vs. temperature

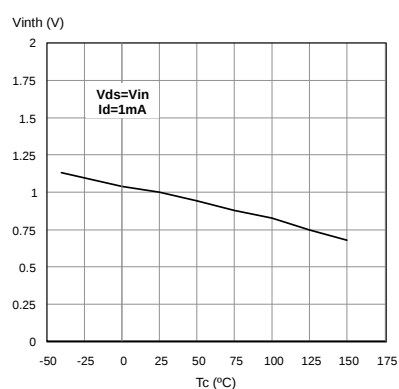


Figure 28. Current limit vs. junction temperature

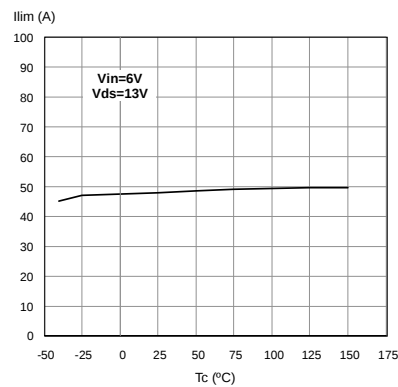


Figure 29. Step response current limit

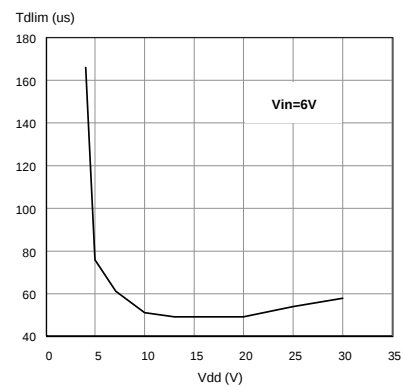
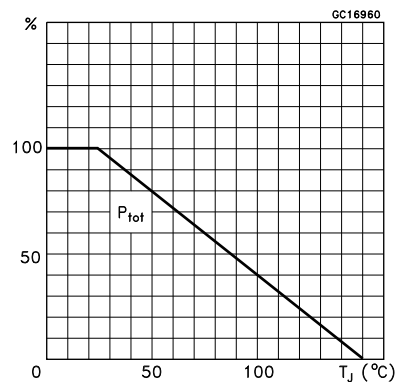


Figure 30. Derating curve



3 Package information

3.1 ECOPACK®

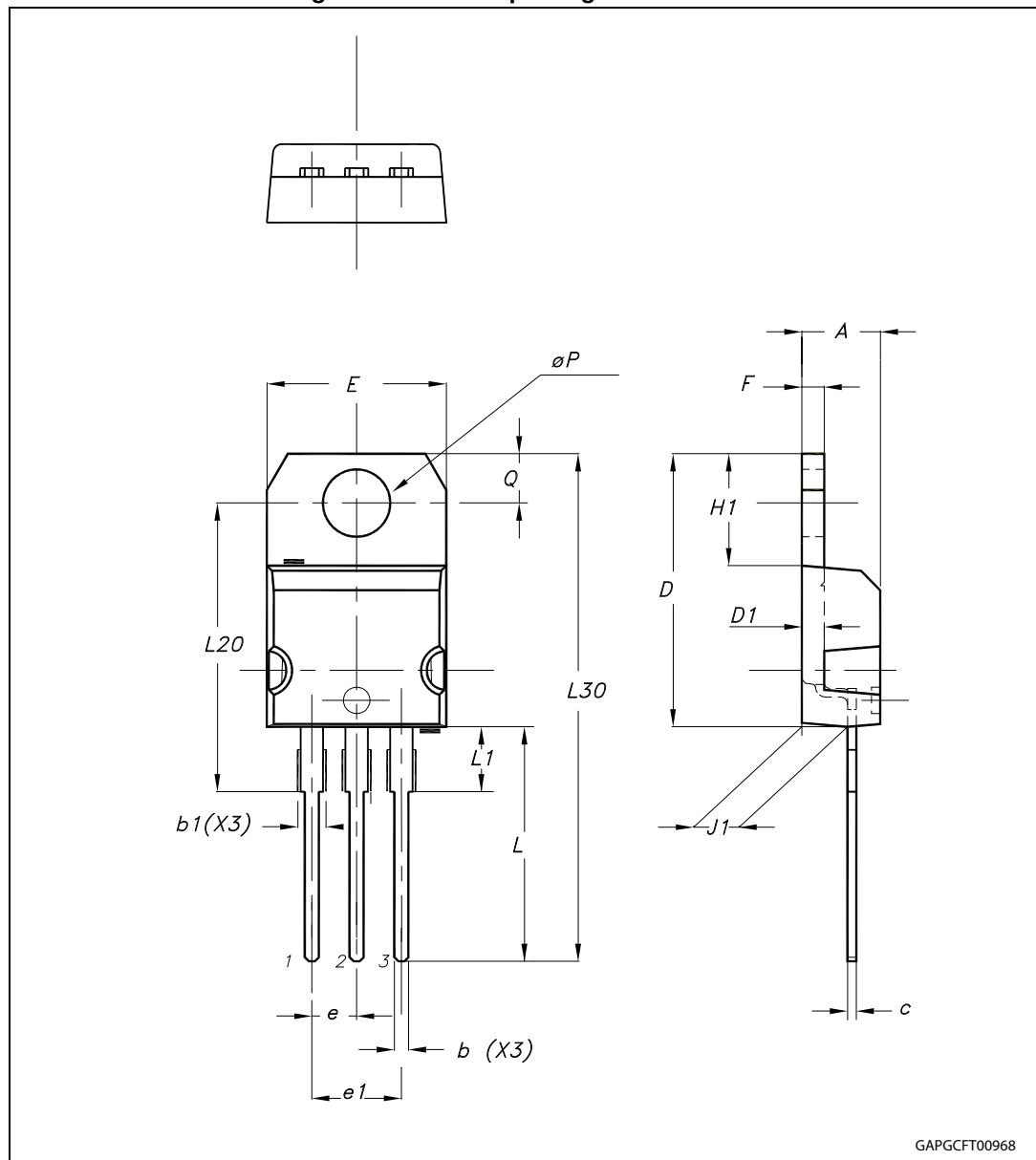
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

3.2 TO-220 mechanical data

Table 10. TO-220 mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95
Package weight	1.9Gr. (Typ.)		

Figure 31. TO-220 package dimensions



3.3 PowerSO-10 mechanical data

Table 11. PowerSO-10 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			3.70
A1	0.00		0.10
A2	3.40		3.60
A3	1.25		1.35
b	0.40		0.53
c	0.35		0.55
D	9.40		9.60
D1 ⁽¹⁾	7.40		7.60
E	13.80		14.40
E1 ⁽¹⁾	9.30		9.50
E2	7.20		7.60
E3	5.90		6.10
e		1.27	
L	0.95		1.65
<	0°		8°

1. Resin protrusion not included (max value: 0.20 mm per side)

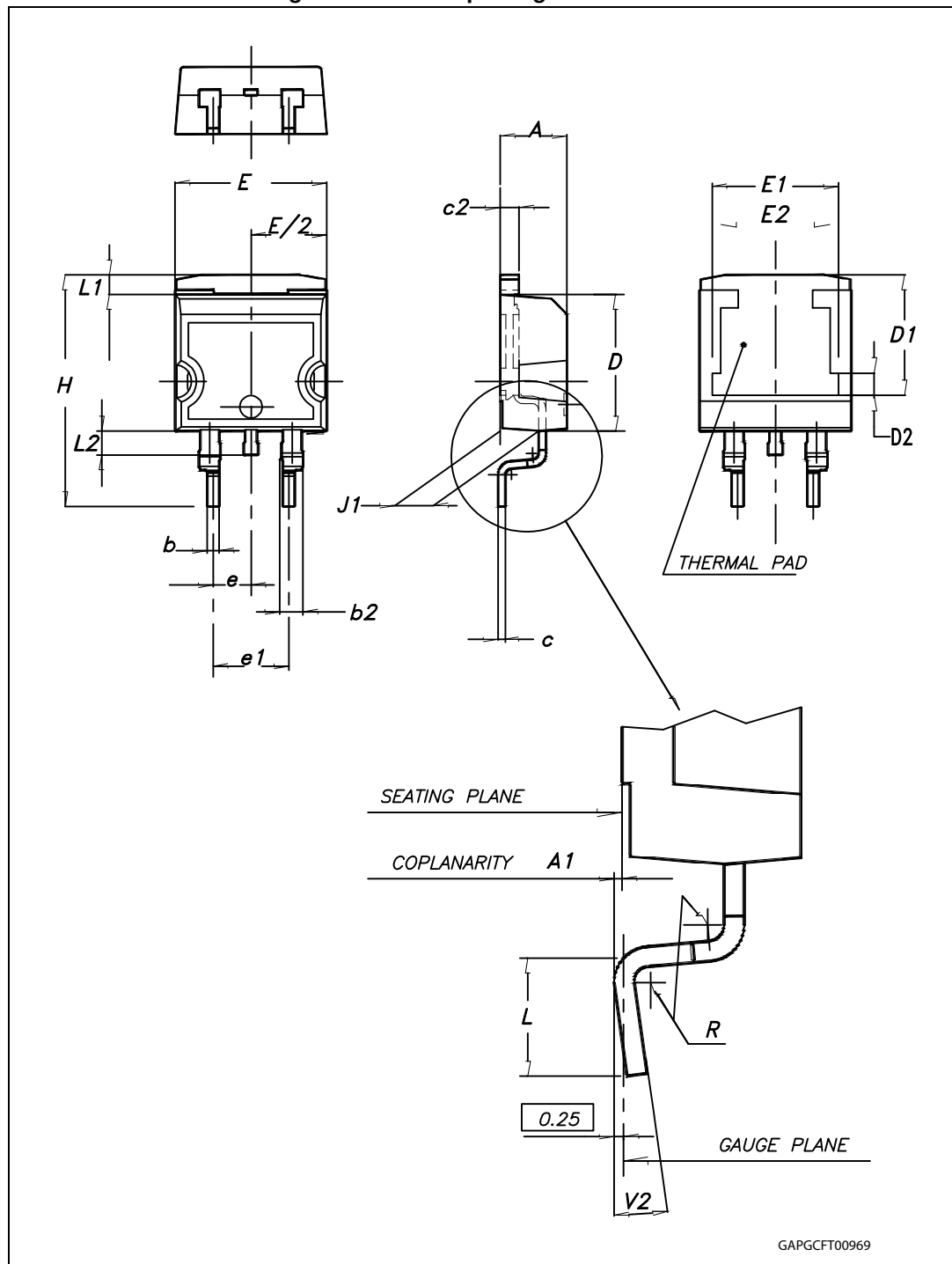
Figure 32. PowerSO-10 package dimensions



3.4 D²PAK mechanical data

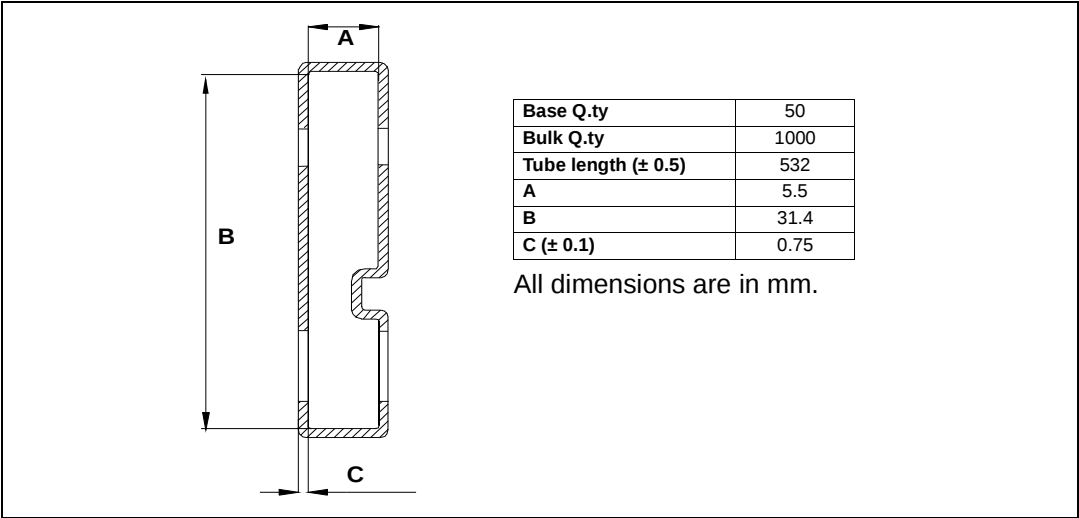
Table 12. D²PAK mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 33. D²PAK package dimensions

3.5 TO-220 packing information

Figure 34. TO-220 tube shipment (no suffix)



3.6 PowerSO-10 packing information

Figure 35. PowerSO-10 suggested pad layout

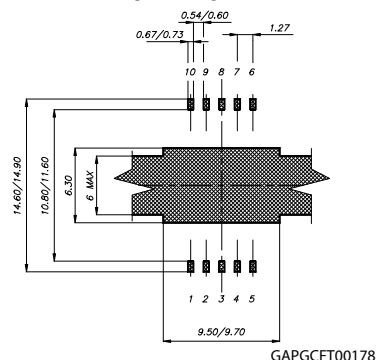
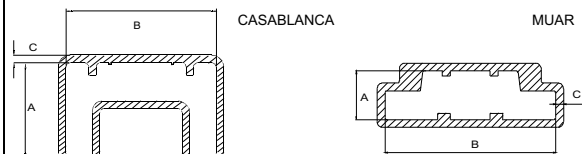


Figure 36. Tube shipment (no suffix)

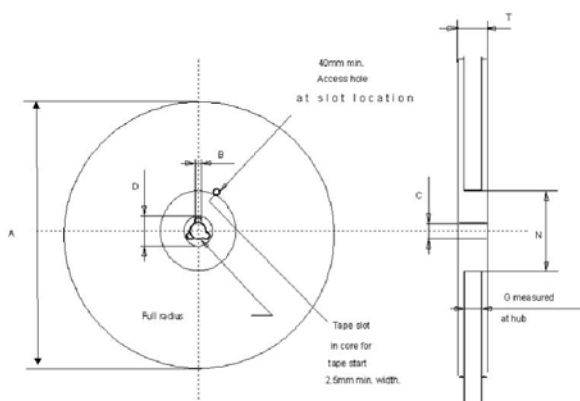


All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

GAPGCT00179

Figure 37. Tape and reel shipment (suffix "13TR")



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

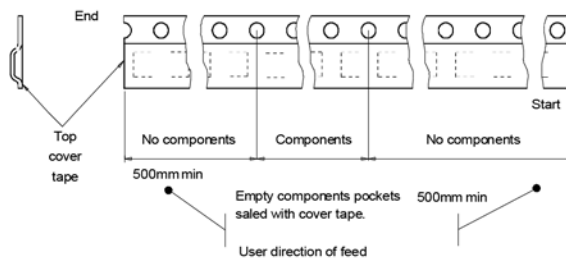
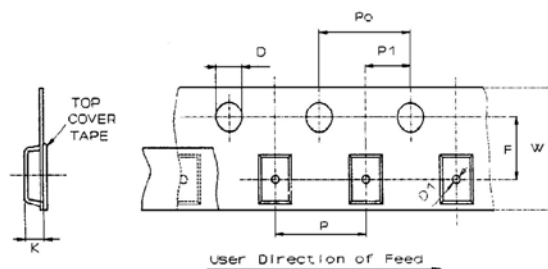
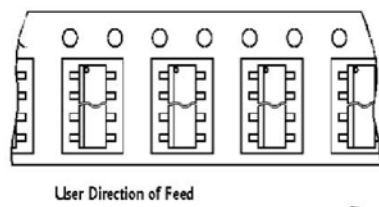
All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



GAPGCT00180

3.7 D²PAK packing information

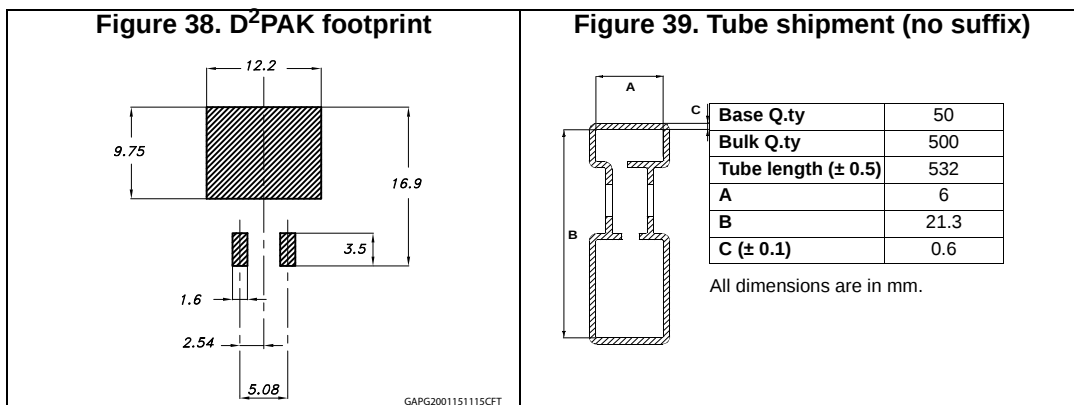
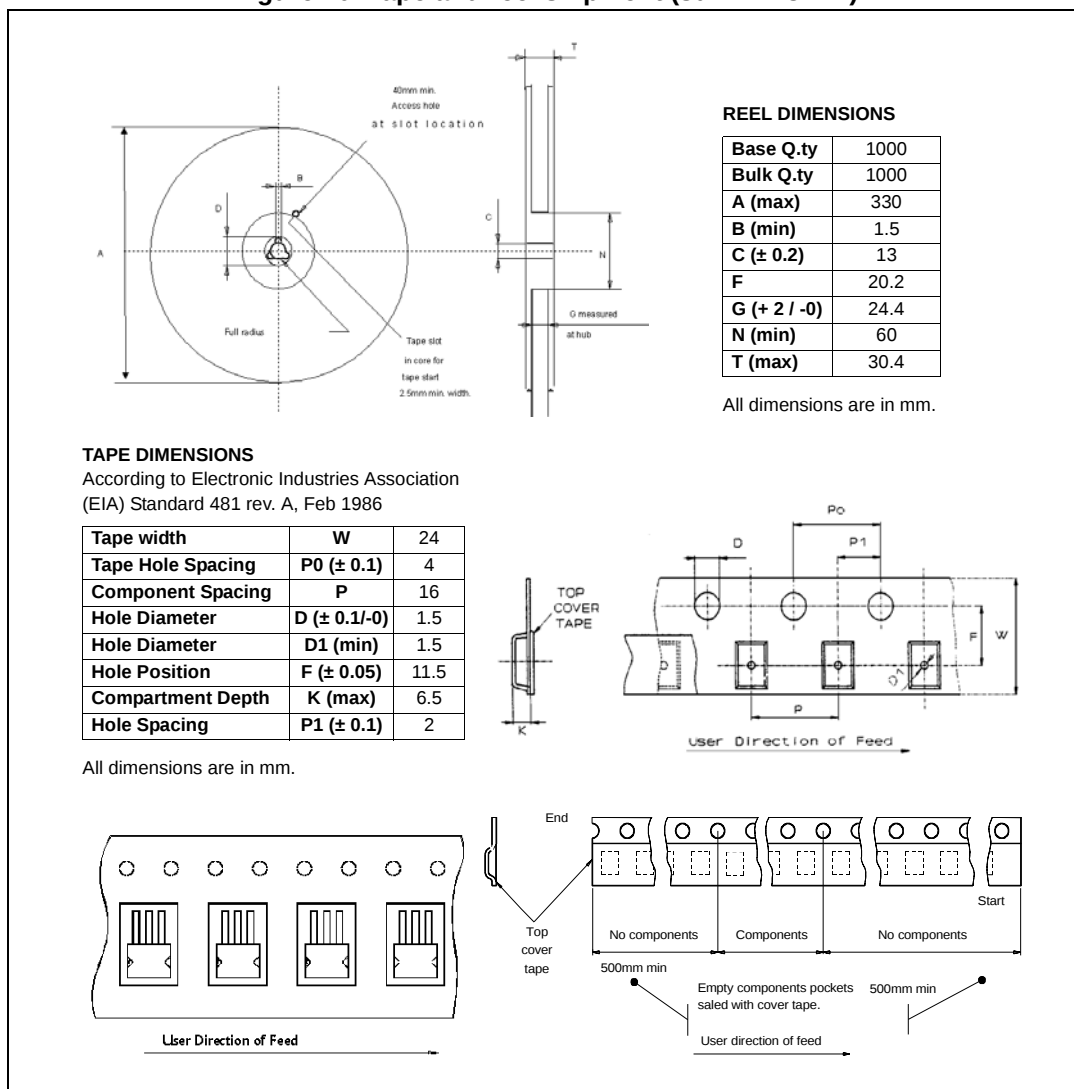


Figure 40. Tape and reel shipment (suffix "13TR")



4 Revision history

Table 13. Document revision history

Date	Revision	Changes
19-Sep-2012	1	Initial release.
25-Sep-2013	2	Updated disclaimer.
30-Sep-2013	3	Added Table 5: On
09-Oct-2013	4	Corrections of typos
03-Feb-2015	5	Updated Section 3.2: TO-220 mechanical data and Section 3.4: D2PAK mechanical data Updated Figure 38: D²PAK footprint

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved

