AP1012A
18V Dual H-Bridge Motor Driver IC

1. Genaral Description

The AP1012A is a dual H-bridge motor driver which has four drive modes: forward, reverse, brake and standby, to operate up to 18V motor supply voltage. An N-channel LDMOS is built in for both high and low sides of the output driver to minimize the device size. Additionally, the AP1012A has under voltage detection and thermal shutdown circuits. It is housed in a small 24-pin QFN package, suitable for driving various types of small motors.

2. Features

• Control Supply Voltage	2.7 to 5.5V
• Logic Terminal Supply Voltage	1.62V to Control Supply Voltage
• Wide Motor Drive Operating Voltage	2 to 18V (NMOS high side and Low side architecture)
• Maximum Output Current(DC)	1.3A
• Maximum Output Current(Peak)	3.0A (Ta = 25°C, less than 10ms in 200ms or less than 5ms in 100ms)
• Maximum Output Current(Peak)	4.5A (Ta = 25°C,less than 5ms in 200ms or less than 2.5ms in 200ms)
• H-Bridge On Resistance	RON(TOP+BPT) = 0.36Ω (typ)@25°C
• Power-Down Mode	VM consumption current less than 2μA(Ta = 25°C)
• Built-in Under Voltage Detection Circuit	Detection Voltage ; 2.2V(typ)
• Built-in Thermal Shut Down Circuit	175°C (typ)
• Junction Temperature (Tj)	150°C (max)
• Package	24-pin QFN (4mmx4mm)

3. Table of Contents

4. Block Diagram

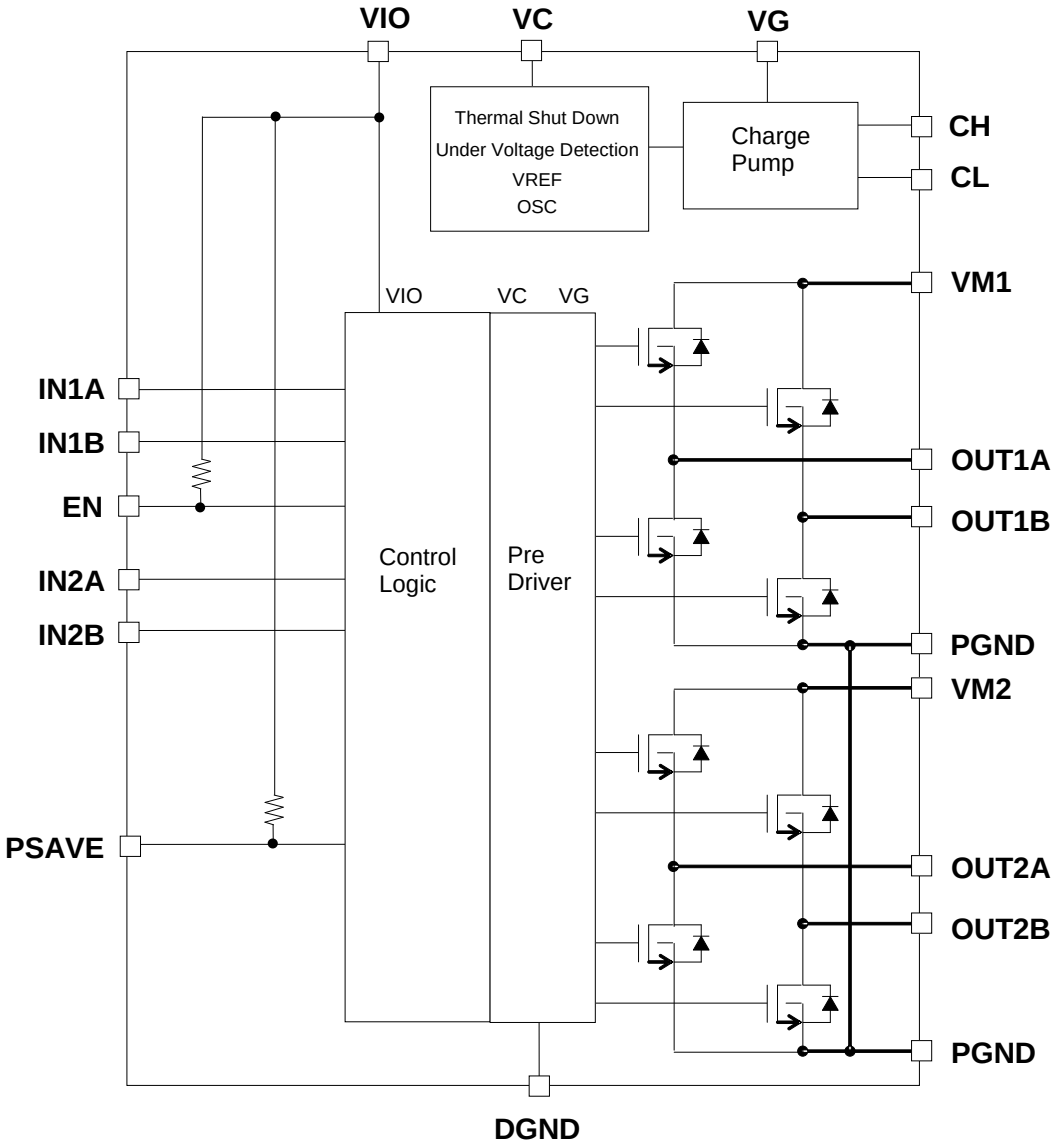


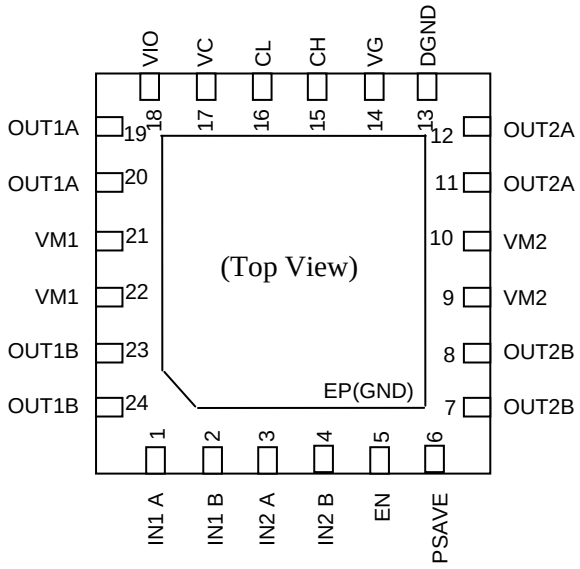
Figure 1. Block Diagram

5. Ordering Guide

AP1012A	-30 to 85°C	24-pin QFN

6. Pin Configurations and Functions

■ Pin Configurations

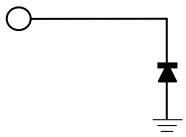
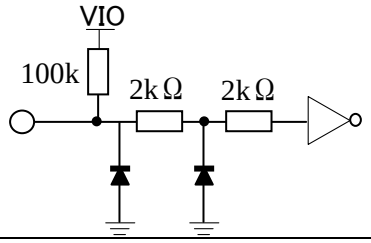
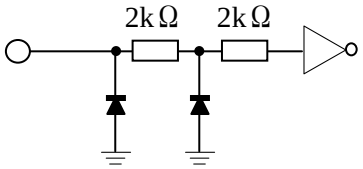
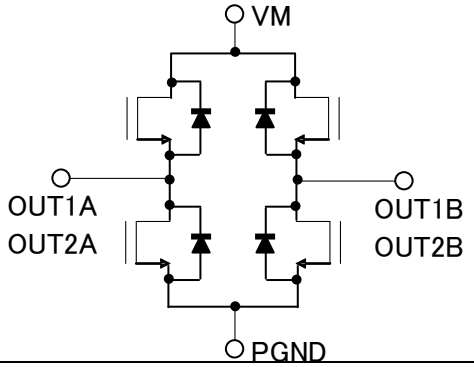
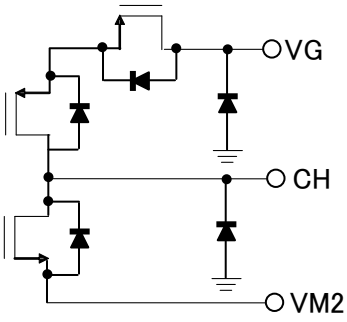
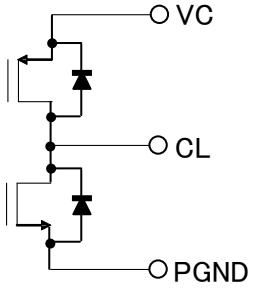
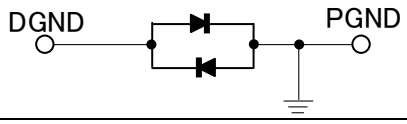


■ Functions

Pin Number	Name	I/O (Note 1)	Function	Remark
14	VG	O	Charge pump output capacitor connection l	
15	CH	I/O	Charge pump capacitor connection l	
16	CL	I/O	Charge pump capacitor connection	
21,22	VM1	P	Motor driver power supply	
19,20	OUT1A	O	Motor driver output	
23,24	OUT1B	O	Motor driver output	
Exposed Pad	PGND	P	Power ground	(Note 2)
11,12	OUT2A	O	Motor driver output	
7,8	OUT2B	O	Motor driver output	
9,10	VM2	P	Motor driver power supply	
4	IN2B	I	Control signal input	
3	IN2A	I	Control signal input	
2	IN1B	I	Control signal input	
1	IN1A	I	Control signal input	
13	DGND	P	Digital Ground	
5	EN	I	Enable signal input	100kΩ pull-up
6	PSAVE	I	Power save input	100kΩ pull-up
18	VIO	P	Logic input terminal power supply	
17	VC	P	Control power supply	

Note 1. I(Input pin), O(Output pin), P(Power pin)
Note 2. The exposed pad must be connected to power ground and DGND.
Note 3. The same voltage must be supplied to VM1(pin No.21, 22) and the VM2 (pin No.9, 10) each other.

■Terminal Equivalent Circuit

Pin No.	Name	Function	Equivalent Circuits
21,22 9,10	VM1 VM2	Motor Driver Power Supply (The same voltage must be supplied to VM1(pin No. 21,22)and VM2(pin No. 9,10) each other)	
18	VIO	Logic Input Terminal Power Supply	
17	VC	Control Power Supply	
5 6	EN PSAVE	Logic Input (Built-in pull-up resistor)	
1 2 3 4	IN1A IN1B IN2A IN2B	Control Signal Input	
19,20 23,24 11,12 7,8	OUT1A OUT1B OUT2A OUT2B	Motor Driver Output	
14 15	VG CH	Charge Pump Output Capacitor Connection Charge Pump Capacitor Connection	
16	CL	Charge Pump Capacitor Connection	
13 Exposed Pad	DGND PGND	Ground Terminal Power Ground Terminal	

7. Absolute Maximum Ratings

Parameter	Symbol	min	max	Unit	Remark
Control supply voltage	VC	-0.5	6	V	
Logic terminal supply voltage	VIO	-0.5	6	V	VIO is under VC voltage (Note 6)
Motor driver supply voltage	VM	-0.5	19	V	
VIO level terminal voltage (PSAVE,EN,IN1A,IN1B,IN2A and IN2B)	Vterminal1	-0.5	5.5	V	
VM level terminal voltage (OUT1A,OUT1B,OUT2A and OUT2B)	Vterminal2	-0.5	19	V	
VG,CH terminal voltage	Vterminal3	-0.5	25	V	
Maximum DC output current	IloaddcMD	-	1.3	A	OUTnA and OUTnB terminal
Maximum peak output current	IloadpeakMD	-	3 4.5	A	OUTnA and OUTnB terminals less than 10ms in 200ms Less than 5ms in 200ms
Power dissipation	PD		1625	mW	Ta=85°C(Note 5)
Operating Temperature range	Ta	-30	85	°C	
Junction temperature	Tj		150	°C	
Storage temperature	Tstg	-65	150	°C	

Note 4. All above voltages respect to Ground (DGND/PGND terminal voltage).
Note 5. The rating is calculated by $R_{\theta J}$ = 40°C/W under the condition when 4 layer board is used. The EP terminal is connected to ground. Compliant to SEMI JEDEC JESD51-6, JESD51-7.
Note 6. Logic terminal supply voltage (VIO) needs to be turned on prior to or at the same time as Control supply voltage(VC).

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

8. Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit	Remark
Control supply voltage	VC	2.7	3.3	5.5	V	
Logic terminal supply voltage	VIO	1.62	1.8/3.3	VC	V	
Motor driver supply voltage	VM	2.0	-	18	V	
Input frequency range (50% duty)	Fin	-	-	200	kHz	

9. Electrical Characteristics

(Ta = 25°C, VM = 15V and VC = 3.3V, otherwise specified.)

Parameter	Symbol	min	typ	max	Unit	Conditions
Charge pump						
Charge pump voltage	VG	18.0	18.2	18.3	V	VG = VC + VM
Charge pump wake up time	t_{VG}	0.1	1	3	ms	VG = VC + VM – 0.3V
VDET1						
VC under voltage detect voltage	VC_{DETLV}	1.9	2.2	2.5	V	
TSD						
Thermal shutdown temperature (Note 7)	T_{DET}	150	175	200	°C	
Temperature hysteresis (Note 7)	T_{DETHYS}	20	30	40	°C	
Consumption current current						
VM consumption current at no power	$I_{VMNOPOW+}$	-	-	2	µA	VC = 0V
VM consumption current at standby	I_{VMSTBY}	-	15	70	µA	PSAVE = “L”, EN = “H” INnA = “L”, INnB = “L”
VC consumption current at standby	I_{VCSTBY}	-	150	300	µA	PSAVE = “L”, EN = “H” INnA = “L”, INnB = “L”
VC consumption current at power save	$I_{VCPSAVE}$	-	-	1	µA	PSAVE = “H”, EN = “H”
VC consumption current at PWM operation	I_{VCPWM}	-	1	2	mA	INnA = 200kHz, INnB = “H”
Motor Driver						
Driver on resistance (High side or Low side)	R_{ON1}	-	0.18	0.25	Ω	VC = 3.3V, Iload = 100mA Ta = 25°C
Driver on resistance (High side or Low side) (Note 7)	R_{ON2}	-	0.22	0.27	Ω	VC = 3.3V, Iload = 1.2A Ta = 25°C (Equivalent Tj = 85°C)
Drive on resistance (High side or Low side) (Note 7)	R_{ON3}	-	0.27	0.32	Ω	VC = 3.3V, Iload = 1.2A Ta = 85°C (Equivalent Tj = 150°C)
Body diode forward voltage	V_{FMD}	-	0.8	1.2	V	I_F = 100 mA
H-Bridge propagation delay time (L→L) (Note 8)	t_{PDLHB}	-	-	0.5	µs	tr = tf = 10ns
H-Bridge propagation delay time (H→H) (Note 8)	t_{PDHHB}	-	-	1.0	µs	tr = tf = 10ns
H-Bridge propagation delay time (HiZ→H)	t_{PDZHHB}	-	-	0.5	µs	tr = tf = 10ns
H-Bridge propagation delay time (H→HiZ)	t_{PDZHHB}	-	-	2.0	µs	tr = tf= 10ns
H-Bridge output pulse width	t_{PWDHB}	0.6	-	-	µs	PWL = 1.0µs, tr = tf = 10ns
Control logic						
Input High level voltage (INnA, INnB)	V_{IH}	0.7×VIO	-	-	V	VIO = 1.6V to 5.5V
Input Low level voltage (INnA, INnB)	V_{IL}	-	-	0.3×VIO	V	

Note 7. Not tested in production.
Note 8. Refer to Figure 2.

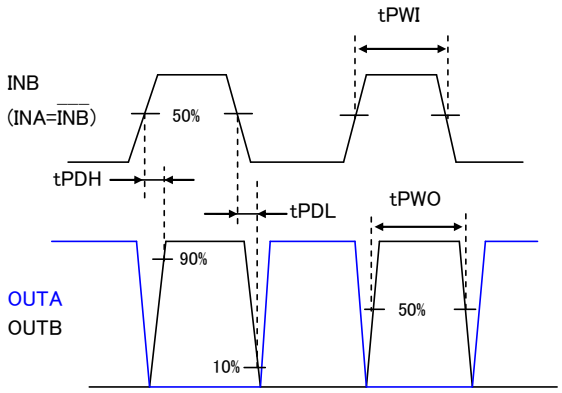


Figure 2. Output Propagate Delay Time Chart

10. Functional Descriptions

10.1 Control Logic

Input and Output statuses of each operation mode are shown below.

PSAVE	EN	Input		Output		Motion
		INnA	INnB	OUTnA	OUTnB	
L	H	L	L	Z	Z	Standby (Idling)
L	H	L	H	L	H	Reverse
L	H	H	L	H	L	Forward
L	H	H	H	L	L	Brake
L	L	X	X	L	L	Brake
H	X	X	X	Z	Z	Power Save (Note 9)

Note 9. TSD/UVLO/VREF/OSC/Charge pump circuits are shut down.

10.2 Basic Architecture of the Motor Driver

The AP1012A has an N-channel LDMOS FET for both high and low sides in the output circuit, so that a small package can be adopted. High side FET is driven by VG voltage, VG=VM+ VC is generated by a charge pump. VG voltage reaches the targeted voltage level within 1ms (typ) after starting the charge pump. The charge pump operates at 360kHz (typ) Low side FET is driven by VC voltage.

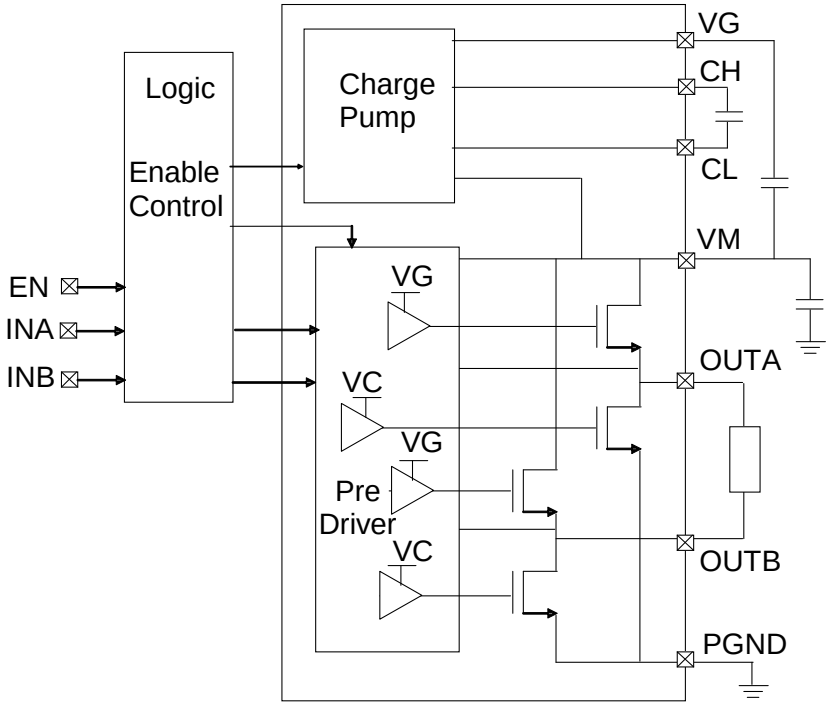


Figure 3. Equivalent Circuit of Motor Driver Block

The OSC block supplies a drive pulse to the charge pump. The input interface block is operated by VIO power supply for logic input terminal VIO power supply needs to be tumed on at the same time as or earlier than VC power supply. (If the VIO is turned on later than the VC, it is recommend to connect pull-up resistance about 5ookΩ between the VIO and the VC pins to avoid an uncertainty stats of the circuit).

10.3 Protection Circuits

The AP1012A has penetration current prevention, thermal shut down and under voltage detection circuits.

- Penetration current prevention circuit
  MOSFET turns off both of high side and low side during the dead time period when penetration current prevention circuit operates. During this period, either body diode is turn on depends on the direction of the current. Figure 4 shows an example when the AP1012A drives the output from "L" to "H" in. (a) shows the case that current flows from external load to the AP1012A, (b) shows the case that current flows from the AP1012A to external load

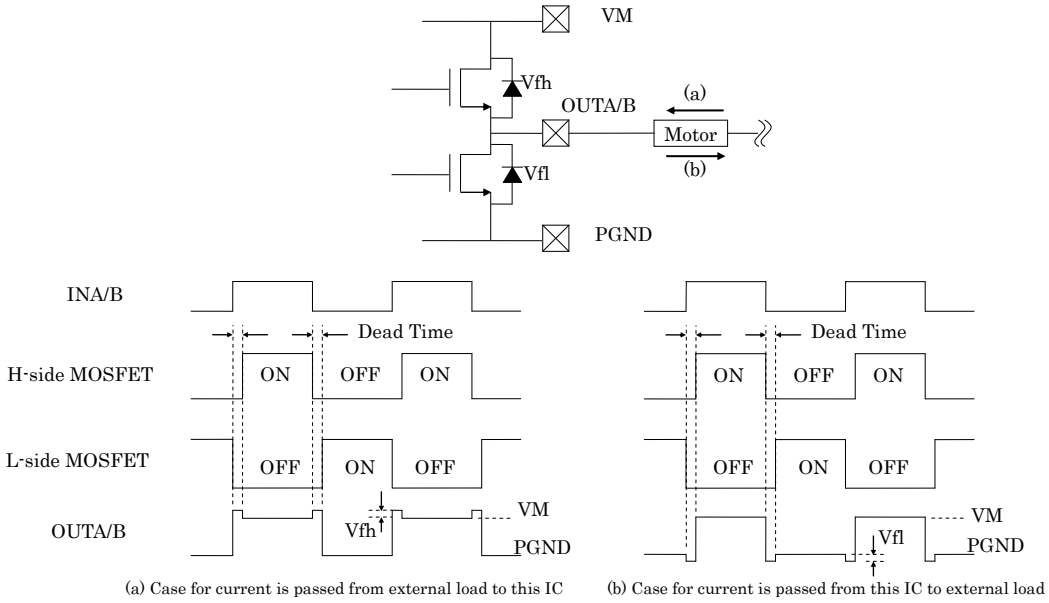


Figure 4. Difference in output terminal by load current direction

- Thermal Shutdown
  The AP1012A prevents damages from self-heating by setting OUTA and OUTB outputs Hi-Z when abnormal high temperature (175°C typ) is detected. The AP1012A is able to return to normal operation as soon as the temperature drops to the level lower than the bottom detection threshold.

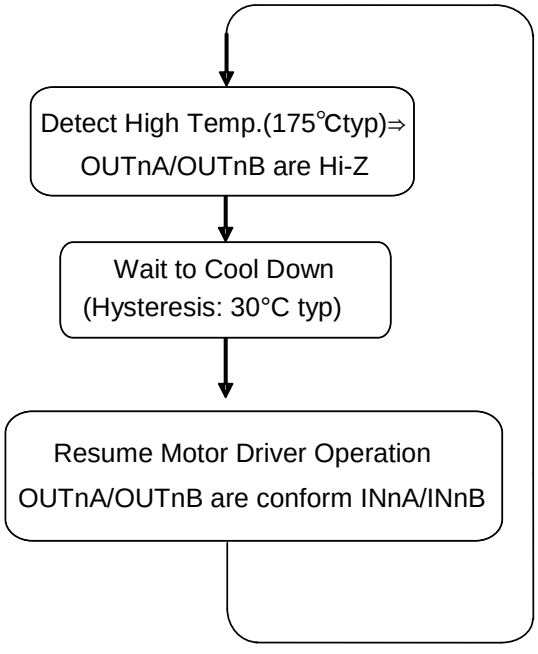


Figure 5. Thermal Shutdown Operation

11. Recommended External Circuits

■ Recommended External Circuits

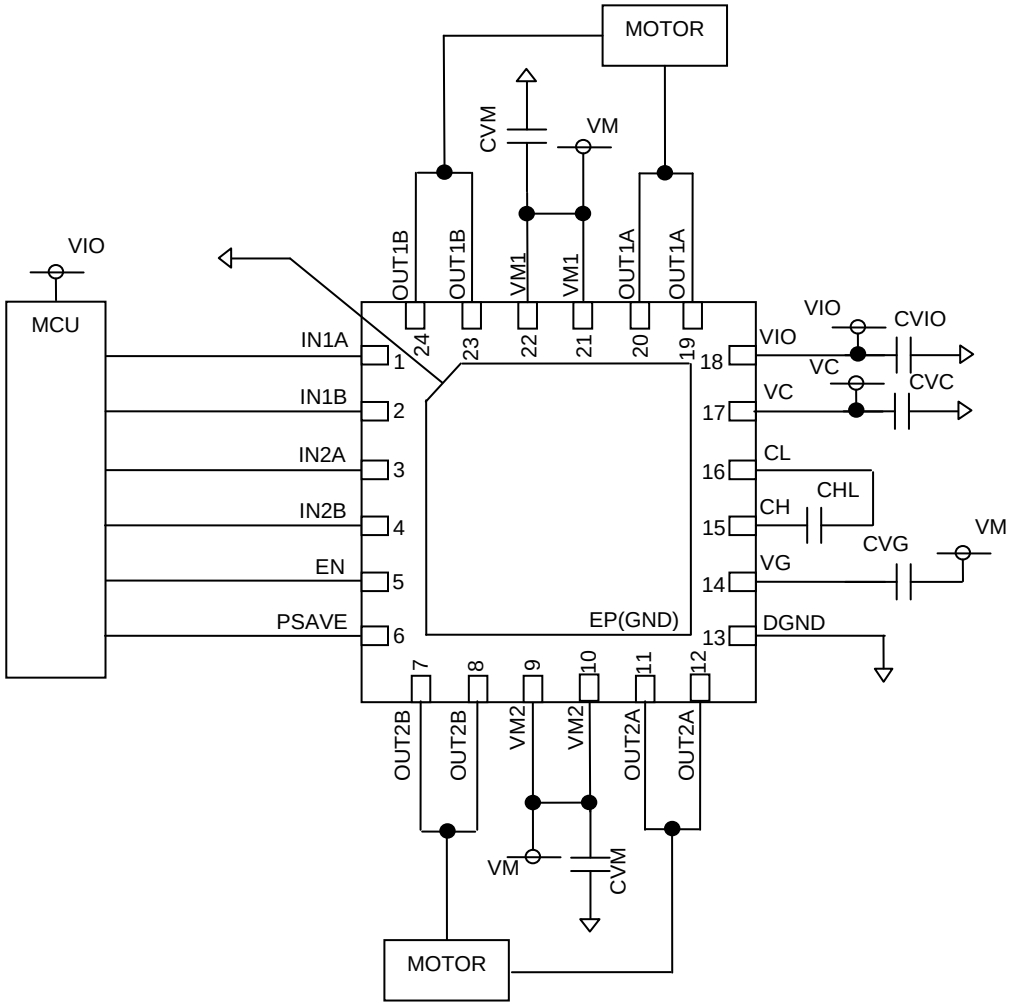


Figure 6. External Circuit Example

■ Reference Value

Table 1. Recommended External Components

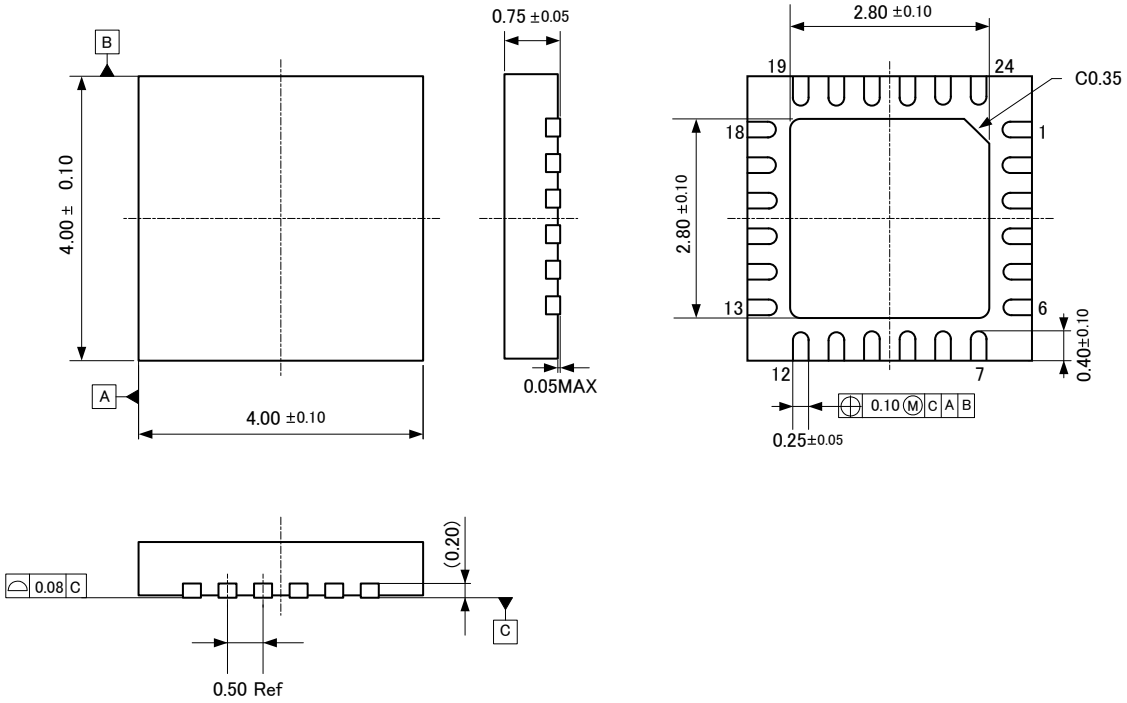
Items	Symbol	min	typ	max	Unit	Remark
Motor driver power supply connection decupling capacitor	CVM	1.0	-	-	µF	(Note 10)
Control power supply connection bypass capacitor	CVC	0.1	1.0	-	µF	Please confirm an appropriate value with the actual system board.
Logic input terminal power supply connection bypass capacitor	CVIO	0.1	1.0	-	µF	Please confirm an appropriate value with the actual system board.
Charge pump capacitor1	CVG	0.047	0.1	0.22	µF	
Charge pump capacitor2	CHL	0.047	0.1	0.22	µF	

Note 10. Connecting capacity of CVM, CVC and CVIO should be determined in consideration of the load current profile, the load capacitance, the wiring resistance and etc. of the actual system board.
Note 11. VM1 and VM2 are not connected internally by a metal layer. Please connect both pins at same voltage level on the mounting board.

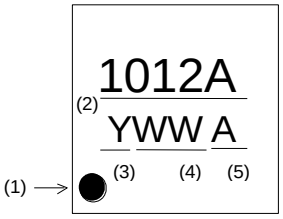
12. Package

■ Outline Dimensions

24-pin QFN (Unit mm)



■ Marking



(1) 1pin Indication
(2) Part Number
(3) Year code（last 1 digit）
(4) Week code
(5) Management code

13. Revise History

Date (YY/MM/DD)	Revision	Page	Contents
12/12/05	00	-	First edition
14/10/09	01	P4	Add Note 3.
14/12/03	02	P10	Correct some sentences and figure 4 in 10.3 Protection Circuits.
14/12/12	03	P12	Correct part number in marking (12. Package).

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