INTEGRATED CIRCUITS

DATA SHEET

74AHC1G14; 74AHCT1G14
Inverting Schmitt trigger

Product specification
Supersedes data of 1999 Aug 05
File under Integrated Circuits, IC06

2001 Feb 22

Philips
Semiconductors

PHILIPS

FEATURES

- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Low power dissipation
- Balanced propagation delays
- Very small 5 pin package
- Output capability: standard.

APPLICATIONS

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.

DESCRIPTION

The 74AHC1G/AHCT1G14 is a high-speed Si-gate CMOS device.

The 74AHC1G/AHCT1G14 provides the inverting buffer function with Schmitt-trigger action. These devices are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC1G	AHCT1G	
t_{PHL}/t_{PLH}	propagation delay A to Y	C_L = 15 pF; V_{CC} = 5 V	3.2	4.1	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance	C_L = 15 pF; f = 1 MHz; notes 1 and 2	12	13	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
A	Y
L	H
H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

Inverting Schmitt trigger — 74AHC1G14; 74AHCT1G14

ORDERING INFORMATION

TYPE NUMBER	PACKAGES					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74AHC1G14GW	–40 to +85 °C	5	SC-88A	plastic	SOT353	AF
74AHCT1G14GW	–40 to +85 °C	5	SC-88A	plastic	SOT353	CF

PINNING

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	A	data input A
3	GND	ground (0 V)
4	Y	data output Y
5	V_{CC}	supply voltage

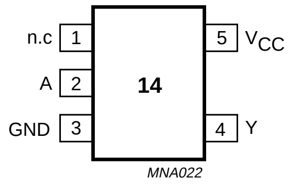


Fig.1 Pin configuration.

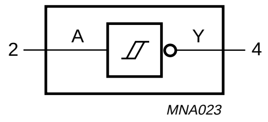


Fig.2 Logic symbol.

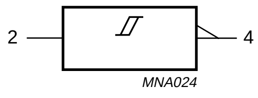


Fig.3 IEC logic symbol.

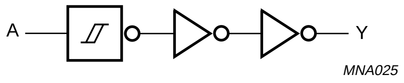


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC1G			74AHCT1G			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V	–	–20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_O	output source or sink current	$-0.5\text{ V} < V_O < V_{CC} + 0.5$ V	–	±25	mA
I_{CC}	V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +85 °C; note 2	–	200	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 55 °C the value of P_D derates linearly with 2.5 mW/K.

DC CHARACTERISTICS

Family 74AHC1G

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		
				MIN.	TYP.	MAX.	MIN.	MAX.	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -50$ μA	2.0	1.9	2.0	–	1.9	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -50$ μA	3.0	2.9	3.0	–	2.9	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -50$ μA	4.5	4.4	4.5	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -4.0$ mA	3.0	2.58	–	–	2.48	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -8.0$ mA	4.5	3.94	–	–	3.8	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 50$ μA	2.0	–	0	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 50$ μA	3.0	–	0	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 50$ μA	4.5	–	0	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 4.0$ mA	3.0	–	–	0.36	–	0.44	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 8.0$ mA	4.5	–	–	0.36	–	0.44	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	0.1	–	1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	1.0	–	10	μA
C_I	input capacitance			–	1.5	10	–	10	pF

Family 74AHCT1G

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		
				MIN.	TYP.	MAX.	MIN.	MAX.	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -50\ \mu A$	4.5	4.4	4.5	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -8.0$ mA	4.5	3.94	–	–	3.8	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 50\ \mu A$	4.5	–	0	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 8.0$ mA	4.5	–	–	0.36	–	0.44	V
I_{LI}	input leakage current	$V_I = V_{IH}$ or V_{IL}	5.5	–	–	0.1	–	1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	1.0	–	10	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = 3.4$ V; other inputs at V_{CC} or GND; $I_O = 0$	5.5	–	–	1.35	–	1.5	mA
C_I	input capacitance			–	1.5	10	–	10	pF

TRANSFER CHARACTERISTICS

Type 74AHC1G14

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		
				MIN.	TYP.	MAX.	MIN.	MAX.	
V_{T+}	positive-going threshold	see Figs 7 and 8	3.0	–	–	2.2	–	2.2	V
			4.5	–	–	3.15	–	3.15	V
			5.5	–	–	3.85	–	3.85	V
V_{T-}	negative-going threshold	see Figs 7 and 8	3.0	0.9	–	–	0.9	–	V
			4.5	1.35	–	–	1.35	–	V
			5.5	1.65	–	–	1.65	–	V
V_H	hysteresis ($V_{T+} – V_{T-}$)	see Figs 7 and 8	3.0	0.3	–	1.2	0.3	1.2	V
			4.5	0.4	–	1.4	0.4	1.4	V
			5.5	0.5	–	1.6	0.5	1.6	V

Type 74AHCT1G14

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		WAVEFORMS	V_{CC} (V)	25			−40 to +85		
				MIN.	TYP.	MAX.	MIN.	MAX.	
V_{T+}	positive-going threshold	see Figs 7 and 8	4.5	–	–	2.0	–	2.0	V
			5.5	–	–	2.0	–	2.0	V
V_{T-}	negative-going threshold	see Figs 7 and 8	4.5	0.5	–	–	0.5	–	V
			5.5	0.6	–	–	0.6	–	V
V_H	hysteresis ($V_{T+} – V_{T-}$)	see Figs 7 and 8	4.5	0.4	–	1.4	0.4	1.4	V
			5.5	0.4	–	1.6	0.4	1.6	V

AC CHARACTERISTICS

Type 74AHC1G14

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		WAVEFORMS	C_L	25			−40 to +85		
				MIN.	TYP.	MAX.	MIN.	MAX.	
V_{CC} = 3.0 to 3.6V; note 1									
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 6	15 pF	–	4.2	12.8	1.0	15.0	ns
			50 pF	–	6.0	16.3	1.0	18.5	ns
V_{CC} = 4.5 to 5.5 V; note 2									
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 6	15 pF	–	3.2	8.6	1.0	10.0	ns
			50 pF	–	4.6	10.6	1.0	12.0	ns

Notes

1. Typical values are measured at V_{CC} = 3.3 V.
2. Typical values are measured at V_{CC} = 5.0 V.

Type 74AHCT1G14

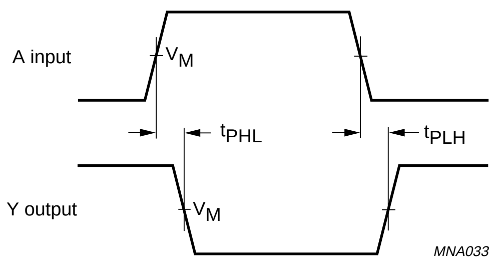
GND = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		WAVEFORMS	C_L	25			−40 to +85		
				MIN.	TYP.	MAX.	MIN.	MAX.	
V_{CC} = 4.5 to 5.5 V; note 1									
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 6	15 pF	–	4.1	7.0	1.0	8.0	ns
			50 pF	–	5.9	8.5	1.0	10.0	ns

Note

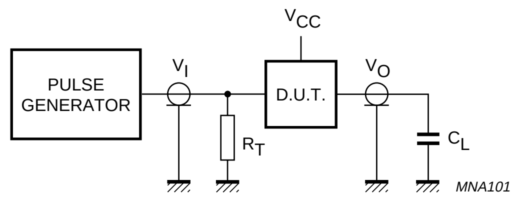
1. Typical values are measured at V_{CC} = 5 V.

AC WAVEFORMS



FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC1G	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT1G	GND to 3.0 V	1.5 V	50% V_{CC}

Fig.5 The input (A) to output (Y) propagation delays.



Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance. (See Chapter “AC characteristics” for values).

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.6 Load circuitry for switching times.

TRANSFER CHARACTERISTIC WAVEFORMS

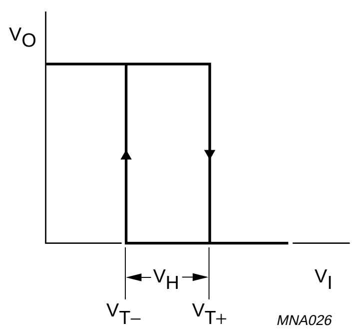


Fig.7 Transfer characteristic.

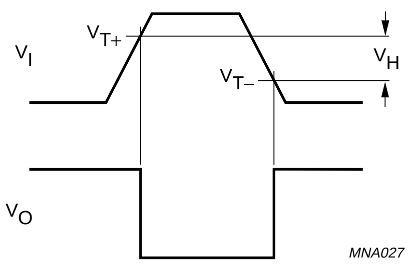


Fig.8 The definitions of V_{T+}, V_{T-} and V_H.

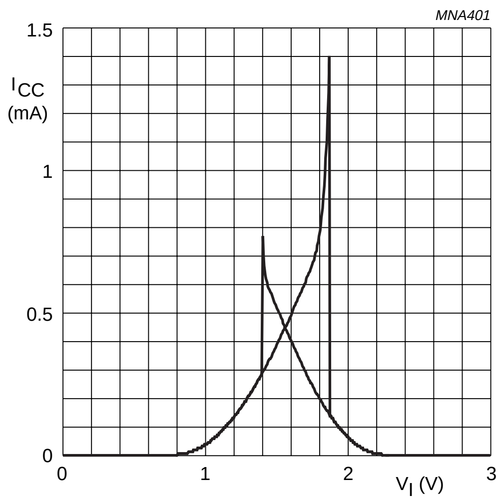


Fig.9 Typical AHC1G14 transfer characteristics; V_{CC} = 3.0 V.

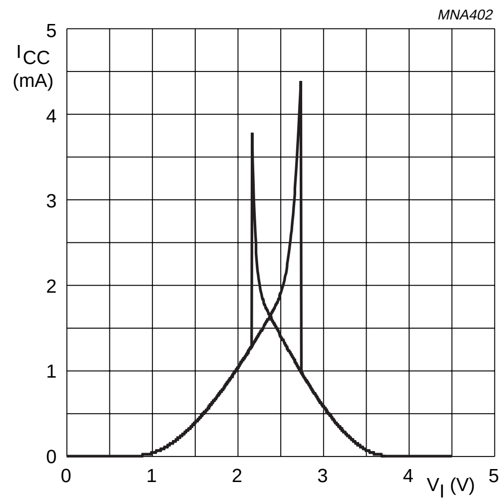


Fig.10 Typical AHC1G14 transfer characteristics; V_{CC} = 4.5 V.

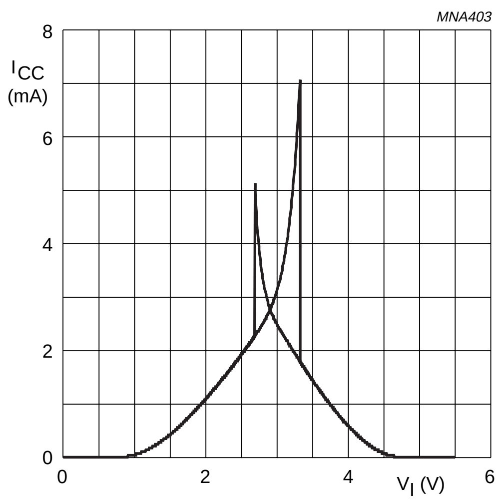


Fig.11 Typical AHC1G14 transfer characteristics; V_{CC} = 5.5 V.

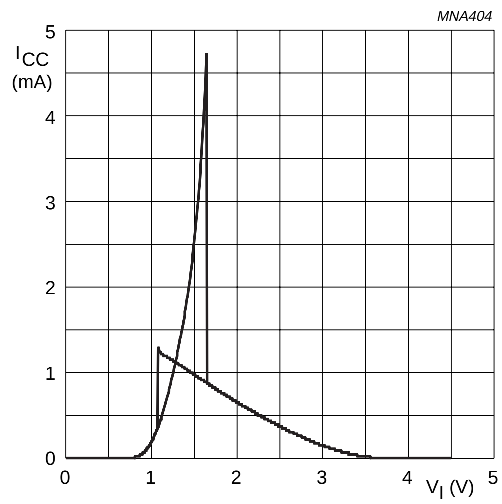


Fig.12 Typical AHCT1G14 transfer characteristics; V_{CC} = 4.5 V.

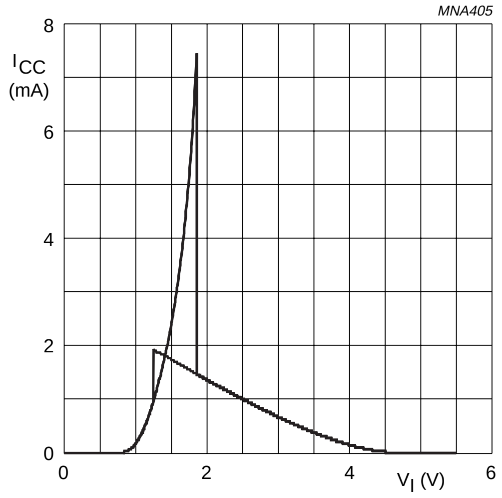


Fig.13 Typical AHCT1G14 transfer characteristics; V_{CC} = 5.5 V.

APPLICATION INFORMATION

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{ad} = f_i \times (t_r \times I_{CC(AV)} + t_f \times I_{CC(AV)}) \times V_{CC}$ where:

P_{ad} = additional power dissipation (μW);

f_i = input frequency (MHz);

t_r = input rise time (ns); 10% to 90%;

t_f = input fall time (ns); 90% to 10%;

$I_{CC(AV)}$ = average additional supply current (μA).

Average I_{CC} differs with positive or negative input transitions, as shown in Figs 14 and 15.

For AHC1G/AHCT1G14 used in relaxation oscillator circuit, see Fig.16.

Note to the application information:

1. All values given are typical unless otherwise specified.

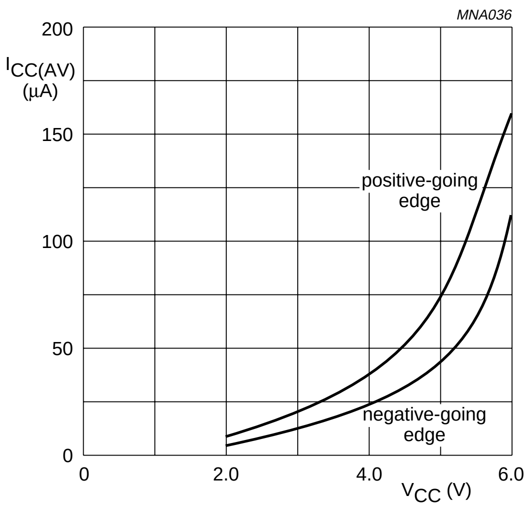


Fig.14 Average I_{CC} for AHC1G Schmitt-trigger devices; linear change of V_I between $0.1V_{CC}$ to $0.9V_{CC}$.

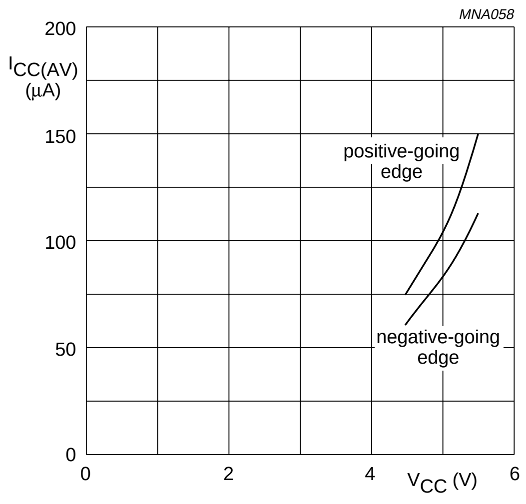
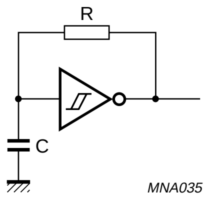


Fig.15 Average I_{CC} for AHCT1G Schmitt-trigger devices; linear change of V_I between $0.1V_{CC}$ to $0.9V_{CC}$.



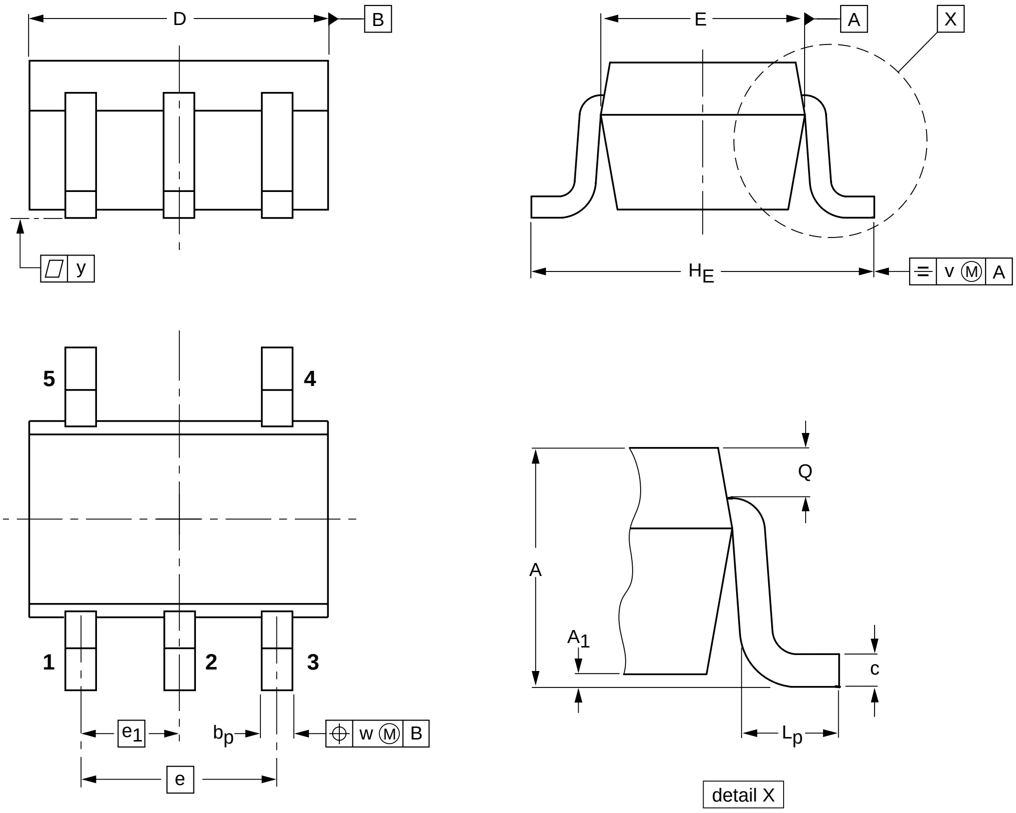
For AHC1G: $f = \frac{1}{T} \approx \frac{1}{0.55 \times RC}$

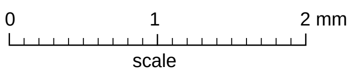
For AHCT1G: $f = \frac{1}{T} \approx \frac{1}{0.60 \times RC}$

Fig.16 Relaxation oscillator using the AHC1G/AHCT1G14.

PACKAGE OUTLINE

Plastic surface mounted package; 5 leads **SOT353**





DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E (2)	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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