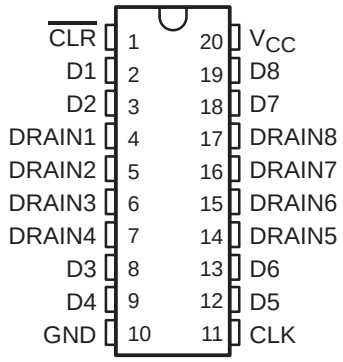
- **Low $r_{DS(on)}$ . . . 1.3 Ω Typ**
- **Avalanche Energy . . . 75 mJ**
- **Eight Power DMOS Transistor Outputs of 250-mA Continuous Current**
- **1.5-A Pulsed Current Per Output**
- **Output Clamp Voltage up to 45 V**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)



description

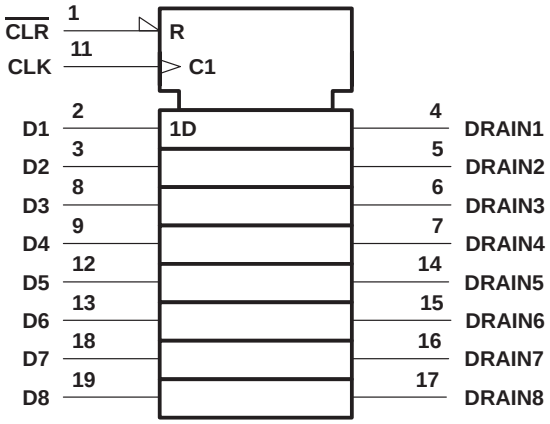
The TPIC6273 is a monolithic high-voltage high-current power logic octal D-type latch with DMOS transistor outputs designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

The TPIC6273 contains eight positive-edge-triggered D-type flip-flops with a direct clear input. Each flip-flop features an open-drain power DMOS transistor output.

When clear ($\overline{CLR}$) is high, information at the D inputs meeting the setup time requirements is transferred to the DRAIN outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous $\overline{CLR}$ is provided to turn all eight DMOS-transistor outputs off.

The TPIC6273 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic symbol†



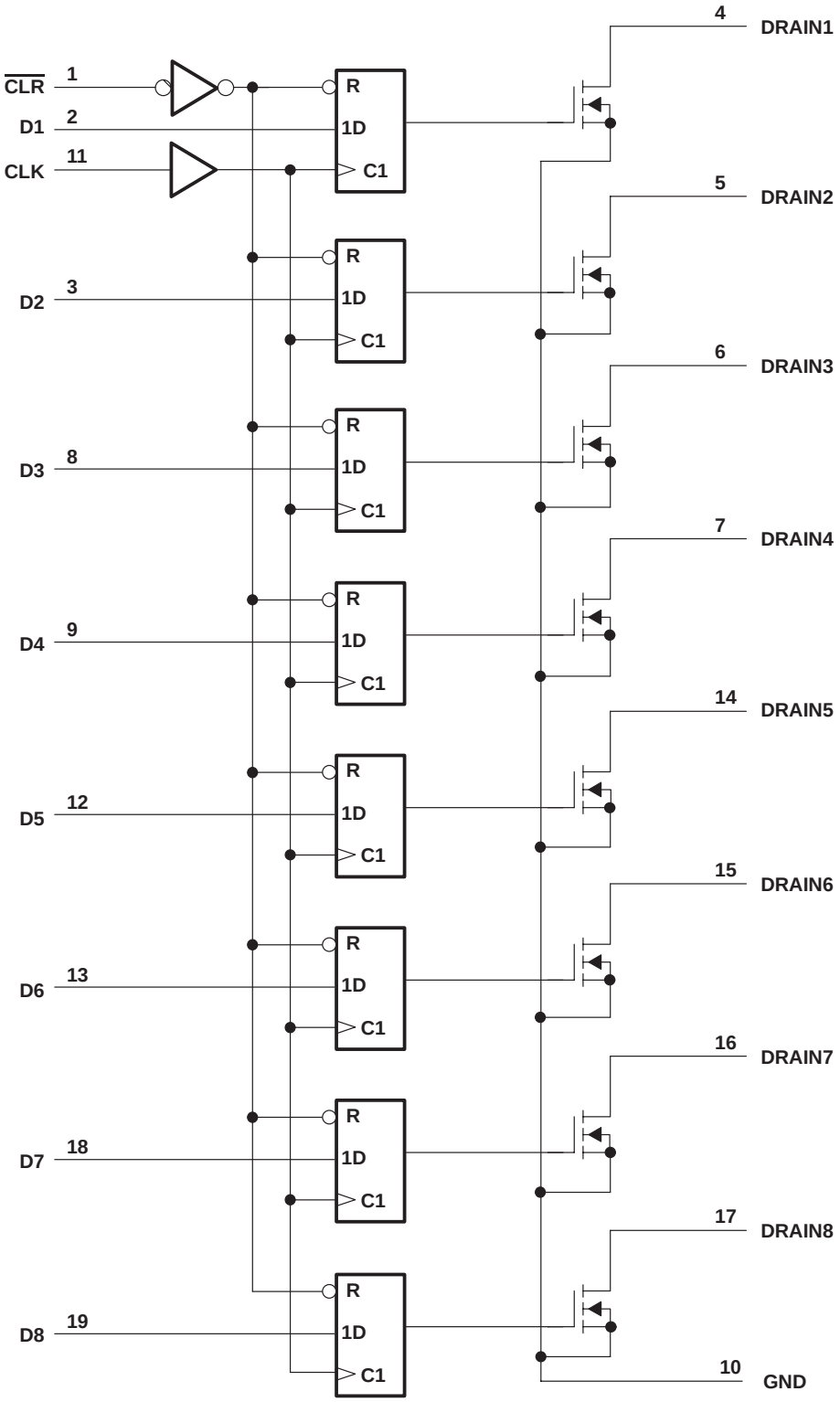
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(each channel)

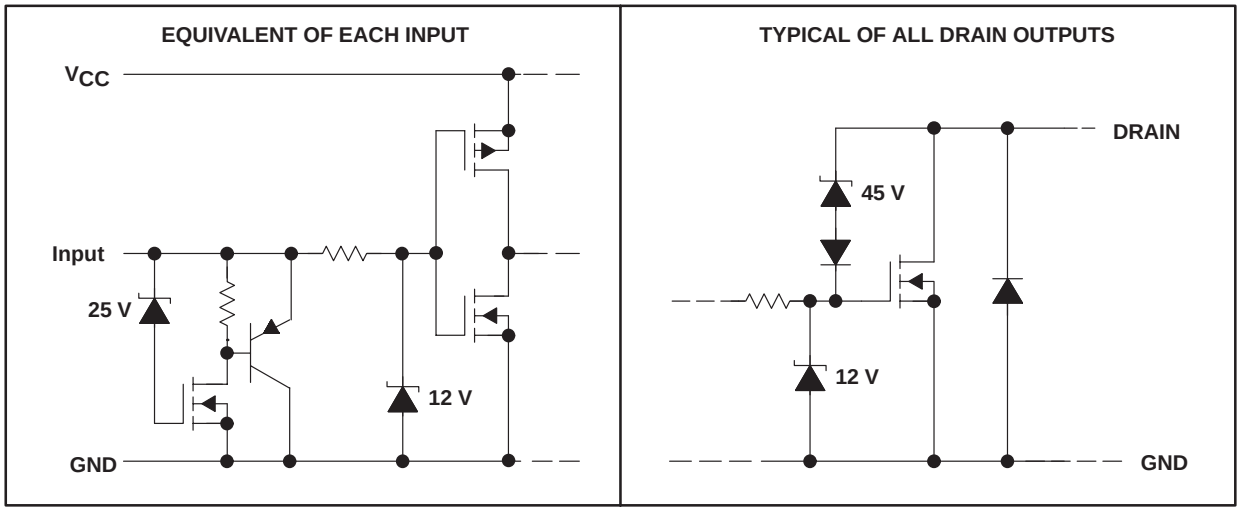
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	DRAIN
L	X	X	H
H	↑	H	L
H	↑	L	H
H	L	X	Latched

H = high level, L = low level, X = irrelevant

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	–0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	250 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	2 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	75 mJ
Avalanche current, I_{AS} (see Note 4)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 100 mH, I_{AS} = 1 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	–1.8	1.5	A
Setup time, D high before CLK↑, t_{su} (see Figure 2)	10		ns
Hold time, D high after CLK↑, t_h (see Figure 2)	15		ns
Pulse duration, t_w (see Figure 2)	25		ns
Operating case temperature, T_C	–40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		45			V
V_{SD}	Source-drain diode forward voltage	I_F = 250 mA, See Note 3			0.85	1	V
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = V_{CC}				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				–1	µA
I_{CC}	Logic supply current	I_O = 0, All inputs low			15	100	µA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, I_N = I_D, T_C = 85°C	See Notes 5, 6, and 7		250		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V			0.05	1	µA
		V_{DS} = 40 V, T_C = 125°C			0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 250 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 8 and 9		1.3	2	Ω
		I_D = 250 mA, T_C = 125°C, V_{CC} = 4.5 V			2	3.2	
		I_D = 500 mA, V_{CC} = 4.5 V			1.3	2	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from CLK	C_L = 30 pF, I_D = 250 mA, See Figures 1, 2, and 10		625		ns
t_{PHL}	Propagation delay time, high-to-low-level output from CLK			150		ns
t_r	Rise time, drain output			675		ns
t_f	Fall time, drain output			400		ns
t_a	Reverse-recovery-current rise time	I_F = 250 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
5. Technique should limit T_J – T_C to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		111	°C/W
		N package			108	

PARAMETER MEASUREMENT INFORMATION

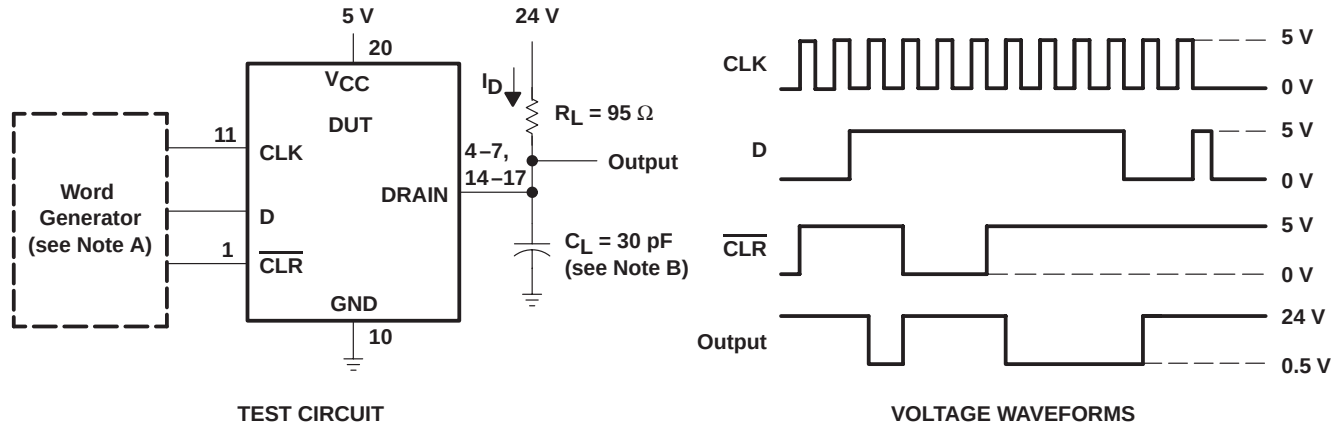


Figure 1. Resistive Load Normal Operation

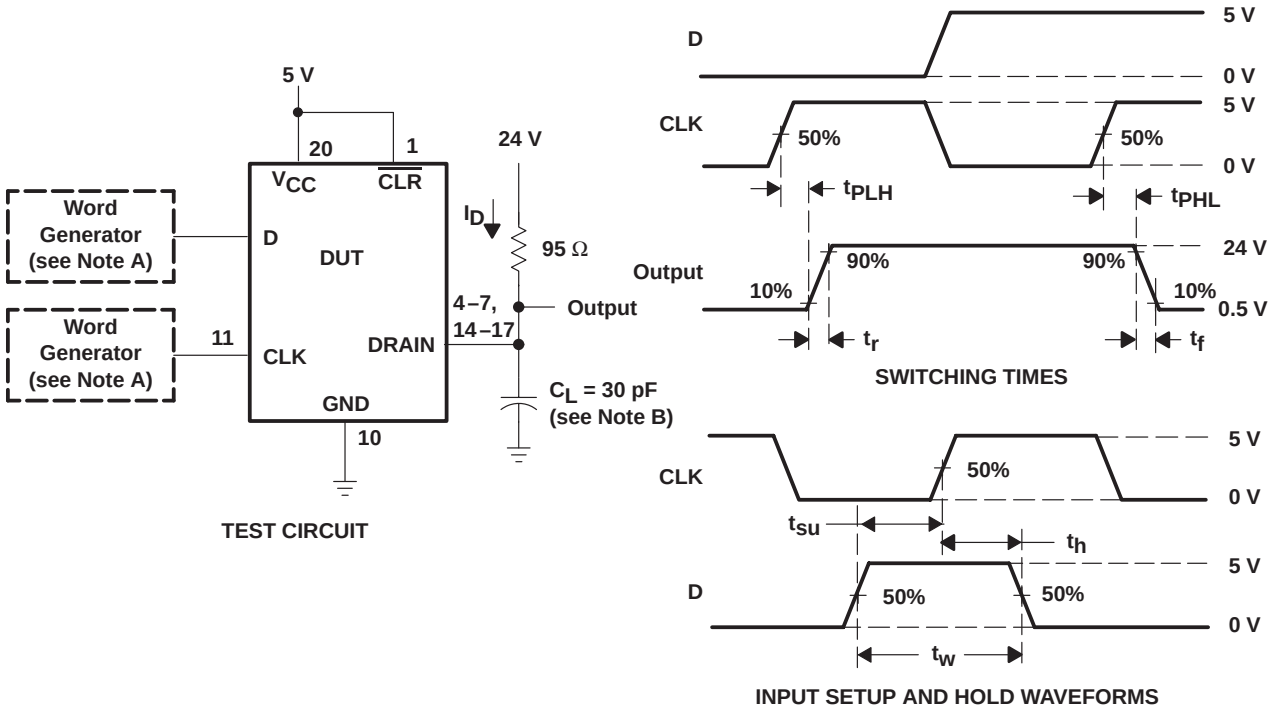
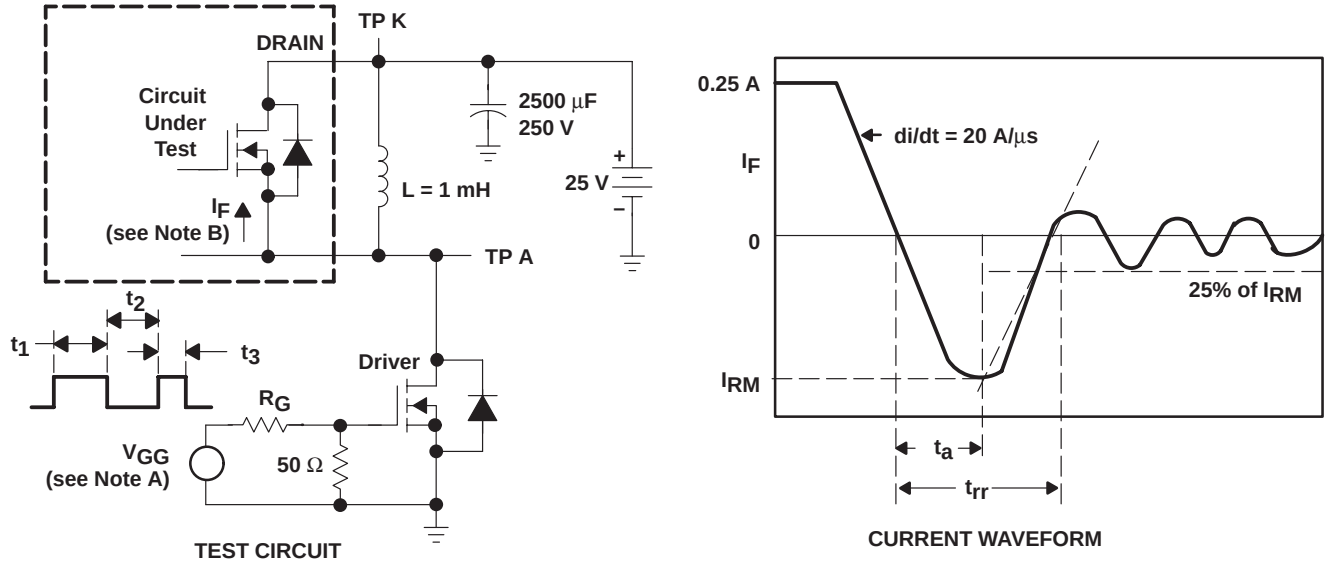


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

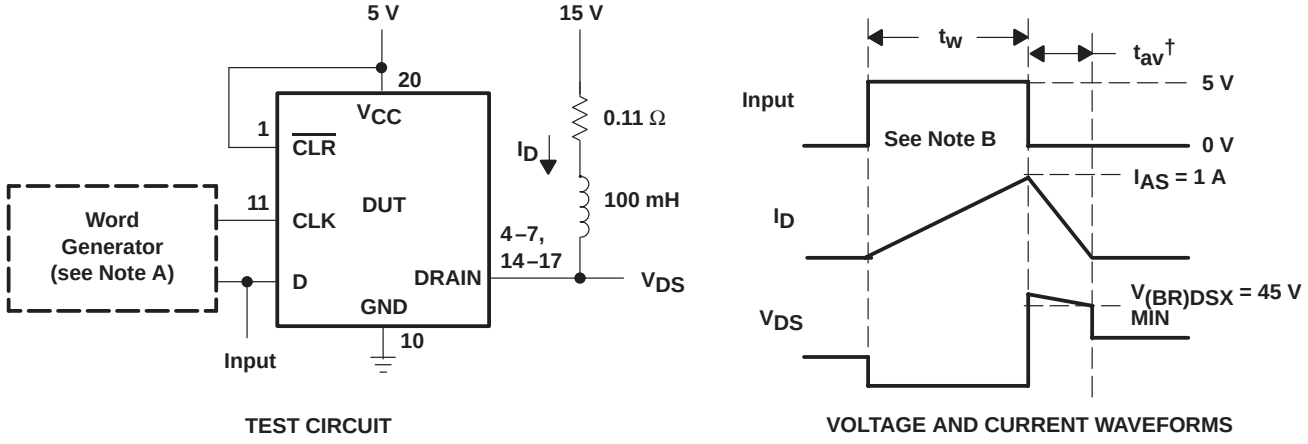
NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 KHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/μs. A V_{GG} double-pulse train is used to set I_F = 0.25 A, where t_1 = 10 μs, t_2 = 7 μs, and t_3 = 3 μs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



† Non-JEDEC symbol for avalanche ftime.

NOTES: A. The word generator A has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, Z_O = 50 Ω.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 1 A.
Energy test is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

**PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE**

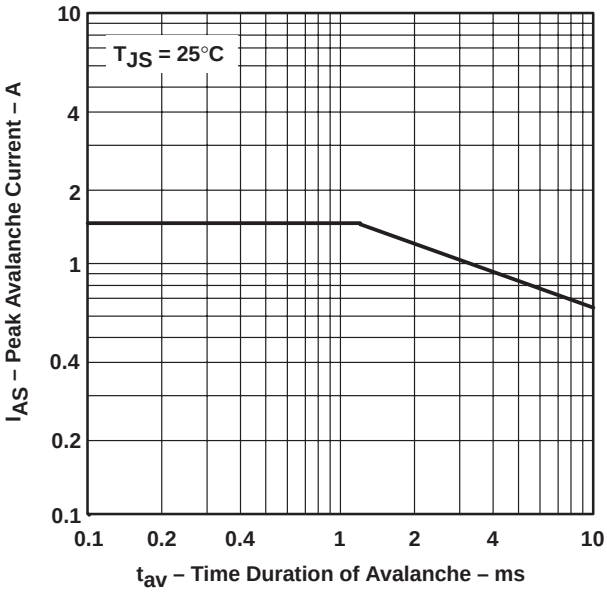


Figure 5

**MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY**

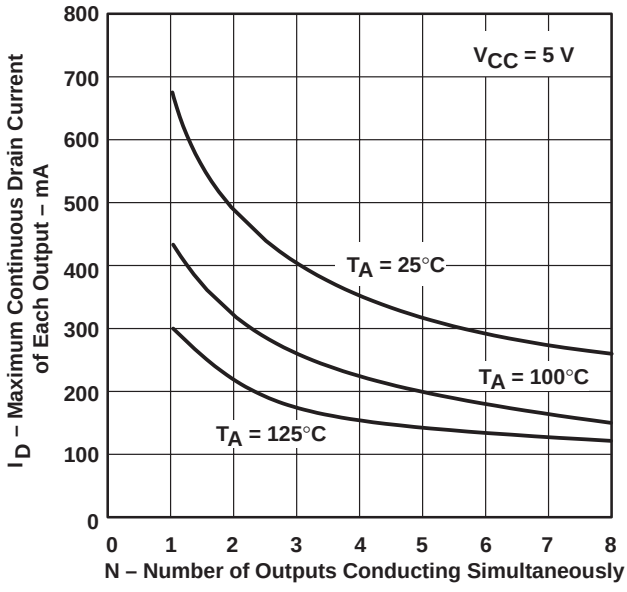


Figure 6

**MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY**

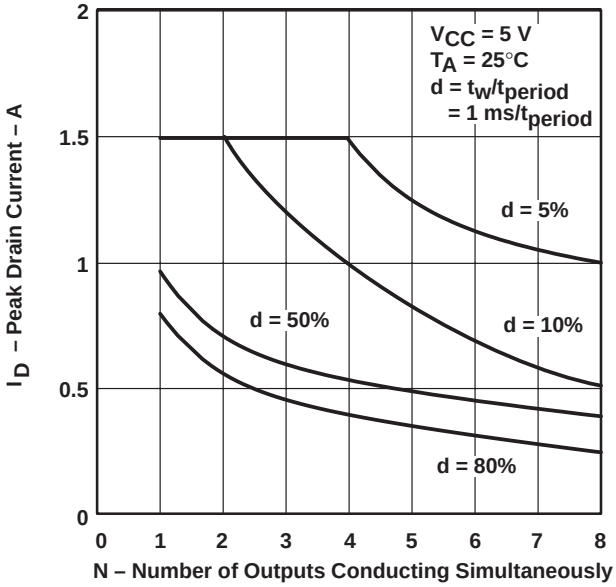


Figure 7

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

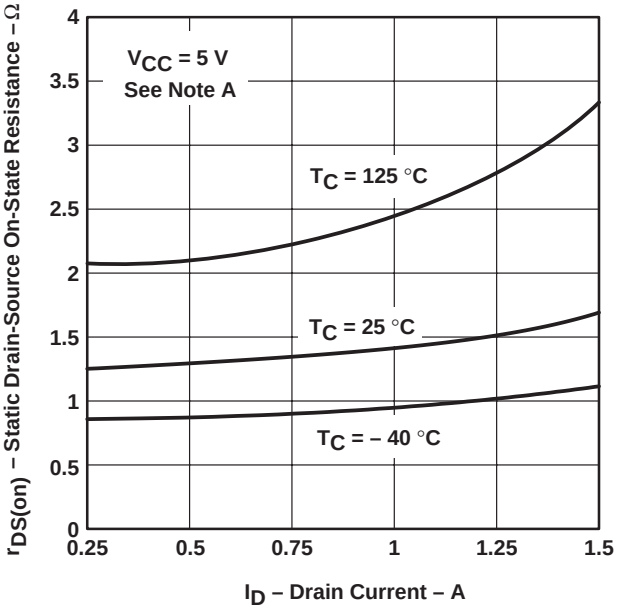


Figure 8

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

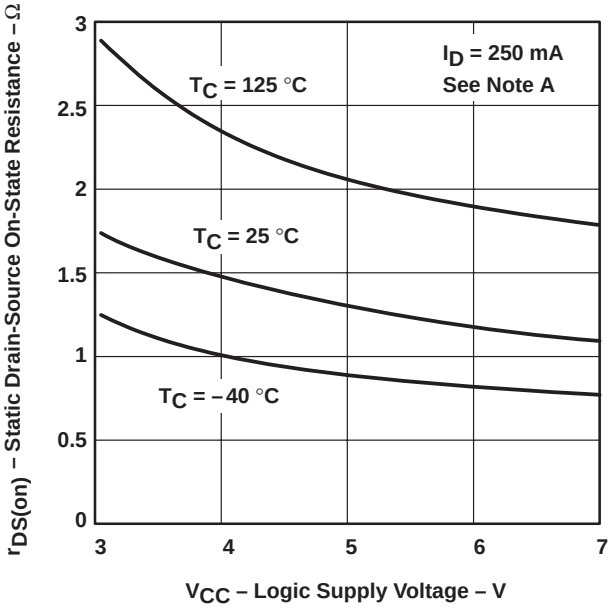


Figure 9

SWITCHING TIME vs FREE-AIR TEMPERATURE

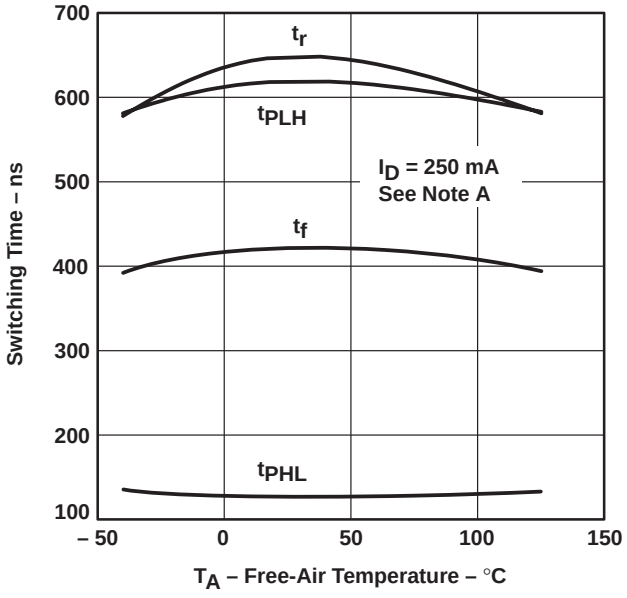


Figure 10

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPIC6273DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6273
TPIC6273DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6273
TPIC6273DWG4	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	TPIC6273
TPIC6273DWG4.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6273
TPIC6273DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6273
TPIC6273DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6273
TPIC6273DWRG4	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TPIC6273
TPIC6273DWRG4.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6273
TPIC6273N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPIC6273N
TPIC6273N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPIC6273N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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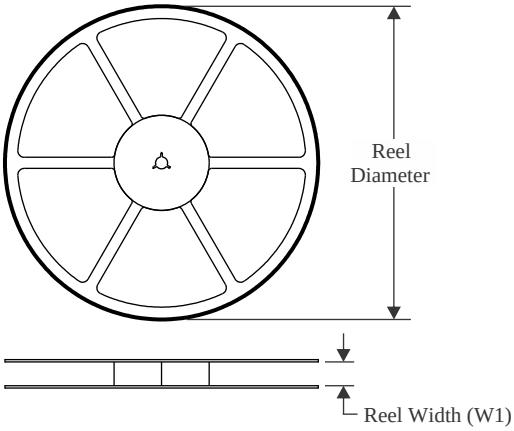
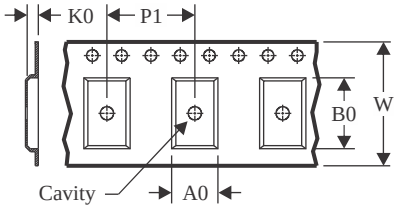
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

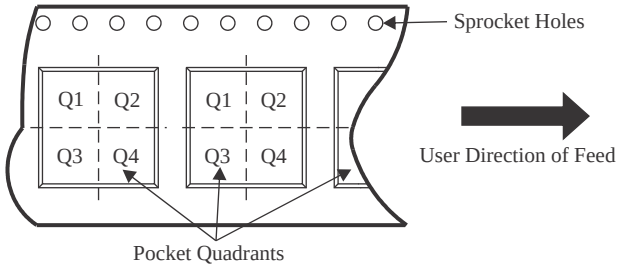


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

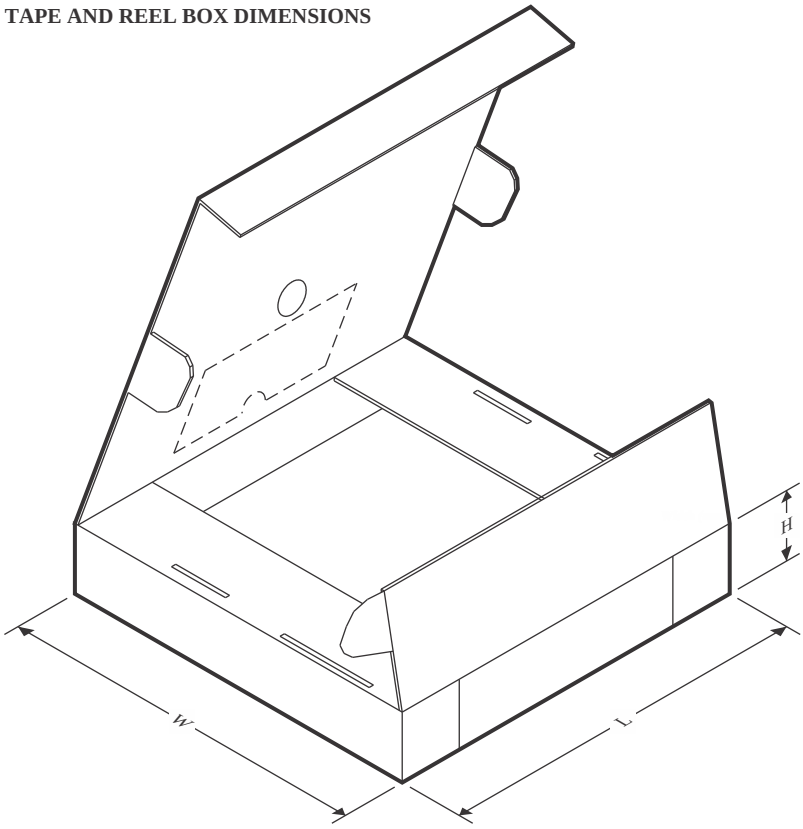
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TPIC6273DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

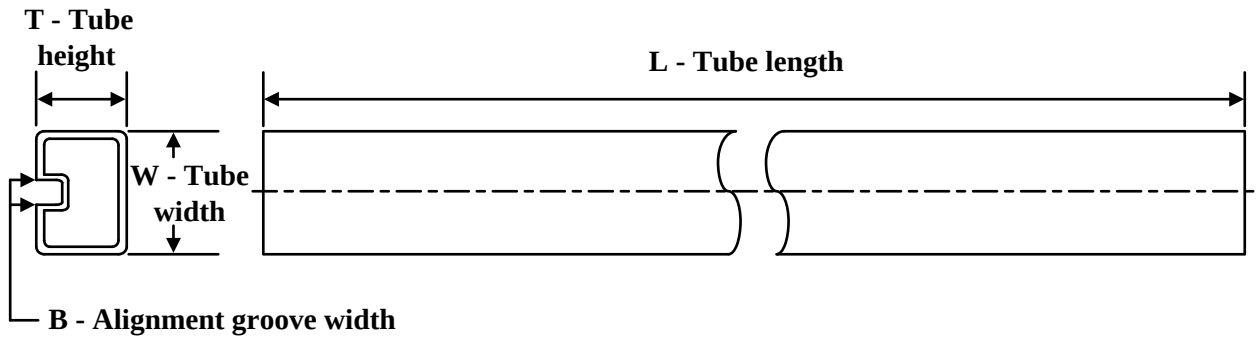
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6273DWR	SOIC	DW	20	2000	350.0	350.0	43.0
TPIC6273DWRG4	SOIC	DW	20	2000	350.0	350.0	43.0

TUBE



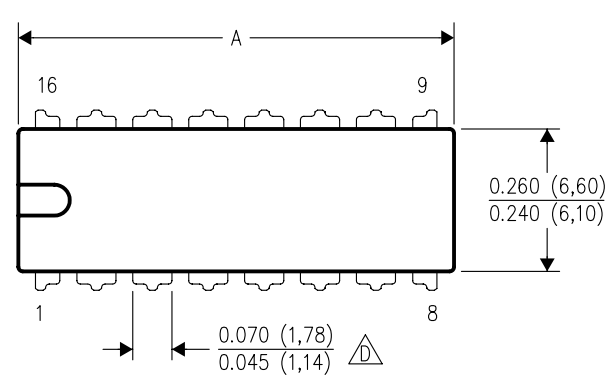
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPIC6273DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TPIC6273DW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
TPIC6273DWG4	DW	SOIC	20	25	506.98	12.7	4826	6.6
TPIC6273DWG4.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
TPIC6273N	N	PDIP	20	20	506	13.97	11230	4.32
TPIC6273N.A	N	PDIP	20	20	506	13.97	11230	4.32

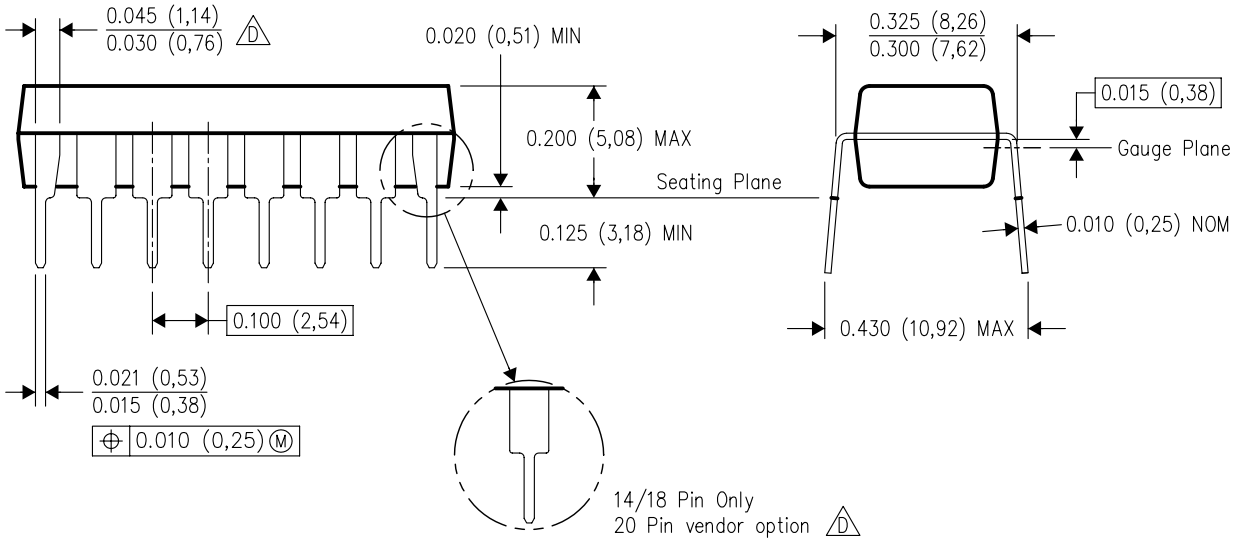
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

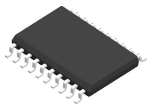


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

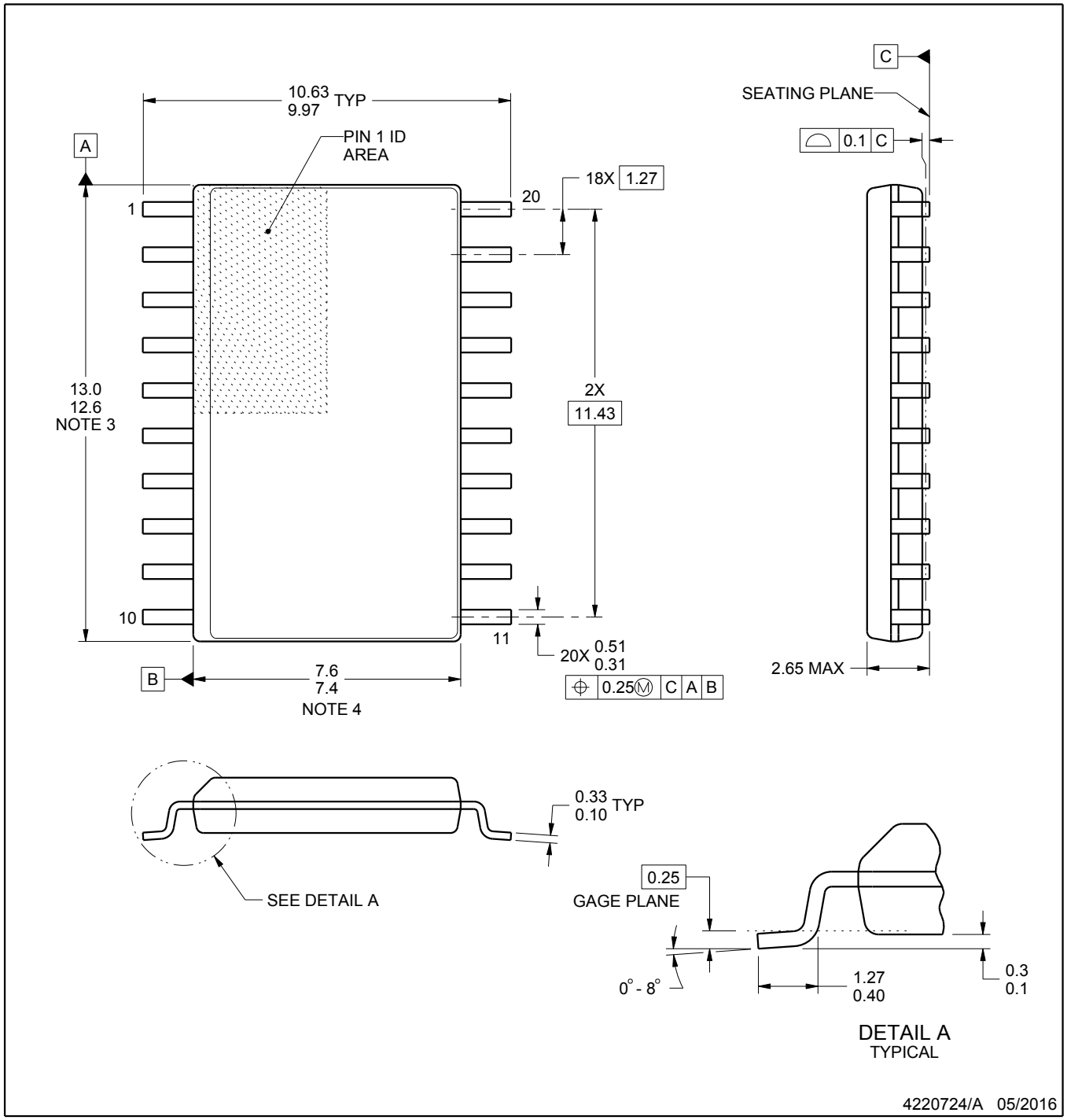


PACKAGE OUTLINE

DW0020A

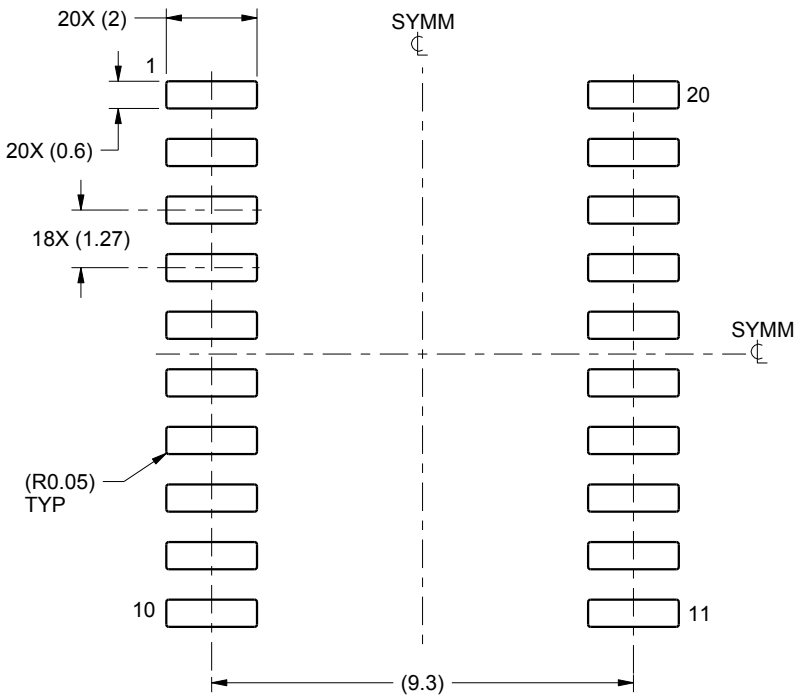
SOIC - 2.65 mm max height

SOIC

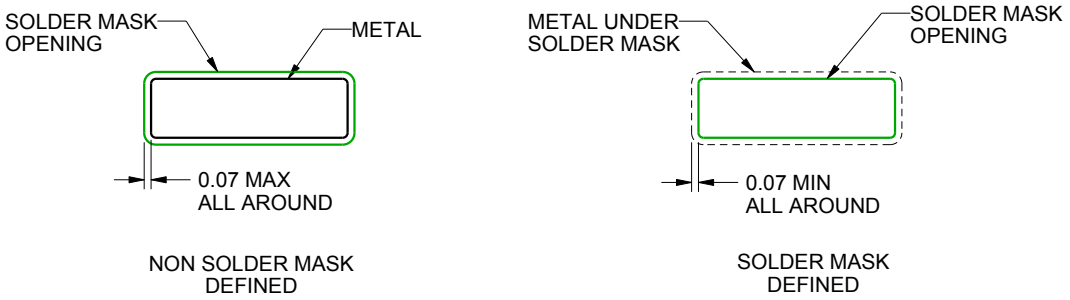


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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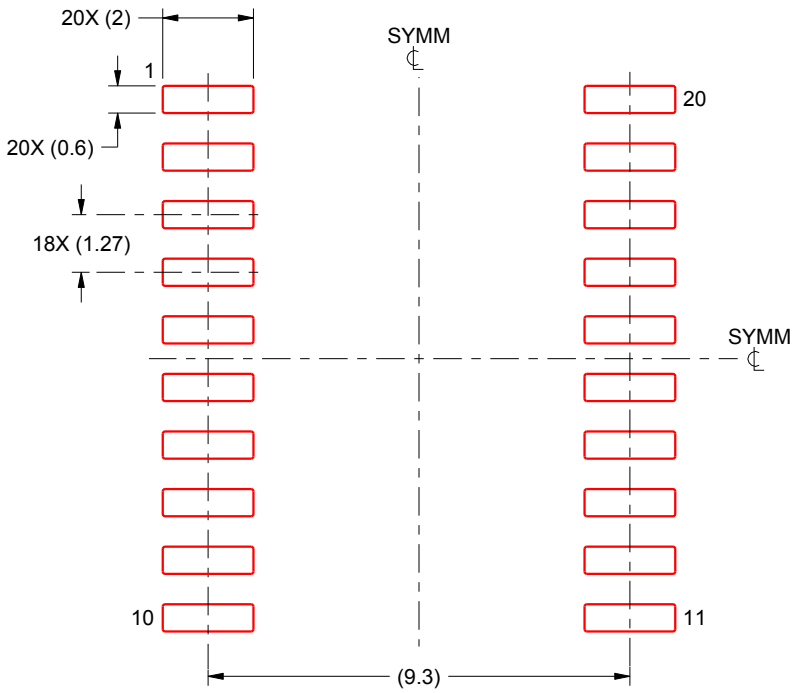
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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