

# 4-channel driver and power controller

## BA6893AK

The BA6893AK is a 4-channel driver and power supply that includes the reset, recharge, and shock detection circuits required for portable CD players on a single IC. The driver block power supply uses the on-chip switching regulator, making this component an ideal choice for low-power sets.

### ● Applications

Portable CD players

### ● Features

- 1) Four H-bridge driver circuits.
- 2) DC to DC converter control circuit.
- 3) Reset circuit.
- 4) Shock detection circuit.
- 5) Battery recharge circuit.
- 6) Ripple filter circuit.
- 7) Audio reference output.
- 8) Low power consumption.
- 9) Thermal shutdown circuit.
- 10) QFP44 package.

### ● Absolute maximum ratings (Ta = 25°C)

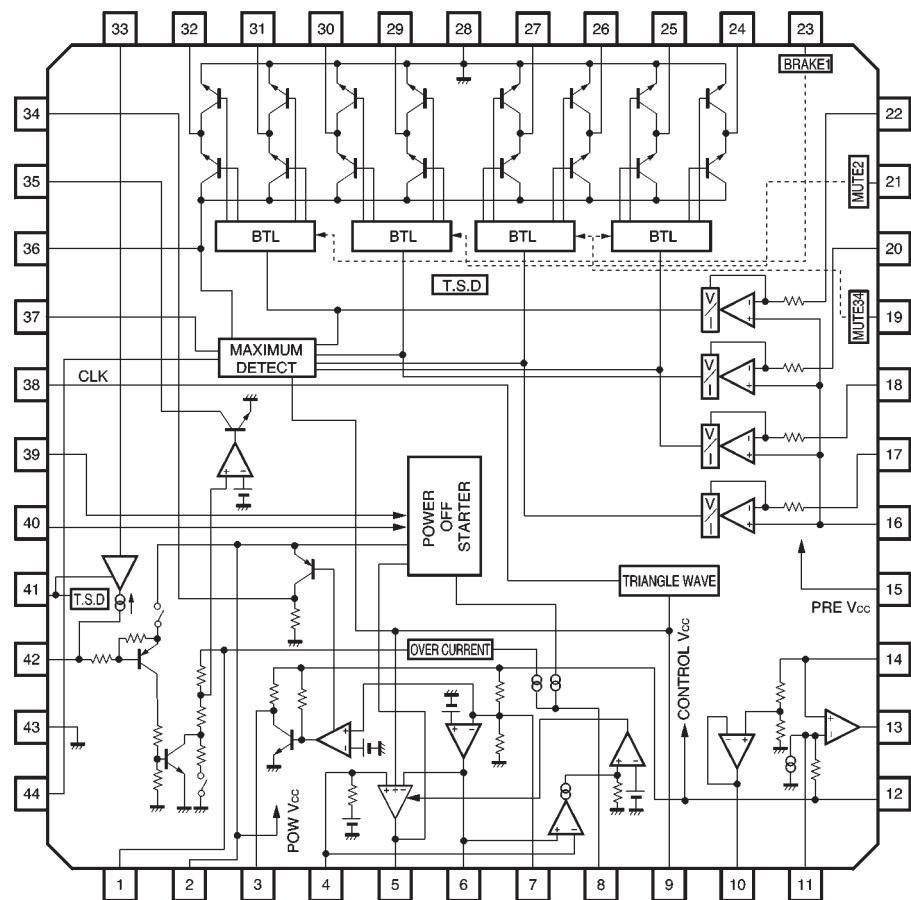
Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>cc</sub>	13.5	V
Drive output current	I <sub>o</sub>	500	mA
Power dissipation	P <sub>d</sub>	625 *	mW
Operating temperature	T <sub>opr</sub>	−30~+85	°C
Storage temperature	T <sub>stg</sub>	−85~+150	°C

\* Reduced by 5mW for each increase in Ta of 1°C over 25°C.

### ● Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control circuit power supply voltage	YSYS1	2.7	3.2	5.5	V
Pre-drive circuit power supply voltage	YSYS2	2.7	3.2	5.5	V
H-bridge power supply voltage	HV <sub>cc</sub>	—	PWM	BATT	V
Battery power supply voltage	BATT	1.5	2.4	8.0	V
Recharge circuit power supply voltage	CHGV <sub>cc</sub>	3.0	4.5	8.0	V
Ambient temperature	T <sub>a</sub>	−10	25	70	°C

## ● Block diagram



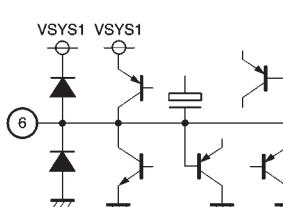
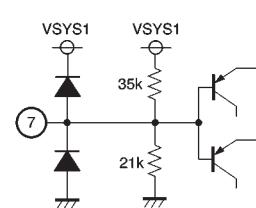
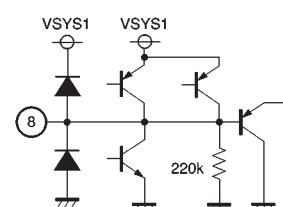
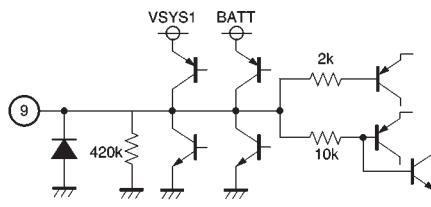
## ●Pin descriptions

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	BSEN	Battery voltage monitor	23	BRAKE1	Channel 1 brake
2	BATT	Battery power supply input	24	OUT4R	Channel 4 negative output
3	RESET	Reset detect output	25	OUT4F	Channel 4 positive output
4	DEAD	Dead-time setting	26	OUT3R	Channel 3 negative output
5	SW	Transistor drive for voltage multiplier	27	OUT3F	Channel 3 positive output
6	EO	Error amplifier output	28	POWGND	Power block power supply ground
7	EI	Error amplifier input	29	OUT2F	Channel 2 positive output
8	SPRT	Short protection setting	30	OUT2R	Channel 2 negative output
9	CT	Triangular-wave output	31	OUT1F	Channel 1 positive output
10	AREF	Audio reference output	32	OUT1R	Channel 1 negative output
11	CRP	Ripple filter smoothing	33	RCHG	Charge current setting
12	VSYS1	Control circuit power supply input	34	AMUTE	Reset invert output
13	PRP	Transistor drive for ripple filter	35	EMP	Empty detect output
14	AVcc	Ripple filter output	36	HVcc	H-bridge power supply input
15	VSYS2	Pre-drive power supply input	37	PSW	PWM transistor drive
16	VREF	Reference voltage input	38	CLK	External clock synchronizing input
17	IN3	Channel 3 control signal input	39	START	Voltage multiplier DC/DC converter start
18	IN4	Channel 4 control signal input	40	OFF	Voltage multiplier DC/DC converter OFF
19	MUTE34	Channel 3 and 4 mute	41	CHGVcc	Charging circuit power supply input
20	IN2	Channel 2 control signal input	42	SEL	Empty detect level switch
21	MUTE2	Channel 2 mute	43	PREGND	Pre section power supply ground
22	IN1	Channel 1 control signal input	44	PWMFIL	PWM phase compensation

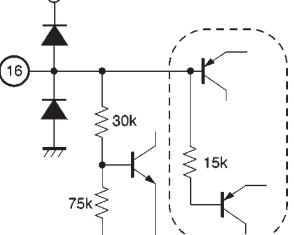
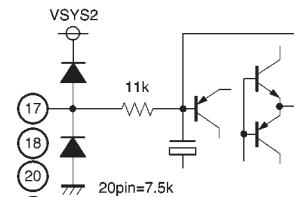
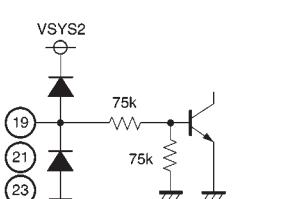
Note: The positive and negative outputs are the polarity with respect to the input.

## ● Input / output circuits

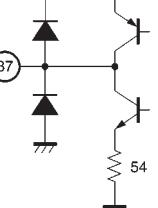
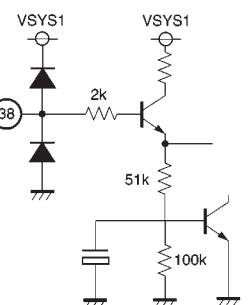
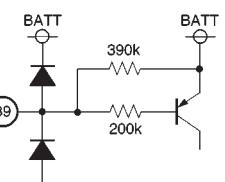
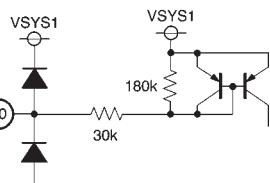
Pin No.	Pin name	Equivalent circuit
1	BSEN	
2	BATT	Battery power supply
3	RESET	
4	DEAD	
5	SW	

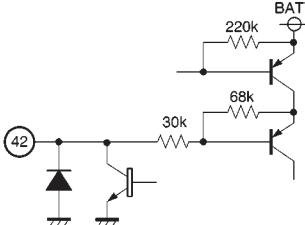
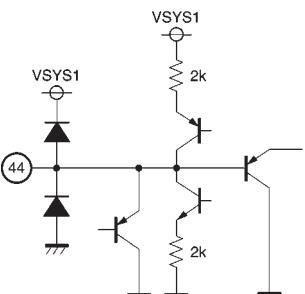
Pin No.	Pin name	Equivalent circuit
6	EO	
7	EI	
8	SPRT	
9	CT	

Pin No.	Pin name	Equivalent circuit
10	AREF	
11	CRP	
12	VSYS1	Control circuit power supply
13	PRP	
14	AVcc	
15	VSYS2	Driver pre-stage power supply

Pin No.	Pin name	Equivalent circuit
16	VREF	
17	IN3	
18	IN4	
20	IN2	
22	IN1	
19	MUTE34	
21	MUTE2	
23	BRAKE1	

Pin No.	Pin name	Equivalent circuit
24 25 26 27 28 29 30 31 32 36	OUT4R OUT4F OUT3R OUT3F POWGND OUT2F OUT2R OUT1F OUT1R HVcc	
33	RCHG	
34	AMUTE	
35	EMP	

Pin No.	Pin name	Equivalent circuit
37	PSW	
38	CLK	
39	START	
40	OFF	
41	CHGVcc	Charging circuit power supply

Pin No.	Pin name	Equivalent circuit
42	SEL	
43	PREGND	Pre block ground
44	PWMFIL	

● Electrical characteristics (unless otherwise noted,  $T_a = 25^\circ\text{C}$ ,  $\text{BATT} = 2.4\text{V}$ ,  $\text{VSYS1} = \text{VSYS2} = 3.2\text{V}$ ,  $\text{VREF} = 1.6\text{V}$ ,  $\text{CHGV}_{\text{cc}} = 0\text{V}$ , and  $\text{fCLK} = 88.2\text{kHz}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
[Total circuit]						
BATT standby current	$I_{\text{ST}}$	—	0	3	$\mu\text{A}$	$\text{BATT}=9\text{V}$ , $\text{VSYS1}=\text{VSYS2}=\text{VREF}=0\text{V}$
BATT no-load power supply current	$I_{\text{BAT}}$	—	2.5	4.0	mA	$\text{HV}_{\text{cc}}=0.45\text{V}$ , $\text{MUTE34}=3.2\text{V}$
VSYS1 no-load power supply current	$I_{\text{SYS1}}$	—	3.3	4.5	mA	$\text{HV}_{\text{cc}}=0.45\text{V}$ , $\text{MUTE34}=3.2\text{V}$ , $\text{EI}=0\text{V}$
VSYS2 no-load power supply current	$I_{\text{SYS2}}$	—	4.1	5.5	mA	$\text{HV}_{\text{cc}}=0.45\text{V}$ , $\text{MUTE34}=3.2\text{V}$
CHGV <sub>cc</sub> no-load power supply current	$I_{\text{CGVCC}}$	—	0.65	2.0	mA	$\text{CHGV}_{\text{cc}}=4.5\text{V}$ , $\text{ROUT}=\text{OPEN}$
[H-bridge drive block]						
Channels 1, 3, 4, and 2 voltage gain	$G_{\text{VC134}}$ $G_{\text{VC2}}$	12 21.5	14 23.5	16 25.5	dB dB	—
Positive / negative voltage gain differential	$\Delta G_{\text{VC}}$	—2	0	2	dB	—
Channels 1, 3, 4, and 2 IN pin input resistance	$R_{\text{IN134}}$ $R_{\text{IN2}}$	9 6	11 7.5	13 9	$\text{k}\Omega$ $\text{k}\Omega$	$\text{IN}=1.7\text{and }1.8\text{V}$
Maximum output amplitude	$V_{\text{OUT}}$	1.9	2.1	—	V	$R_{\text{L}}=8\Omega$ , $\text{HV}_{\text{cc}}=\text{BATT}=4\text{V}$ , $\text{IN}=0\text{--}3.2\text{V}$
Lower-side transistor saturation voltage	$V_{\text{SATL}}$	—	240	400	mV	$I_{\text{O}}=-300\text{mA}$ , $\text{IN}=0$ and $3.2\text{V}$
Upper-side transistor saturation voltage	$V_{\text{SATU}}$	—	240	400	mV	$I_{\text{O}}=300\text{mA}$ , $\text{IN}=0$ and $3.2\text{V}$
Input offset voltage	$V_{\text{OI}}$	—8	0	8	mV	—
Channels 1, 3, 4, and 2 output offset voltage	$V_{\text{OO134}}$ $V_{\text{OO2}}$	—50 —130	0 0	50 130	mV mV	$\text{VREF}=\text{IN}=1.6\text{V}$
Dead-band width	$V_{\text{DB}}$	—10	0	10	mV	—
BRAKE1 on threshold voltage	$V_{\text{BRON}}$	2.0	—	—	V	$\text{IN1}=1.8\text{V}$
BRAKE1 off threshold voltage	$V_{\text{BROFF}}$	—	—	0.8	V	$\text{IN1}=1.8\text{V}$
MUTE2 on threshold voltage	$V_{\text{M2ON}}$	2.0	—	—	V	$\text{IN2}=1.8\text{V}$
MUTE2 off threshold voltage	$V_{\text{M2OFF}}$	—	—	0.8	V	$\text{IN2}=1.8\text{V}$
MUTE34 on threshold voltage	$V_{\text{M34ON}}$	—	—	0.8	V	$\text{IN3}=\text{IN4}=1.8\text{V}$
MUTE34 off threshold voltage	$V_{\text{M34OFF}}$	2.0	—	—	V	$\text{IN3}=\text{IN4}=1.8\text{V}$
VREF on threshold voltage	$V_{\text{REFON}}$	1.2	—	—	V	$\text{IN1}=\text{IN2}=\text{IN3}=\text{IN4}=1.8\text{V}$
VREF off threshold voltage	$V_{\text{REFOFF}}$	—	—	0.8	V	$\text{IN1}=\text{IN2}=\text{IN3}=\text{IN4}=1.8\text{V}$
BRAKE1 brake current	$I_{\text{BRAKE1}}$	4	7	10	mA	Current difference between when BRAKE1 pin is high level and low level.

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
[PWM power supply drive]						
PSW sink current	$I_{PSW}$	10	13	17	mA	$IN1=2.1V$
HVcc level shift voltage	$V_{SHIF}$	0.35	0.45	0.55	V	$IN1=1.8V$ , $HV_{cc}-OUT1F$
HVcc leak current	$I_{HLK}$	—	0	5	$\mu A$	$HV_{cc}=9V$ , $VSYS1=VSYS2=BATT=0V$
PWM amp transfer gain	$G_{PWM}$	1 / 60	1 / 50	1 / 40	1 / $k\Omega$	$IN1=1.8V$ , $HV_{cc}=1.2V \sim 1.4V$
[DC/DC converter]						
⟨Error amplifier block⟩						
VSYS1 threshold voltage	$V_{SITH}$	3.05	3.20	3.35	V	—
EO output high level voltage	$V_{EOH}$	1.4	1.6	—	V	$EI=0.7V$ , $Io=-100 \mu A$
EO output low level voltage	$V_{EOL}$	—	—	0.3	V	$EI=1.3V$ , $Io=100 \mu A$
⟨Short protect block⟩						
SPRT voltage normal	$V_{SPR}$	—	0	0.1	V	$EI=1.3V$
SPRT current 1, EO=high level	$I_{SPR1}$	6	10	16	$\mu A$	$EI=0.7V$
SPRT current 2, OFF=low level	$I_{SPR2}$	12	20	32	$\mu A$	$EI=1.3V$ , OFF=0V
SPRT current 3, overload	$I_{SPR3}$	12	20	32	$\mu A$	$EI=1.3V$ , BATT=9.5V
SPRT pin impedance	$R_{SPR}$	175	220	265	$k\Omega$	—
SPRT threshold voltage	$V_{SPTH}$	1.10	1.20	1.30	V	$EI=0.7V$ , CT=0V
Over voltage protection detection voltage	$V_{HVPR}$	8.0	8.4	9.0	V	BSEN voltage
⟨Transistor drive⟩						
SW output high level voltage 1	$V_{SW1H}$	0.78	0.98	1.13	V	$BATT=CT=1.5V$ $VSYS1=VSYS2=OV$ , $Io=-2mA$ , at start
SW output high level voltage 2	$V_{SW2H}$	1.0	1.50	—	V	$CT=0V$ , $Io=-10mA$ , $EI=0.7V$ , SPRT=0V
SW output low level voltage 2	$V_{SW2L}$	—	0.3	0.45	V	$CT=2V$ , $Io=10mA$
SW oscillator frequency 1	$f_{sw1}$	65	80	95	kHz	$CT=470pF$ , $VSYS1=VSYS2=0V$ , At start
SW oscillator frequency 2	$f_{sw2}$	60	70	82	kHz	$CT=470pF$ , CLK=0V
SW oscillator frequency 3	$f_{sw3}$	—	88.2	—	kHz	$CT=470pF$
SW minimum pulse width	$T_{SWMIN}$	0.01	—	0.6	$\mu sec$	$CT=470pF$ , EO=0.5→0.7V sweep
Pulse duty at start	$D_{sw1}$	40	50	60	%	$CT=470pF$ , $VSYS1=VSYS2=ON$
Max. duty at free run	$D_{sw2}$	70	80	90	%	$EI=0.7V$ , $CT=470pF$ , CLK=0V
Max. duty with synchronized CLK	$D_{sw3}$	65	75	85	%	$EI=0.7V$ , $CT=470pF$

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>⟨Dead-time block⟩</b>						
Dead pin impedance	$R_{DEAD}$	52	65	78	$k\Omega$	—
Dead pin output voltage	$V_{DEAD}$	0.78	0.88	0.98	V	—
<b>⟨Interface block⟩</b>						
OFF pin threshold voltage	$V_{OFTH}$	—	—	$V_{SYS1}-2.0$	V	$EI=1.3V$
OFF pin bias current	$I_{OFF}$	75	95	115	$\mu A$	$OFF=0V$
START pin off threshold voltage	$V_{STATH1}$	—	—	$BATT-1.0$	V	$V_{SYS1}=V_{SYS2}=0V$ , $CT=2V$
START pin off threshold voltage	$V_{STATH2}$	$BATT-0.3$	—	—	V	$V_{SYS1}=V_{SYS2}=0V$ , $CT=2V$
START pin bias current	$I_{START}$	13	16	19	$\mu A$	$START=0V$
CLK pin threshold high level voltage	$V_{CLKTHH}$	2.0	—	—	V	—
CLK pin threshold low level voltage	$V_{CLKTHL}$	—	—	0.8	V	—
CLK pin bias current	$I_{CLK}$	—	—	10	$\mu A$	$CLK=3.2V$
<b>⟨Start circuit⟩</b>						
Start switch voltage	$V_{STNM}$	2.3	2.5	2.7	V	$V_{SYS1}=V_{SYS2}=0V \rightarrow 3.2V$ , $START=0V$
Start switch hysteresis width	$V_{SNHS}$	130	200	300	mV	$START=0V$
Discharge release voltage	$V_{DIS}$	1.63	1.83	2.03	V	—
<b>[Empty detect block]</b>						
Empty detect voltage 1	$V_{EMPT1}$	2.1	2.2	2.3	V	$VSEL=0V$
Empty detect voltage 2	$V_{EMPT2}$	1.7	1.8	1.9	V	$ISEL=-2\mu A$
Empty detect hysteresis 1	$V_{EMHS1}$	25	50	100	mV	$VSEL=0V$
Empty detect hysteresis 2	$V_{EMHS2}$	25	50	100	mV	$ISEL=-2\mu A$
EMP output voltage	$V_{EMP}$	—	—	0.5	V	$I_o=1mA$ , $BSEN=1V$
EMP output leak current	$I_{EMPL}$	—	—	1.0	$\mu A$	$BSEN=2.4V$
BSEN input resistance	$R_{BSEN}$	17	23	27	$k\Omega$	$VSEL=0V$
BSEN leak current	$I_{BSNL}$	—	—	1.0	$\mu A$	$V_{SYS1}=V_{SYS2}=0V$ , $BSEN=4.5V$
SEL detect voltage	$V_{SELTH}$	1.5	—	—	V	$V_{SELTH}=BATT-SEL$ , $BSEN=2V$
SEL detect current	$I_{SELT}$	—2	—	—	$\mu A$	—

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
[Reset circuit]						
VSYS1 pin reset threshold voltage ratio	$H_{SRT}$	85	90	95	%	Ratio to error amplifier threshold voltage
Reset detect hysteresis width	$V_{RSTHs}$	25	50	100	mV	—
RESET output voltage	$V_{RST}$	—	—	0.5	V	$I_o=1mA$ , VSYS1=VSYS2=2.8V
RESET pin pull-up resistance	$R_{RST}$	72	90	108	k $\Omega$	—
AMUTE output voltage 1	$V_{AMT1}$	BATT —0.4	—	BATT	V	$I_o=-1mA$ VSYS1=VSYS2=2.8V
AMUTE output voltage 2	$V_{AMT2}$	BATT —0.4	—	BATT	V	$I_o=-1mA$ VSYS1=VSYS2=0V, START=0V
AMUTE pull-down resistance	$R_{AMT}$	77	95	113	k $\Omega$	—
[Ripple filter]						
Voltage between AVcc and VSYS1	$V_{AVCC}$	0.22	0.24	0.27	V	$I_o=-5mA$ , external PNP, CRP=OPEN
CRP input resistance	$R_{CRP}$	18	22	26	k $\Omega$	—
AVcc discharge current	$I_{AVCC}$	1.7	2.5	4.0	mA	VSYS1=VSYS2=2.8V
PRP pull-up resistance	$R_{PRP}$	21	27	33	k $\Omega$	CRP=2.8V, AVcc=3.0V
PRP drive current sink	$I_{PRP}$	150	400	600	$\mu A$	CRP=3.0V, AVcc=2.8V
[Charge circuit block]						
RCHG bias voltage	$V_{RCHG}$	0.71	0.81	0.91	V	$CHGV_{cc}=4.5V$ , RCHG=1.8k $\Omega$
RCHG output resistance	$R_{RCHG}$	0.75	0.95	1.20	k $\Omega$	$CHGV_{cc}=4.5V$ , RCHG=0.5 and 0.6V
SEL leak current 1	$I_{SELLK}$	—	—	1.0	$\mu A$	$CHGV_{cc}=4.5V$ , RCHG=OPEN
SEL leak current 2	$I_{SELLK}$	—	—	1.0	$\mu A$	$CHGV_{cc}=0.6V$ , RCHG=1.8k $\Omega$
SEL saturation voltage	$V_{SELCG}$	—	0.45	1.0	V	$CHGV_{cc}=4.5V$ , $I_o=300mA$ , RCHG=0 $\Omega$
[Audio reference circuit]						
AREF output voltage	$V_{AREF}$	1.4	1.5	1.6	V	AVcc=3V
AREF output impedance	$R_{AREF}$	3.3	4.0	4.7	k $\Omega$	AVcc=3V
AREF discharge current	$I_{AREF}$	1.7	2.5	4.0	mA	VSYS1=VSYS2=2.6V

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### ● Circuit operation

#### (1) Empty detector block

When the voltage applied to the BSEN pin falls below the detector voltage, EMP (pin 35) goes from high level to low level (open-collector output). The detector voltage has 50mV (Typ.) of hysteresis to prevent output chattering. Use SEL (pin 42) to switch the detection voltage as shown below.

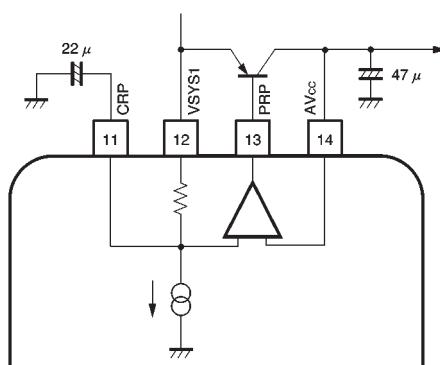
SEL	Detect voltage	Return voltage
"L"	2.2V (Typ.)	2.25V (Typ.)
HIGH-Z	1.8V (Typ.)	1.85V (Typ.)

#### (2) Reset circuit block

At about 90% (Typ.) of the DC/DC comparator output voltage, RESET (pin 3) goes from low level to high level, and AMUTE (pin 34) goes from high level to low level. The reset voltage has 50mV (Typ.) of hysteresis to prevent output chattering.

#### (3) Ripple filter circuit

By connecting an external PNP transistor, a voltage of (VSYS1 0.24)V is supplied from AV<sub>cc</sub> (pin 14). Connect a ripple bypass capacitor between CRIP (pin 11) and GND.



#### (4) Audio reference circuit block

One half of the AV<sub>cc</sub> voltage (pin 14) generated by the ripple filter circuit is output from AREF (pin 10). The output impedance is 4.0kΩ (Typ.).

#### (5) Charging circuit block

The power supply for the charging circuit block is CHGV<sub>cc</sub> (pin 41), and is independent from the other circuits. The resistance between RCHG (pin 33) and GND sets the charging current. This current is drawn from SEL.

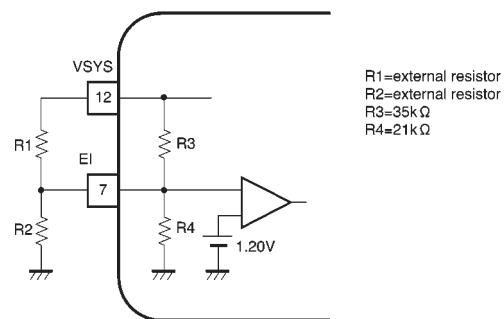
A thermal shutdown circuit is provided, and when the chip temperature reaches 150°C (Typ.) the charging current is cut. The chip starts operating again at about 120°C (Typ.).

#### (6) DC/DC converter block

##### 1) Output voltage

A 3.2V (Typ.) voltage multiplier circuit can be constructed using external components. This voltage can be varied with the addition of an external resistor. The setting method is as follows.

$$VSYS1 = 1.20 \times \frac{\frac{R1 \cdot R3}{R1 + R3} + \frac{R2 \cdot R4}{R2 + R4}}{\frac{R2 \cdot R4}{R2 + R4}} \text{ (V)}$$



#### 2) Short protect function

When the error amplifier output (pin 6) has switched to the high-level state, SPRT (pin 8) is charged, and when the voltage reaches 1.2V (Typ.), the SW (pin 5) switching stops. The time until switching stops is set by the capacitor connected to SPRT (pin 8) according to the following formula.

$$t = CSPRT \times \frac{VTH}{ISPRT} \text{ (sec)}$$

(VTH = 1.20V, ISPRT = 10μA)

#### 3) Soft start function

The soft start function operates when a capacitor is connected between DEAD (pin 4) and GND. Also, the maximum duty can be varied by connecting a resistor to pin 4.

$$t = CDEAD \times R \text{ (sec)} \quad (R = 65kΩ)$$

## 4) Power off function

When low-level is applied to OFF (pin 40), SPRT (pin 8) is charged, and when the voltage reaches 1.2V (Typ.), the SW (pin 5) switching stops. The time until switching stops is set by the capacitor connected to SPRT (pin 8) according to the following formula.

$$t = CSPRT \times \frac{V_{TH}}{I_{OFF}} \text{ (sec)}$$

( $V_{TH} = 1.20V$ ,  $I_{OFF} = 20\mu A$ )

## 5) Over voltage protection circuit

When the voltage applied to BSEN (pin 1) reaches 8.4V (Typ.), SPRT (pin 8) is charged, and when the voltage reaches 1.2V (Typ.), the SW (pin 5) switching stops. The time until switching stops is set by the capacitor connected to SPRT (pin 8) according to the following formula.

$$t = CSPRT \times \frac{V_{TH}}{I_{HV}} \text{ (sec)}$$

( $V_{TH} = 1.20V$ ,  $I_{HV} = 20\mu A$ )

## (7) H-bridge driver block

## 1) Gain setting

The driver input resistance is  $11k\Omega$  (Typ.) for channels 1, 3, and 4, and  $7.5k\Omega$  for channel 2. Set the gain according to the following formula.

ch1	$GV = 20 \log \left  \frac{55k}{11k+R} \right  \text{ (dB)}$
ch2	$GV = 20 \log \left  \frac{110k}{7.5k+R} \right  \text{ (dB)}$

R: Externally-connected input resistor

The driver output stage power supply is HVCC (pin 36), and the bridge circuit power supply is VSYS2 (pin 15). Connect a bypass capacitor between these two power supplies (approximately  $0.1\mu F$ ).

## 2) Mute function

Of the four drivers, channel 1 has a brake function, and the other channels have a mute function.

When BRAKE1 (pin 23) is set to high level, both channel 1 outputs go low level, and the circuit enters brake mode. When MUTE2 (pin 21) is set to high level, the channel 2 output is muted.

When MUTE34 (pin 19) is set to high level, the channel 3 and 4 outputs are muted.

## 3) VREF drop mute

When the voltage applied to VREF (pin 16) is 1.0V or less (Typ.), the driver outputs are set to high impedance.

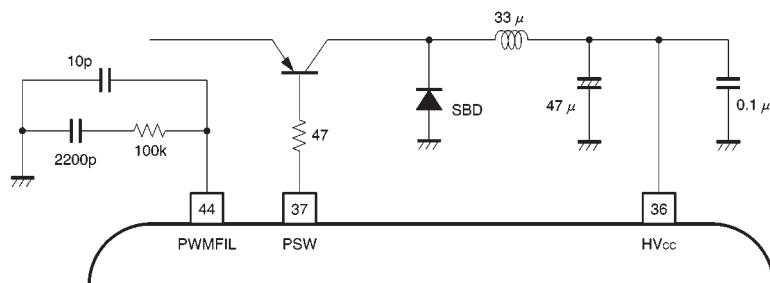
## 4) Thermal shutdown

When the chip temperature reaches  $150^\circ C$  (Typ.) the output current is cut. The chip starts operating again at about  $120^\circ C$  (Typ.).

## (8) PWM power supply drive block

This detects the maximum output level from among the four channels, and supplies the load drive power supply for the PWM.

The external components are a PNP transistor, coil, Schottky diode, and capacitor.



## ● Application example

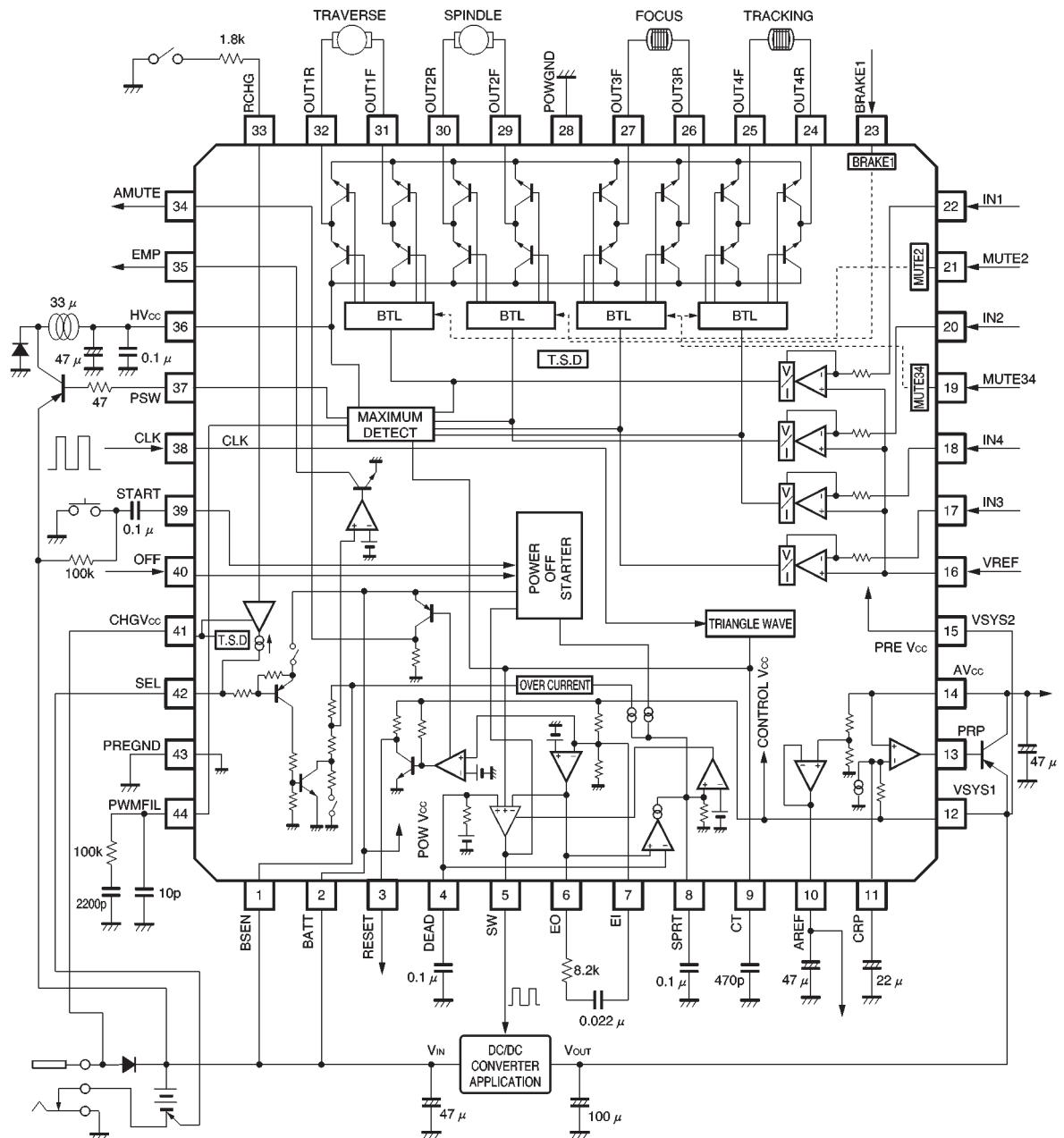
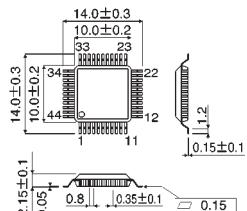


Fig.4

## ● External dimensions (Units: mm)



QFP44