NPN Silicon Power Transistor

High Voltage SWITCHMODE Series

Designed for use in electronic ballast (light ballast) and in SWITCHMODE Power supplies up to 50 W.

Features

- Improved Efficiency Due to:
 - ◆ Low Base Drive Requirements (High and Flat DC Current Gain h_{FE})
 - ◆ Low Power Losses (On-State and Switching Operations)
 - Fast Switching: $t_{fi} = 100 \text{ ns (typ)}$ and $t_{si} = 3.2 \mu \text{s (typ)}$
 - @ $I_C = 2.0 \text{ A}$, $I_{B1} = I_{B2} = 0.4 \text{ A}$
- Full Characterization at 125°C
- Tight Parametric Distributions Consistent Lot-to-Lot
- These Devices are Pb-Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	V _{CEO}	400	Vdc
Collector-Base Breakdown Voltage	V _{CES}	700	Vdc
Emitter-Base Voltage	V _{EBO}	9.0	Vdc
Collector Current - Continuous - Peak (Note 1)	I _C	5.0 10	Adc
Base Current	I _B	2.0	Adc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	75 0.6	W W/°C
Operating and Storage Temperature	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.65	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

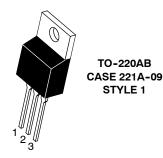
1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



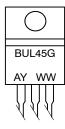
ON Semiconductor®

http://onsemi.com

POWER TRANSISTOR 5.0 AMPERES, 700 VOLTS, 35 AND 75 WATTS



MARKING DIAGRAM



BUL45 = Device Code A = Assembly Location

Y = Year

WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
BUL45G	TO-220 (Pb-Free)	50 Units / Rail

1

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

ELECTRICAL CHARACTE	Characteristic			Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS			- cymine.		.,,,,	max	5	
	altono (l. 100 m.A.	1 0F m	LN	l v	400		_	Vdc
Collector-Emitter Sustaining Vo			п)	V _{CEO(sus)}		-		
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , I _B = 0)			I _{CEO}	-	-	100	μAdc	
Collector Cutoff Current (V _{CE} =	Rated V_{CES} , $V_{EB} = $	0) T _C = 125	°C)	ICES	-	-	10 100	μAdc
Emitter Cutoff Current (V _{EB} = 9	.0 Vdc, I _C = 0)			I _{EBO}	-	-	100	μAdc
ON CHARACTERISTICS						-		
Base-Emitter Saturation Voltag				V _{BE(sat)}				Vdc
$(I_C = 1.0 \text{ Adc}, I_B = 0.2 \text{ Adc})$ $(I_C = 2.0 \text{ Adc}, I_B = 0.4 \text{ Adc})$					-	0.84 0.89	1.2 1.25	
Collector-Emitter Saturation Vo		I _B = 0.2 A T _C = 125		V _{CE(sat)}	-	0.175 0.150	0.25	Vdc
Collector Emitter Saturation Va				V		0.150	0.4	Vdc
Collector-Emitter Saturation Vo		$T_{\rm C} = 0.4 P$		V _{CE(sat)}	-	0.25	-	vuc
DC Current Gain (I _C = 0.3 Adc,	V _{CE} = 5.0 Vdc)	T 405		h _{FE}	14	-	34	-
(I _C = 2.0 Adc, V _{CF} = 1.0 V		$T_{\rm C} = 125$	(°C)		7.0	32 14	-	
(5	, ($T_{\rm C} = 125$	°C)		5.0	12	-	
$(I_C = 10 \text{ mAdc}, V_{CE} = 5.0)$					10	22	-	
DYNAMIC CHARACTERISTICS				1	ı		ı	ı
Current Gain Bandwidth (I _C = 0	.5 Adc, V _{CE} = 10 Vd	c, f = 1.0	MHz)	f _T	-	12		MHz
Output Capacitance (V _{CB} = 10	Vdc, $I_E = 0$, $f = 1.0 \text{ N}$	1Hz)		C _{ob}	-	50	75	pF
Input Capacitance (V _{EB} = 8.0 V	(dc)			C _{ib}	-	920	1200	pF
	(I _C = 1.0 Adc I _{B1} = 100 mAdc V _{CC} = 300 V)	1.0 μs	(T _C = 125°C)	V _{CE} (Dyn sat)	-	1.75 4.4	- -	Vdc
Dynamic Saturation Voltage:		3.0 μs			-	0.5	-	
Determined 1.0 μs and 3.0 μs	,	0.0 μο	(T _C = 125°C)		-	1.0	-	
respectively after rising I _{B1} reaches 90% of final I _{B1}	(I _C = 2.0 Adc I _{B1} = 400 mAdc V _{CC} = 300 V)	1.0 μs	(T _C = 125°C)		-	1.85 6.0	-	
(see Figure 18)		3.0 μs	(T _C = 125°C)		-	0.5 1.0	-	
SWITCHING CHARACTERIST	ICS: Resistive Load	d d	,		<u> </u>	1	Į	
Turn-On Time	(I _C = 2.0 Adc, I _{B1} =		4 Adc	t _{on}	_	75	110	ns
	Pulse Width = 20 µ	ıs,	$(T_C = 125^{\circ}C)$	-011	-	120	-	
Turn-Off Time	Duty Cycle < 20% V _{CC} = 300 V (T _C = 125°C)			t _{off}	-	2.8 3.5	3.5 -	μs
SWITCHING CHARACTERIST	ICS: Inductive Load	d (V _{CC} =	15 Vdc, L _C = 200	μ H, $V_{clamp} = 30$	00 Vdc)	-		
Fall Time	(I _C = 2.0 Adc, I _{B1} = 0.4 Adc I _{B2} = 0.4 Adc) (T _C = 125°C)			t _{fi}	70 -	200	170 -	ns
Storage Time	,		,	t _{si}	2.6	-	3.8	μs
	 		$(T_C = 125^{\circ}C)$		-	4.2	-	
Crossover Time			(T _C = 125°C)	t _c	-	230 400	350 -	ns
Fall Time	(I _C = 1.0 Adc, I _{B1} = 100 mAdc I _{B2} = 0.5 Adc) (T _C = 125°C)			t _{fi}	-	110 100	150 -	ns
Storage Time	$(T_C = 125^{\circ}C)$			t _{si}	-	1.1 1.5	1.7	μs
Crossover Time	(IC = 125 C)			t _c	-	170	250	ns
$(T_C = 125^{\circ}C)$				-	170	-		
Fall Time	$(I_C = 2.0 \text{ Adc}, I_{B1} = 250 \text{ mAdc} $ $I_{B2} = 2.0 \text{ Adc})$ $(T_C = 125^{\circ}C)$			t _{fi}	-	80	120	ns
Storage Time	$(T_C = 125^{\circ}C)$			t _{si}	-	0.6	0.9	μs
Crossover Time	(T _C = 125°C)			t _c	-	175	300	ns

TYPICAL STATIC CHARACTERISTICS

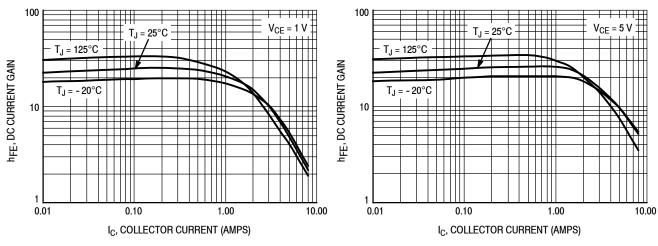


Figure 1. DC Current Gain @ 1 Volt

Figure 2. DC Current Gain at @ 5 Volts

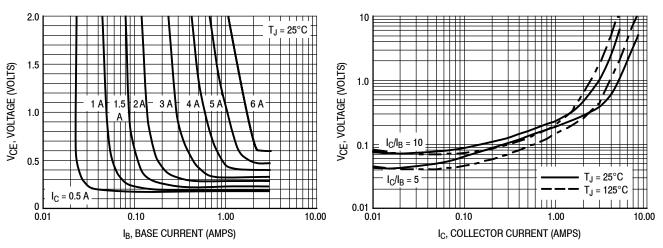


Figure 3. Collector-Emitter Saturation Region

Figure 4. Collector-Emitter Saturation Voltage

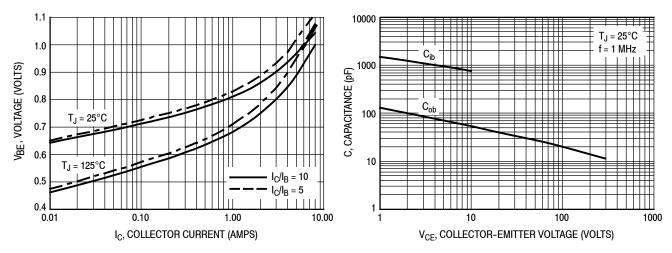
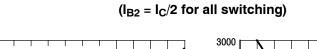


Figure 5. Base-Emitter Saturation Region

Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS (I_{R2} = I_C/2 for all switching)



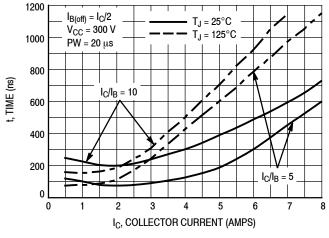
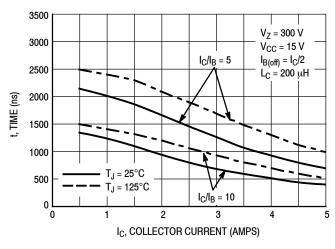


Figure 7. Resistive Switching, ton

Figure 8. Resistive Switching, toff



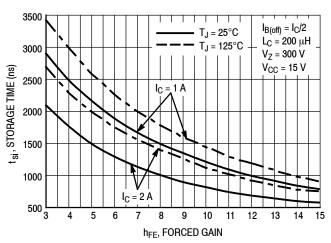
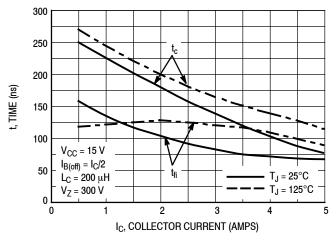


Figure 9. Inductive Storage Time, tsi

Figure 10. Inductive Storage Time, tsi(hFE)



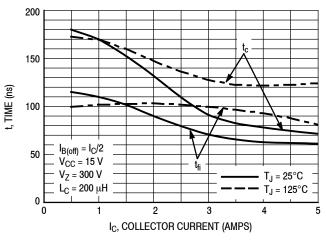


Figure 11. Inductive Switching, t_c & t_{fi} , $I_C/I_B = 5$

Figure 12. Inductive Switching, t_c & t_{fi} , I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS $(I_{B2} = I_C/2 \text{ for all switching})$

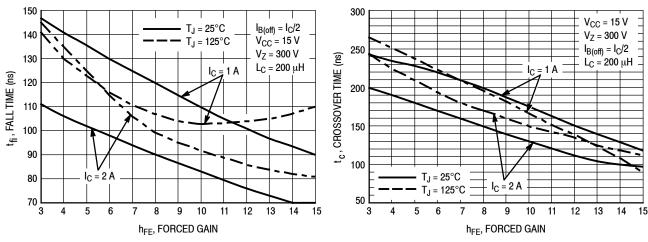


Figure 13. Inductive Fall Time, tfi(hFE)

Figure 14. Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

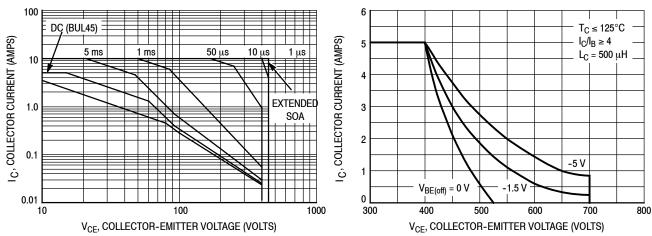


Figure 15. Forward Bias Safe Operating Area

POWER DERATING FACTOR

0.2

20

40

60

Safe operating area curves indicate I_C – V_{CE} limit that must be observed for reliable operation; i. must not be subjected to greater dissipation indicate. The data of Figure 15 is based on T_C variable depending on power level. Second belimits are valid for duty cycles to 10% but must $T_C \ge 25^{\circ}C$. Second breakdown limitations do not as thermal limitations. Allowable current at the valid for duty cycles to 10% but must $T_C \ge 25^{\circ}C$. Second breakdown limitations do not as thermal limitations. Allowable current at the valid for duty cycles to 10% but must $T_C \ge 25^{\circ}C$. Second breakdown limitations do not as thermal limitations. Allowable current at the valid for duty cycles to 10% but must $T_C \ge 25^{\circ}C$. Second breakdown limitations do not as thermal limitations.

T_C, CASE TEMPERATURE (°C)

Figure 17. Forward Bias Power Derating

100

120

140

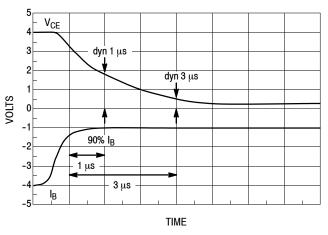
160

THERMAL DERATING

80

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25$ °C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. T_{J(pk)} may be calculated from the data in Figures 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse-biased. The safe level is specified as a reverse-biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

Figure 16. Reverse Bias Switching Safe Operating Area



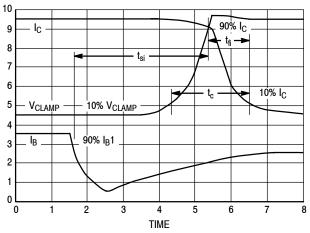


Figure 18. Dynamic Saturation Voltage Measurements

Figure 19. Inductive Switching Measurements

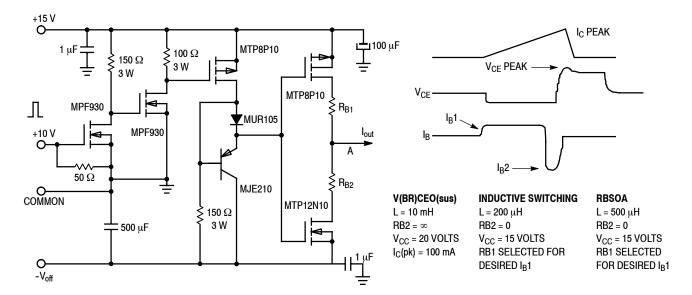


Table 1. Inductive Load Switching Drive Circuit

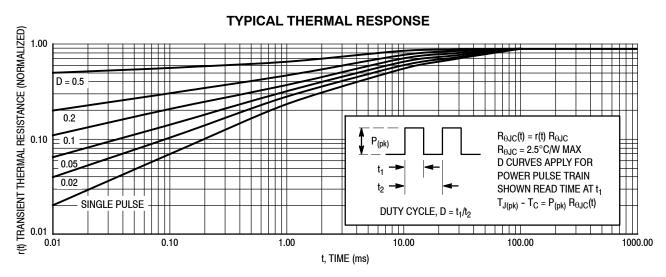


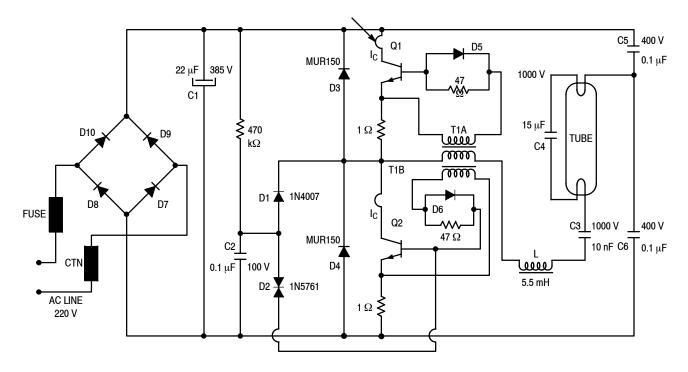
Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45

The BUL45 Bipolar Power Transistors were specially designed for use in electronic lamp ballasts. A circuit designed by ON Semiconductor applications was built to

Secondaries: T1A: 4 turns

T1B: 4 turns

demonstrate how well these devices operate. The circuit and detailed component list are provided below.



Components Lists

Q1 =	Q2 = BUL45 Transistor	All resistors are 1/4 Watt, ±5%
D1 =	1N4007 Rectifier	$R1 = 470 \text{ k}\Omega$
D2 =	1N5761 Rectifier	$R2 = R3 = 47 \Omega$
D3 =	D4 = MUR150	R4 = R5 = 1 Ω (these resistors are optional, and
D5 =	D6 = MUR105	might be replaced by a short circuit)
D7 =	D8 = D9 = D10 = 1N400	C1 = 22 μF/385 V
CTN =	47 Ω @ 25°C	$C2 = 0.1 \mu\text{F}$
L =	RM10 core, A1 = 400, B51 (LCC) 75 turns,	C3 = 10 nF/1000 V
	wire \emptyset = 0.6 mm	C4 = 15 nF/1000 V
T1 =	FT10 toroid, T4A (LCC)	$C5 = C6 = 0.1 \mu F/400 V$
	Primary: 4 turns	

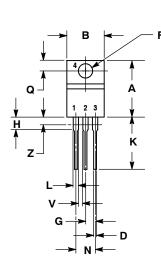
NOTES:

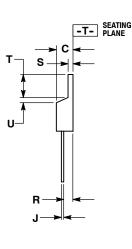
- 1. Since this design does not include the line input filter, it cannot be used "as-is" in a practical industrial circuit.
- 2. The windings are given for a 55 Watt load. For proper operation they must be re-calculated with any other loads.

Figure 21. Application Example

PACKAGE DIMENSIONS

TO-220 CASE 221A-09 ISSUE AG





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
 V14 5M 1982
- Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
- DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.036	0.64	0.91
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
Н	0.110	0.161	2.80	4.10
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

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