**MOTOROLA**
SEMICONDUCTOR ————
TECHNICAL DATA

## *Advance Information*
# 16M CMOS Dynamic RAM Family
## Fast Page Mode, x4, 2K and 4K Refresh

The family of 16M dynamic RAMs is fabricated using 0.5μ CMOS high–speed sili-con–gate process technology. It includes devices organized as 4,194,304 four–bit words. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The x4 devices with 4096 cycle refresh (MCM516400B) require 12 address lines (12 rows, 10 columns), while the x4 devices with 2048 cycle refresh (MCM517400B) re-quire only 11 address lines.

These devices are packaged in a standard 300 mil J–lead small outline package (SOJ) and a 300 mil thin–small–outline package (TSOP).

- Three–State Data Output
- Fast Page Mode
- TTL–Compatible Inputs and Outputs
- RAS–Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM517400B = 32 ms
- 4096 Cycle Refresh: MCM516400B = 64 ms
- Fast Access Time ($t_{RAC}$):
  MCM51x400B–50 = 50 ns (Max)
  MCM51x400B–60 = 60 ns (Max)
  MCM51x400B–70 = 70 ns (Max)
- Low Active Power Dissipation:
  MCM516400B–50 = 550 mW (Max)
  MCM516400B–60 = 440 mW (Max)
  MCM516400B–70 = 385 mW (Max)
  MCM517400B–50 = 715 mW (Max)
  MCM517400B–60 = 605 mW (Max)
  MCM517400B–70 = 523 mW (Max)
- Low Standby Power Dissipation:
  All Devices = 11 mW (Max, TTL Levels)
  All Devices = 5.5 mW (Max, CMOS Levels)
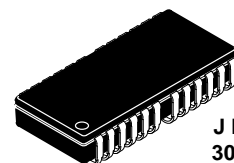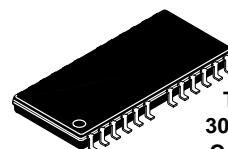
---

**4M x 4**

**MCM516400B**
**Fast Page Mode
4096 Cycle Refresh**

**MCM517400B**
**Fast Page Mode
2048 Cycle Refresh**

---



**J PACKAGE
300 MIL SOJ
CASE 880A–02**

**T PACKAGE
300 MIL TSOP II
CASE 892A–02**

---

**PIN ASSIGNMENT**
**300 MIL SOJ**
**300 MIL TSOP**

| | | | |
|---|---|---|---|
| $V_{CC}$ | 1 | 26 | $V_{SS}$ |
| DQ0 | 2 | 25 | DQ3 |
| DQ1 | 3 | 24 | DQ2 |
| $\overline{W}$ | 4 | 23 | $\overline{CAS}$ |
| $\overline{RAS}$ | 5 | 22 | $\overline{G}$ |
| A11R OR NC * | 6 | 21 | A9 |
| A10R OR A10 * | 8 | 19 | A8 |
| A0 | 9 | 18 | A7 |
| A1 | 10 | 17 | A6 |
| A2 | 11 | 16 | A5 |
| A3 | 12 | 15 | A4 |
| $V_{CC}$ | 13 | 14 | $V_{SS}$ |

\* 4096 Cycle Refresh or
2048 Cycle Refresh
(R suffix = Row Address)

---

| **PIN NAMES** | |
|---|---|
| A0 – A11 . . . . . . . . . . . . . . . Address Input | $\overline{CAS}$ . . . . . . . . . . Column Address Strobe |
| DQ0 – DQ3 . . . . . . . . . Data Input/Output | $V_{CC}$ . . . . . . . . . . . . . . Power Supply (+ 5 V) |
| $\overline{G}$ . . . . . . . . . . . . . . . . . . . . . Output Enable | $V_{SS}$ . . . . . . . . . . . . . . . . . . . . . . . . . Ground |
| $\overline{W}$ . . . . . . . . . . . . . . . . Read/Write Enable | NC . . . . . . . . . . . . . . . . . . . . No Connection |
| $\overline{RAS}$ . . . . . . . . . . . . . Row Address Strobe | |

---

This document contains information on a new product. Specifications and information herein are subject to change without notice.

**10/95**

  **MOTOROLA**

## BLOCK DIAGRAMS
### 4096 CYCLE REFRESH BLOCK DIAGRAM
### MCM516400B
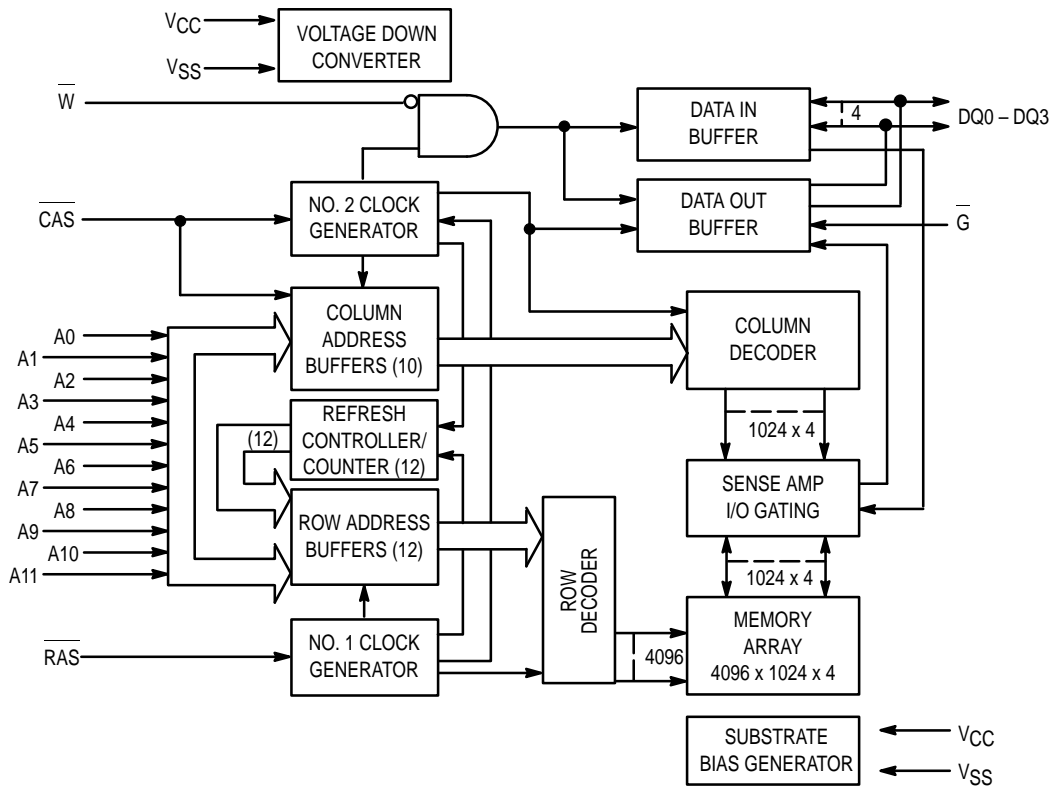


### 2048 CYCLE REFRESH BLOCK DIAGRAM
### MCM517400B
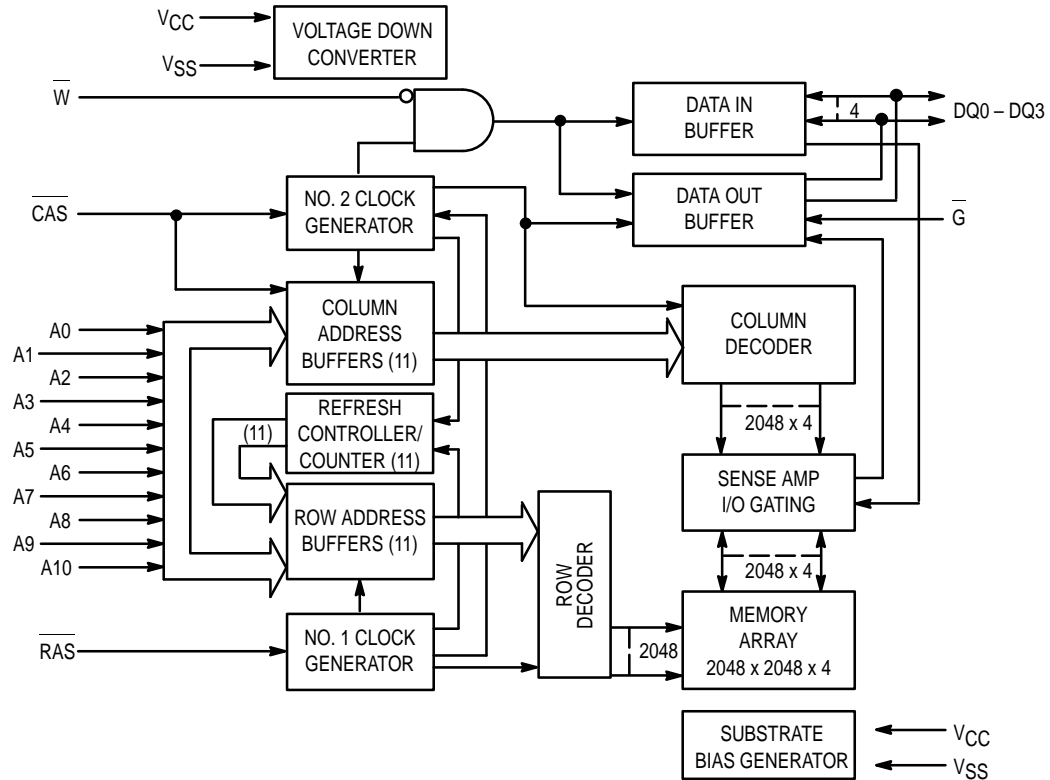
**ABSOLUTE MAXIMUM RATINGS** (See Note)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | − 0.5 to + 7 | V |
| Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$ | $V_{in}$, $V_{out}$ | − 0.5 to + 7 | V |
| Data Output Current | $I_{out}$ | 50 | mA |
| Power Dissipation | $P_D$ | 900 | mW |
| Operating Temperature Range | $T_A$ | 0 to + 70 | °C |
| Storage Temperature Range | $T_{stg}$ | − 55 to + 150 | °C |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

## DC OPERATING CONDITIONS AND CHARACTERISTICS
($V_{CC}$ = 5.0 V ± 10%, $T_A$ = 0 to 70°C, Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS**  (All voltages referenced to $V_{SS}$)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage (Operating Voltage Range) | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
|  | $V_{SS}$ | 0 | 0 | 0 | |
| Logic High Voltage, All Inputs | $V_{IH}$ | 2.4 | — | $V_{CC}$ + 0.5 V | V |
| Logic Low Voltage, All Inputs | $V_{IL}$ | − 0.5* | — | 0.8 | V |

* −2.0 V at pulse width ≤ 20 ns.

**DC CHARACTERISTICS AND SUPPLY CURRENTS** (See note 1)

| Characteristic | | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{CC}$ Power Supply Current (Operating) | MCM516400B–50, $t_{RC}$ = 90 ns | $I_{CC1}$ | — | 100 | mA | 2, 3, 4 |
| | MCM516400B–60, $t_{RC}$ = 110 ns | | — | 80 | | |
| | MCM516400B–70, $t_{RC}$ = 130 ns | | — | 70 | | |
| | MCM517400B–50, $t_{RC}$ = 90 ns | | — | 130 | | |
| | MCM517400B–60, $t_{RC}$ = 110 ns | | — | 110 | | |
| | MCM517400B–70, $t_{RC}$ = 130 ns | | — | 95 | | |
| $V_{CC}$ Power Supply Current (Standby) (RAS = CAS = $V_{IH}$) Output Open | | $I_{CC2}$ | — | 2 | mA | |
| $V_{CC}$ Power Supply Current During RAS–Only Refresh Cycles (CAS = $V_{IH}$) Output Open | | $I_{CC3}$ | | | mA | 2, 4 |
| | MCM516400B–50, $t_{RC}$ = 90 ns | | — | 100 | | |
| | MCM516400B–60, $t_{RC}$ = 110 ns | | — | 80 | | |
| | MCM516400B–70, $t_{RC}$ = 130 ns | | — | 70 | | |
| | MCM517400B–50, $t_{RC}$ = 90 ns | | — | 130 | | |
| | MCM517400B–60, $t_{RC}$ = 110 ns | | — | 110 | | |
| | MCM517400B–70, $t_{RC}$ = 130 ns | | — | 95 | | |
| $V_{CC}$ Power Supply Current During Fast Page Mode Cycle (RAS = $V_{IL}$), (CAS cycling) Output Open | | $I_{CC4}$ | | | mA | 2, 3, 4 |
| | MCM516400B–50, MCM517400B–50, $t_{PC}$ = 35 ns | | — | 80 | | |
| | MCM516400B–60, MCM517400B–60, $t_{PC}$ = 40 ns | | — | 70 | | |
| | MCM516400B–70, MCM517400B–70, $t_{PC}$ = 45 ns | | — | 60 | | |
| $V_{CC}$ Power Supply Current (Standby) (RAS = CAS = $V_{CC}$ – 0.5 V) | | $I_{CC5}$ | — | 1.0 | mA | |
| $V_{CC}$ Power Supply Current During CAS or Before RAS Refresh Cycle, Output Open | | $I_{CC6}$ | | | mA | 2, 4 |
| | MCM516400B–50, $t_{RC}$ = 90 ns | | — | 100 | | |
| | MCM516400B–60, $t_{RC}$ = 110 ns | | — | 80 | | |
| | MCM516400B–70, $t_{RC}$ = 130 ns | | — | 70 | | |
| | MCM517400B–50, $t_{RC}$ = 90 ns | | — | 130 | | |
| | MCM517400B–60, $t_{RC}$ = 110 ns | | — | 110 | | |
| | MCM517400B–70, $t_{RC}$ = 130 ns | | — | 95 | | |
| Input Leakage Current (0 V $\leq$ $V_{in}$ $\leq$ 6.0 V, Other Input Pins = 0 V) | | $I_{lkg(I)}$ | –10 | 10 | µA | |
| Output Leakage Current (0 V $\leq$ $V_{out}$ $\leq$, 5.5 V, Q Floating) | | $I_{lkg(O)}$ | –10 | 10 | µA | |
| Output High Voltage ($I_{OH}$ = – 5 mA) | | $V_{OH}$ | 2.4 | — | V | |
| Output Low Voltage ($I_{OL}$ = 4.2 mA) | | $V_{OL}$ | — | 0.4 | V | |

NOTES:
1. All voltages are referenced to $V_{SS}$.
2. $I_{CC1}$, $I_{CC3}$, $I_{CC4}$, and $I_{CC6}$ depend on cycle rate.
3. $I_{CC1}$, $I_{CC4}$, depend on output loading. Specified values are obtained with the output open.
4. Address can be changed once or less while RAS = $V_{IL}$. In case of $I_{CC4}$, it can be changed once or less during a fast page mode cycle ($t_{PC}$).

**CAPACITANCE** (f = 1.0, $T_A$ = 25°, $V_{CC}$ = 5 V, Periodically Sampled Rather Than 100% Tested)

| Characteristic | | Symbol | Max | Unit |
|---|---|---|---|---|
| Input Capacitance | A0 – A11, D | $C_{in}$ | 5 | pF |
| | G, RAS, CAS, W | | 7 | |
| I/O Capacitance (CAS = $V_{IH}$ to Disable Output) | DQ0 – DQ3, Q | $C_{I/O}$ | 7 | pF |

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I $\Delta t / \Delta V$.

## 16M FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V $\pm$ 10%, $T_A$ = 0 to 70°C, Unless Otherwise Noted)

### ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

| Parameter | Symbol | | MCM51x400B–50 | | MCM51x400B–60 | | MCM51x400B–70 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | Min | Max | | |
| Random Read or Write Cycle Time | $t_{RELREL}$ | $t_{RC}$ | 90 | — | 110 | — | 130 | — | ns | |
| Read–Write Cycle Time<br>MCM516400B<br>MCM517400B | $t_{RELREL}$ | $t_{RWC}$ | <br>130<br>135 | <br>—<br>— | <br>155<br>155 | <br>—<br>— | <br>180<br>180 | <br>—<br>— | ns | |
| Access Time from RAS | $t_{RELQV}$ | $t_{RAC}$ | — | 50 | — | 60 | — | 70 | ns | 8, 13, 14 |
| Access Time from CAS | $t_{CELQV}$ | $t_{CAC}$ | — | 13 | — | 15 | — | 20 | ns | 8, 13 |
| Access Time from Column Address | $t_{AVQV}$ | $t_{AA}$ | — | 25 | — | 30 | — | 35 | ns | 8, 14 |
| Access Time from Precharge CAS | $t_{CEHQV}$ | $t_{CPA}$ | — | 30 | — | 35 | — | 40 | ns | 8 |
| CAS to Output in Low–Z | $t_{CELQX}$ | $t_{CLZ}$ | 0 | — | 0 | — | 0 | — | ns | 8 |
| Output Buffer and Turn–Off Delay | $t_{CEHQZ}$ | $t_{OFF}$ | 0 | 13 | 0 | 15 | 0 | 15 | ns | 9 |
| Transition Time (Rise and Fall) | $t_T$ | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | 7 |
| RAS Precharge Time | $t_{REHREL}$ | $t_{RP}$ | 30 | — | 40 | — | 50 | — | ns | |
| RAS Pulse Width | $t_{RELREH}$ | $t_{RAS}$ | 50 | 10 k | 60 | 10 k | 70 | 10 k | ns | |
| RAS Hold Time | $t_{CELREH}$ | $t_{RSH}$ | 13 | — | 15 | — | 20 | — | ns | |
| CAS Hold Time | $t_{RELCEH}$ | $t_{CSH}$ | 50 | — | 60 | — | 70 | — | ns | |
| CAS Precharge to RAS Hold Time | $t_{CEHREH}$ | $t_{RHCP}$ | 30 | — | 35 | — | 40 | — | ns | |
| CAS Pulse Width | $t_{CELCEH}$ | $t_{CAS}$ | 13 | 10 k | 15 | 10 k | 20 | 10 k | ns | |
| RAS to CAS Delay Time | $t_{RELCEL}$ | $t_{RCD}$ | 17 | 37 | 20 | 45 | 20 | 50 | ns | 13 |
| RAS to Column Address Delay Time | $t_{RELAV}$ | $t_{RAD}$ | 12 | 25 | 15 | 30 | 15 | 35 | ns | 14 |
| CAS to RAS Precharge Time | $t_{CEHREL}$ | $t_{CRP}$ | 5 | — | 5 | — | 5 | — | ns | |
| CAS Precharge Time | $t_{CEHCEL}$ | $t_{CP}$ | 10 | — | 10 | — | 10 | — | ns | |
| Row Address Setup Time | $t_{AVREL}$ | $t_{ASR}$ | 0 | — | 0 | — | 0 | — | ns | |
| Row Address Hold Time | $t_{RELAX}$ | $t_{RAH}$ | 7 | — | 10 | — | 10 | — | ns | |
| Column Address Setup Time | $t_{AVCEL}$ | $t_{ASC}$ | 0 | — | 0 | — | 0 | — | ns | |
| Column Address Hold Time | $t_{CELAX}$ | $t_{CAH}$ | 10 | — | 10 | — | 15 | — | ns | |
| Column Address to RAS Lead Time | $t_{AVREH}$ | $t_{RAL}$ | 25 | — | 30 | — | 35 | — | ns | |
| Read Command Setup Time | $t_{WHCEL}$ | $t_{RCS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Read Command Hold Time Referenced to CAS | $t_{CEHWX}$ | $t_{RCH}$ | 0 | — | 0 | — | 0 | — | ns | 10 |
| Read Command Hold Time Referenced to RAS | $t_{REHWX}$ | $t_{RRH}$ | 0 | — | 0 | — | 0 | — | ns | 10 |

NOTES:                                                                                    (continued)
1. All voltages are referenced to $V_{SS}$.
2. $I_{CC1}$, $I_{CC3}$, $I_{CC4}$, $I_{CC6}$ depend on cycle rate.
3. $I_{CC1}$, $I_{CC4}$ depend on output loading. Specified values are obtained with the output open.
4. Address can be changed once or less while RAS = $V_{IL}$. In case of $I_{CC4}$, it can be changed once or less during a fast page mode cycle ($t_{PC}$).
5. An initial pause of 200 μs is required after power–up followed by 8 RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS before RAS refresh cycles instead of 8 RAS only refresh cycles are required.
6. AC measurements $t_T$ = 5.0 ns.
7. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$.

**ALL DEVICES, READ, WRITE, AND READ–WRITE CYCLES** (Continued)

| Parameter | Symbol Std | Alt | MCM51x400B–50 Min | MCM51x400B–50 Max | MCM51x400B–60 Min | MCM51x400B–60 Max | MCM51x400B–70 Min | MCM51x400B–70 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| Write Command Hold Time Referenced to CAS | $t_{CELWH}$ | $t_{WCH}$ | 10 | — | 10 | — | 15 | — | ns | |
| Write Command Pulse Width | $t_{WLWH}$ | $t_{WP}$ | 10 | — | 10 | — | 15 | — | ns | |
| Write Command to RAS Lead Time | $t_{WLREH}$ | $t_{RWL}$ | 15 | — | 15 | — | 20 | — | ns | |
| Write Command to CAS Lead Time | $t_{WLCEH}$ | $t_{CWL}$ | 15 | — | 15 | — | 20 | — | ns | |
| Data In Setup Time | $t_{DVCEL}$ | $t_{DS}$ | 0 | — | 0 | — | 0 | — | ns | 11 |
| Data In Hold Time | $t_{CELDX}$ | $t_{DH}$ | 10 | — | 10 | — | 15 | — | ns | 11 |
| Write Command Setup Time | $t_{WLCEL}$ | $t_{WCS}$ | 0 | — | 0 | — | 0 | — | ns | 12 |
| CAS to Write Delay | $t_{CELWL}$ | $t_{CWD}$ | 35 | — | 40 | — | 45 | — | ns | 12 |
| RAS to Write Delay | $t_{RELWL}$ | $t_{RWD}$ | 73 | — | 85 | — | 95 | — | ns | 12 |
| Column Address to Write Delay | $t_{AVWL}$ | $t_{AWD}$ | 48 | — | 55 | — | 60 | — | ns | 12 |
| Refresh Period MCM516400B / MCM517400B | $t_{RVRV}$ | $t_{RFSH}$ | — / — | 64 / 32 | — / — | 64 / 32 | — / — | 64 / 32 | ms | |
| CAS Setup Time for CAS Before RAS Refresh | $t_{RELCEL}$ | $t_{CSR}$ | 5 | — | 5 | — | 5 | — | ns | |
| CAS Hold Time for CAS Before RAS Refresh | $t_{RELCEH}$ | $t_{CHR}$ | 10 | — | 10 | — | 10 | — | ns | |
| RAS Precharge to CAS Active Time | $t_{REHCEL}$ | $t_{RPC}$ | 5 | — | 5 | — | 5 | — | ns | |
| CAS Precharge Time for CAS Before RAS Counter Time | $t_{CEHCEL}$ | $t_{CPT}$ | 20 | — | 20 | — | 20 | — | ns | |
| Write Command Setup Time (Test Mode) | $t_{WLREL}$ | $t_{WTS}$ | 10 | — | 10 | — | 10 | — | ns | |
| Write Command Hold Time (Test Mode) | $t_{RELWH}$ | $t_{WTH}$ | 10 | — | 10 | — | 10 | — | ns | |
| Write to RAS Precharge Time (CAS Before RAS Refresh) | $t_{WHREL}$ | $t_{WRP}$ | 10 | — | 10 | — | 10 | — | ns | |
| Write to RAS Hold Time (CAS Before RAS Refresh) | $t_{RELWL}$ | $t_{WRH}$ | 10 | — | 10 | — | 10 | — | ns | |

NOTES:
8. Measured with a load equivalent to 2 TTL loads and 100 pF.
9. $t_{OFF}$ (max) and $t_{GZ}$ (max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
10. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.
11. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in Read–Modify–Write cycles.
12. $t_{WCS}$, $t_{CWD}$, $t_{RWD}$, $t_{AWD}$ and $t_{CPWD}$ are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the DQ pins remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (for fast page mode cycle only), the cycle is a read–modify–write cycle and the DQ pins will contain the data read from the selected address. If neither of these conditions are met; delayed write or at access time and until CAS or OE goes back to $V_{IH}$, DQ is indeterminate.
13. Operation within the $t_{RCD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
14. Operation within the $t_{RAD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RAD}$ (max) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$ (max), then access time is controlled exclusively by $t_{AA}$.

($V_{CC}$ = 5.0 V $\pm$ 10%, $T_A$ = 0 to 70°C, Unless Otherwise Noted)

**4M x 4 CONFIGURATION–SPECIFIC READ, WRITE, AND READ–WRITE CYCLES** (See Notes 1, 2, 3, and 4)

| Parameter | Symbol | | MCM51x400B–50 | | MCM51x400B–60 | | MCM51x400B–70 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | Min | Max | | |
| RAS Hold Time Referenced to G | $t_{GLREH}$ | $t_{ROH}$ | 10 | — | 10 | — | 10 | — | ns | |
| G Access Time | $t_{GLQV}$ | $t_{GA}$ | — | 13 | — | 15 | — | 15 | ns | 5 |
| G to Data Delay | $t_{GLHDX}$ | $t_{GD}$ | 13 | — | 15 | — | 15 | — | ns | 6 |
| Output Buffer Turn–Off Delay Time from G | $t_{GHQZ}$ | $t_{GZ}$ | 0 | 13 | 0 | 15 | 0 | 15 | ns | |
| G Command Hold Time | $t_{WLGL}$ | $t_{GH}$ | 15 | — | 15 | — | 15 | — | ns | |
| Output Disable Setup Time | $t_{GHCEL}$ | $t_{GDS}$ | 0 | — | 0 | — | 0 | — | ns | |

NOTES:
1. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$.
2. An initial pause of 200 $\mu$s is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
4. AC measurements $t_T$ = 5.0 ns.
5. Measured with a current load equivalent to 2 TTL ($-$ 200 $\mu$A, + 4 mA) loads and 100 pF with the data output trip points set at $V_{OH}$ = 2.0 V and $V_{OL}$ = 0.8 V.
6. $t_{OFF}$ (max) and/or $t_{GZ}$ (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

**FAST PAGE MODE READ, WRITE, AND READ–WRITE CYCLES** (See Notes 1, 2, 3, and 4)

| Parameter | Symbol | | MCM51x400B–50 | | MCM51x400B–60 | | MCM51x400B–70 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | Min | Max | | |
| Fast Page Mode Cycle Time | $t_{CELCEL}$ | $t_{PC}$ | 35 | — | 40 | — | 45 | — | ns | |
| CAS Precharge to RAS Hold Time (Fast Page Mode) | $t_{CEHREH}$ | $t_{RHCP}$ | 30 | — | 35 | — | 40 | — | ns | |
| Fast Page Mode Read–Write Cycle Time    MCM516400B<br>                  MCM517400B | $t_{CELCEL}$ | $t_{PRWC}$ | 65<br>80 | —<br>— | 85<br>85 | —<br>— | 95<br>95 | —<br>— | ns | |
| RAS Pulse Width (Fast Page Mode) | $t_{RELREH}$ | $t_{RASP}$ | 50 | 200 k | 60 | 200 k | 70 | 200 k | ns | |
| CAS Precharge to Write Delay | $t_{CEHWL}$ | $t_{CPWD}$ | 53 | — | 60 | — | 65 | — | ns | 5 |

NOTES:
1. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$.
2. An initial pause of 200 $\mu$s is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
4. AC measurements $t_T$ = 5.0 ns.
5. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$, and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through–out the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
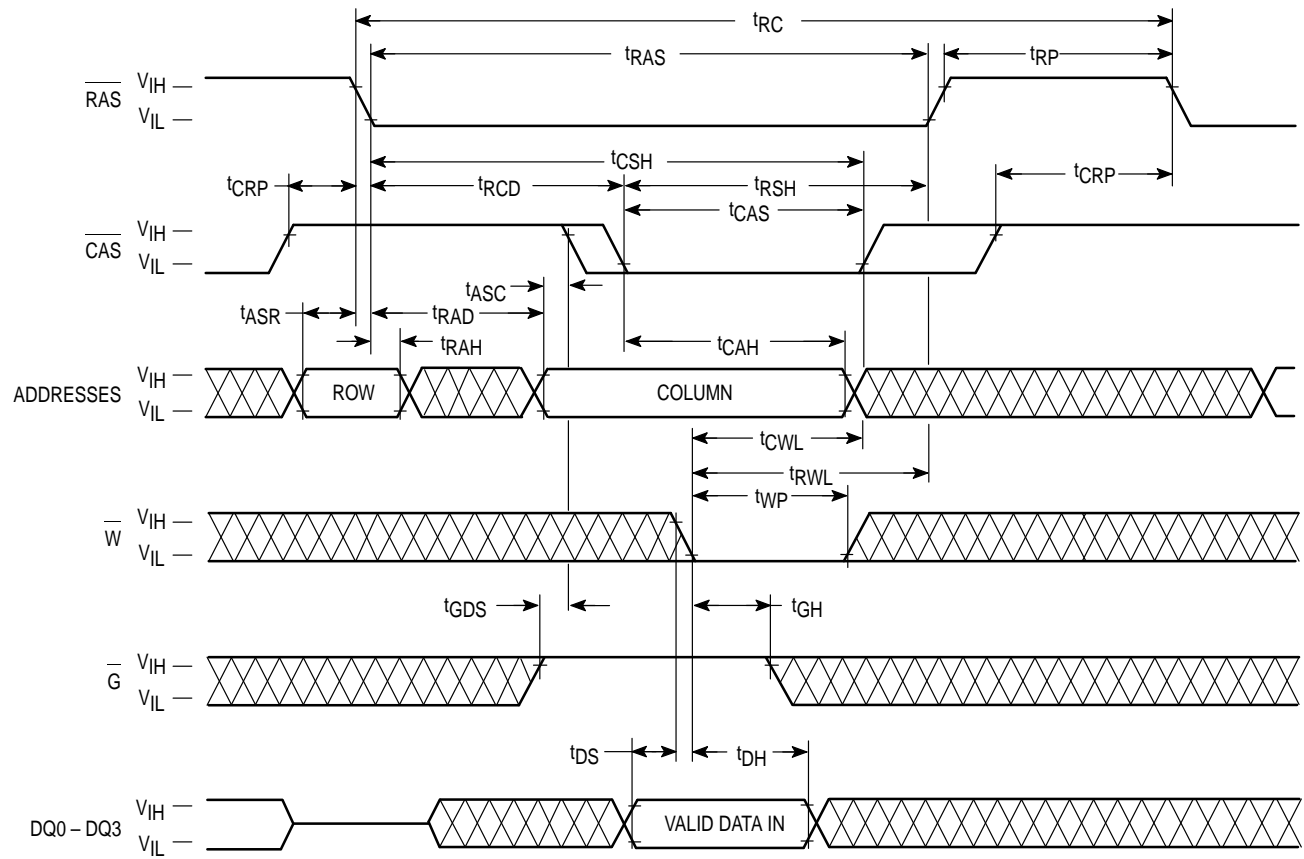
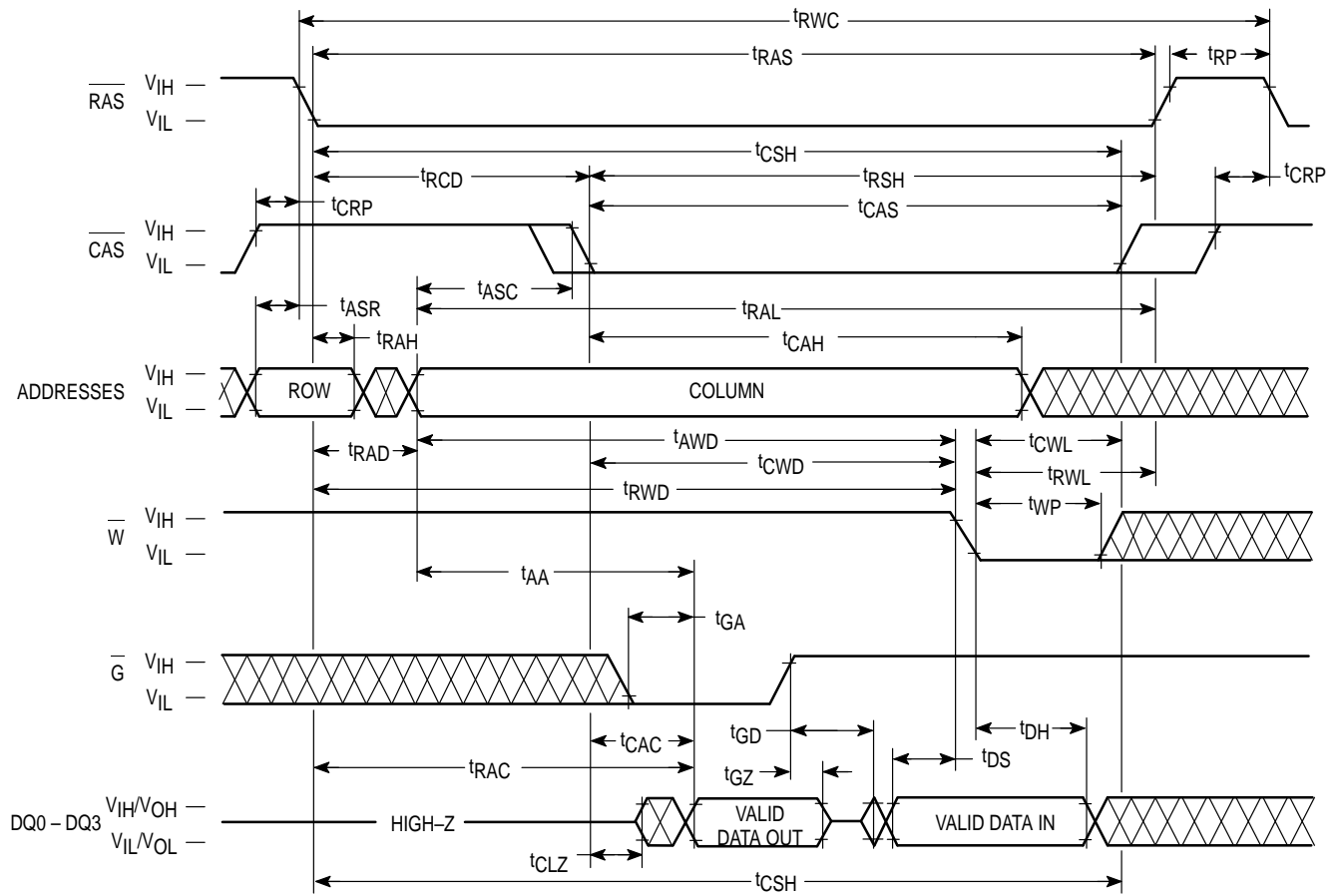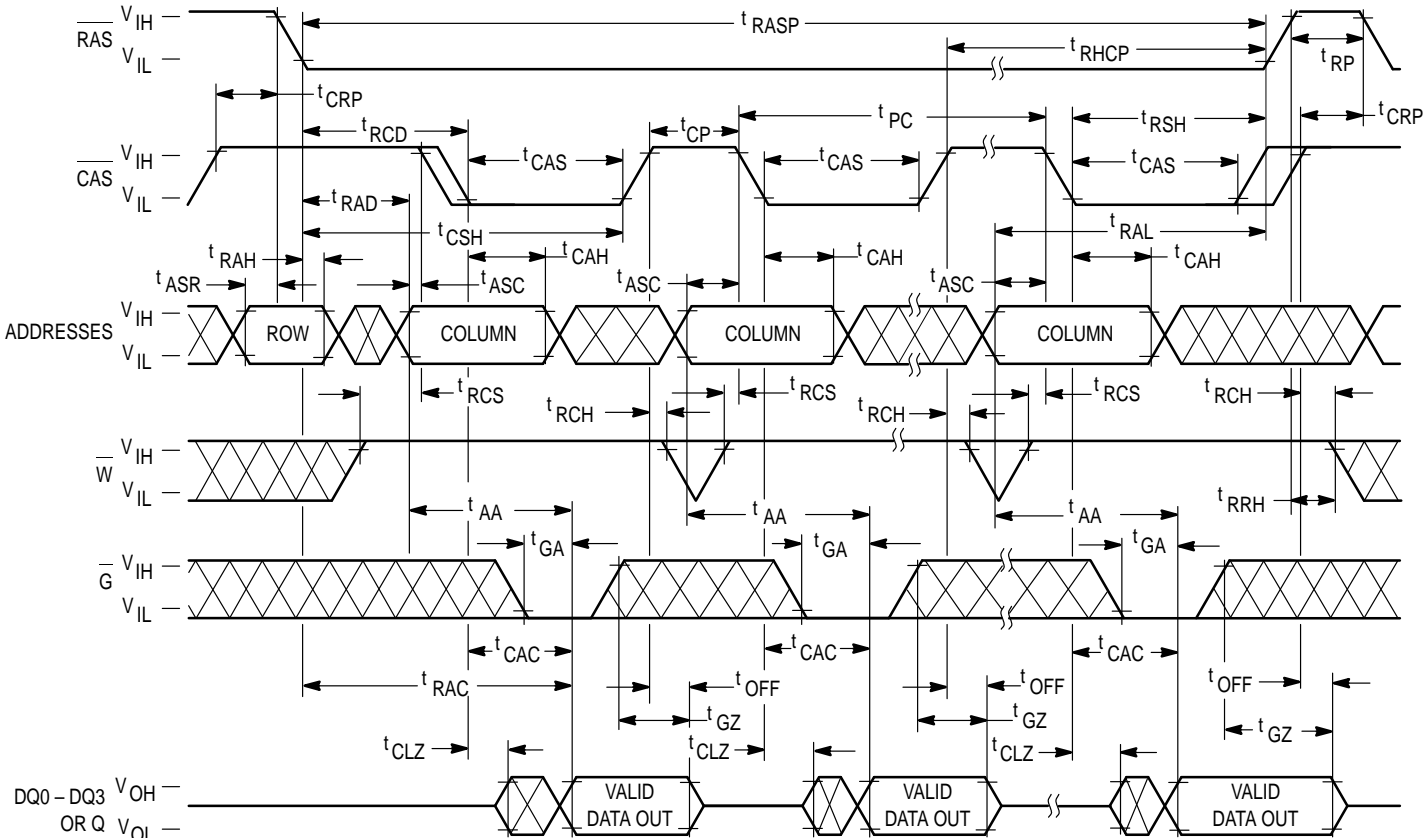## TIMING DIAGRAMS

### PAGE MODE READ CYCLE
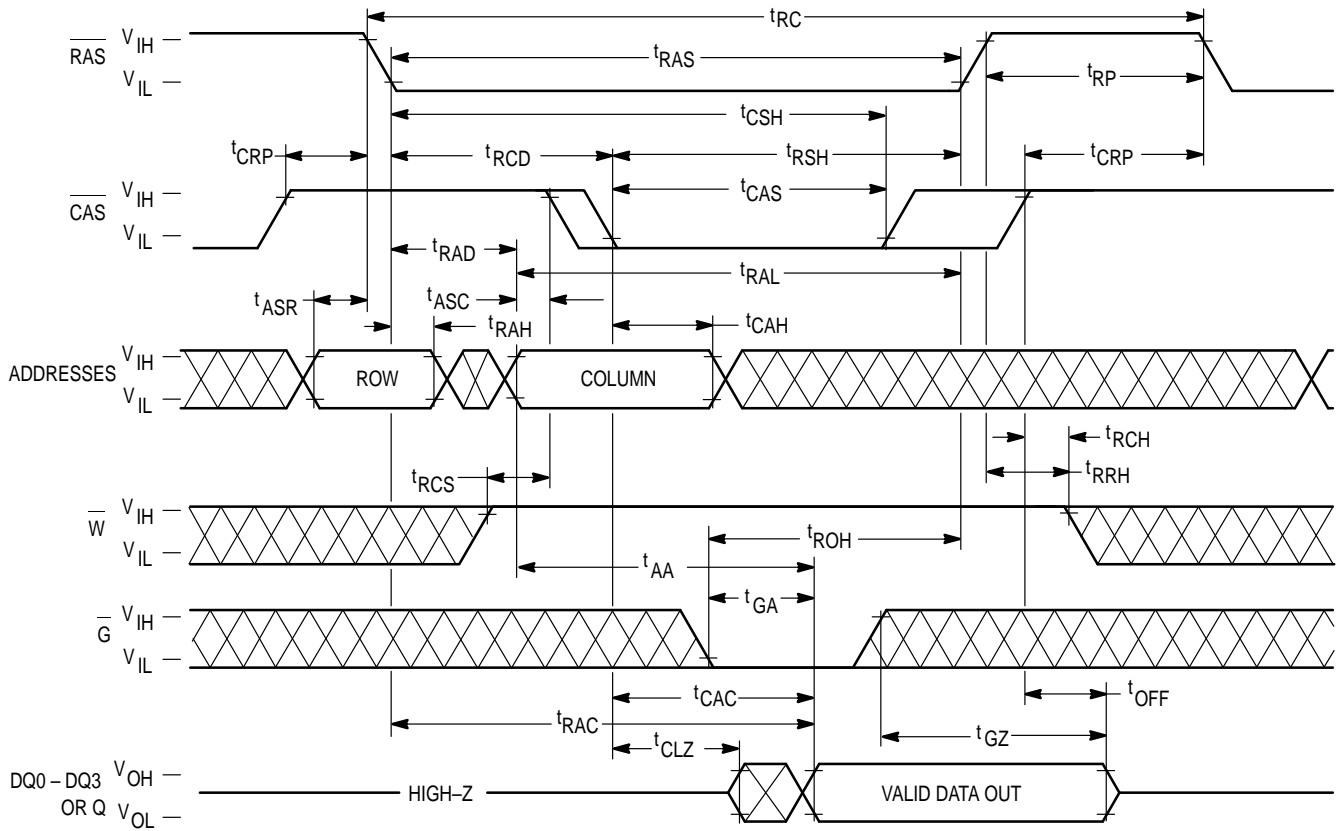
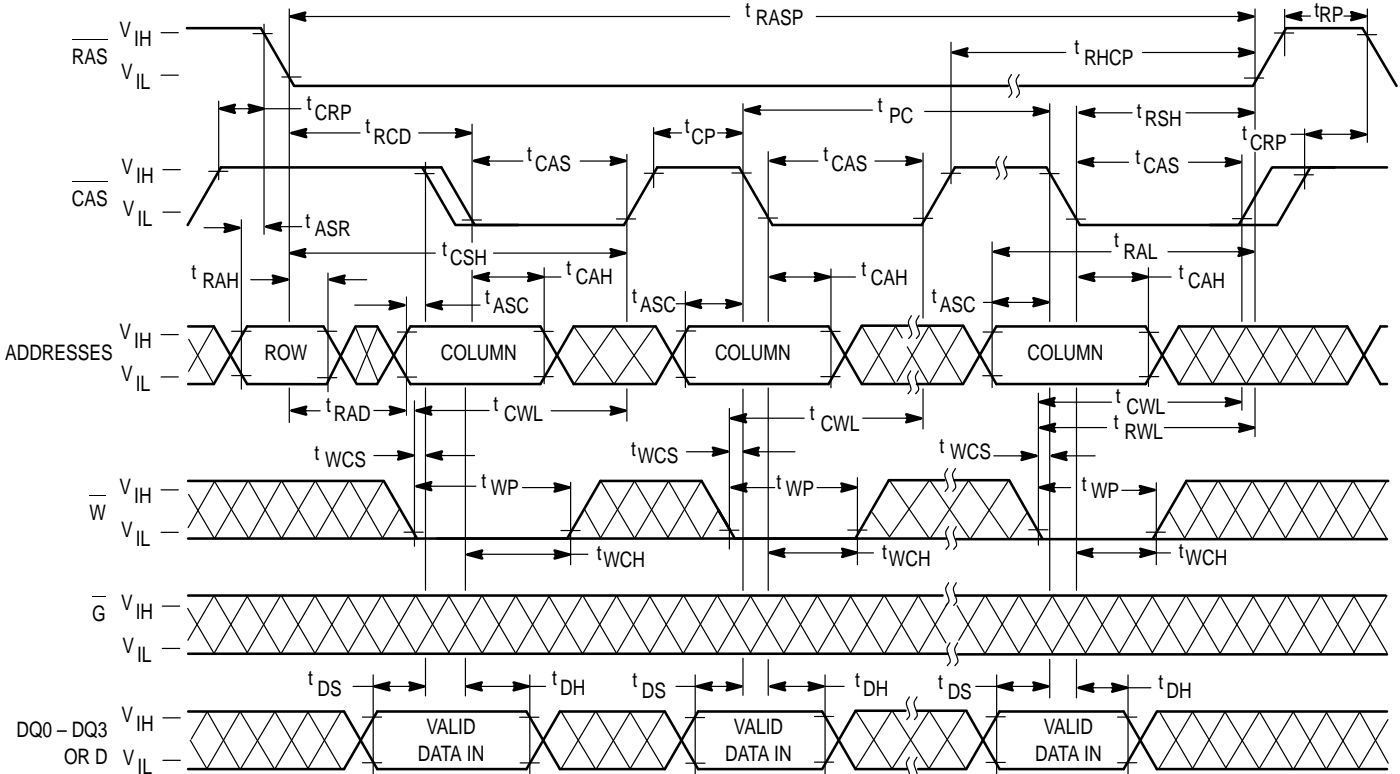**EARLY WRITE CYCLE**
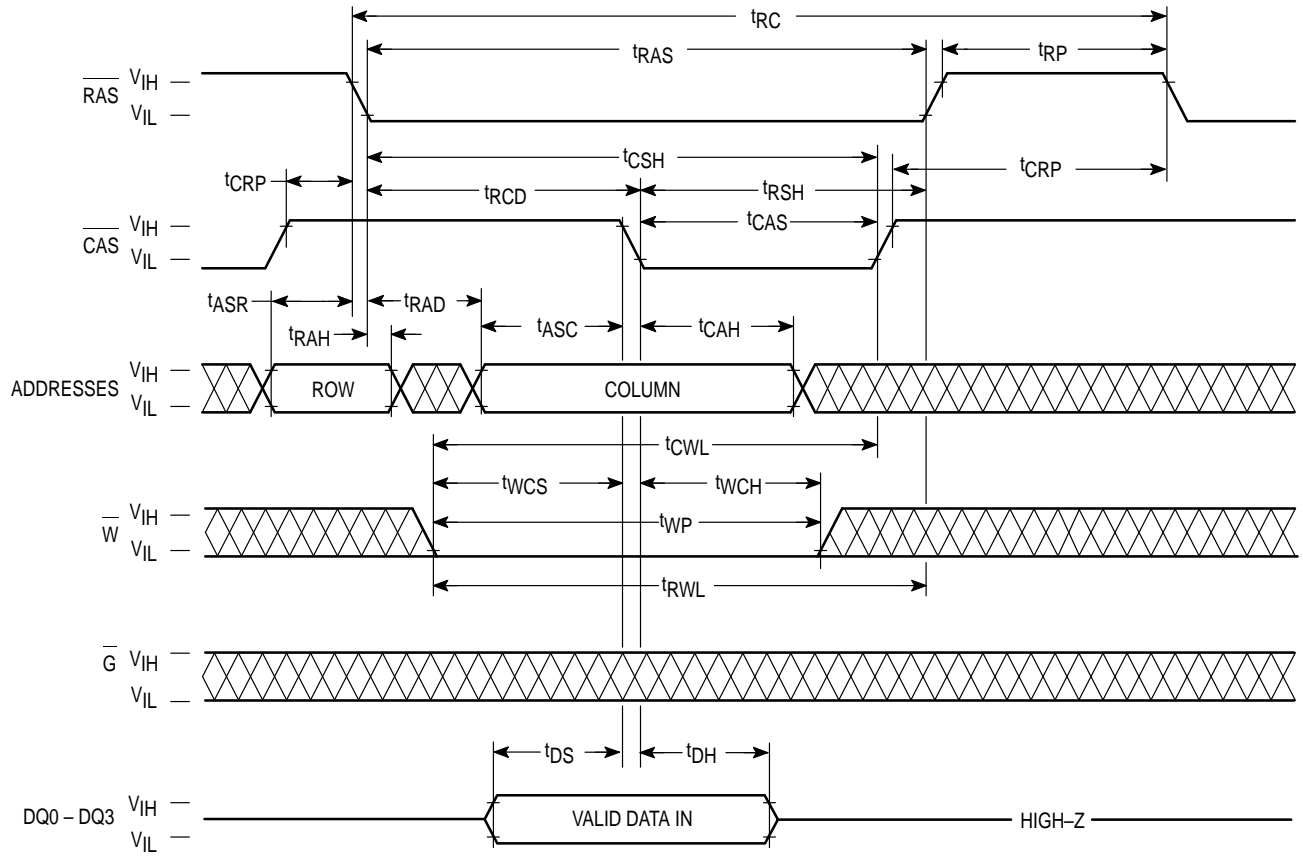
# $\overline{G}$ CONTROLLED LATE WRITE CYCLE
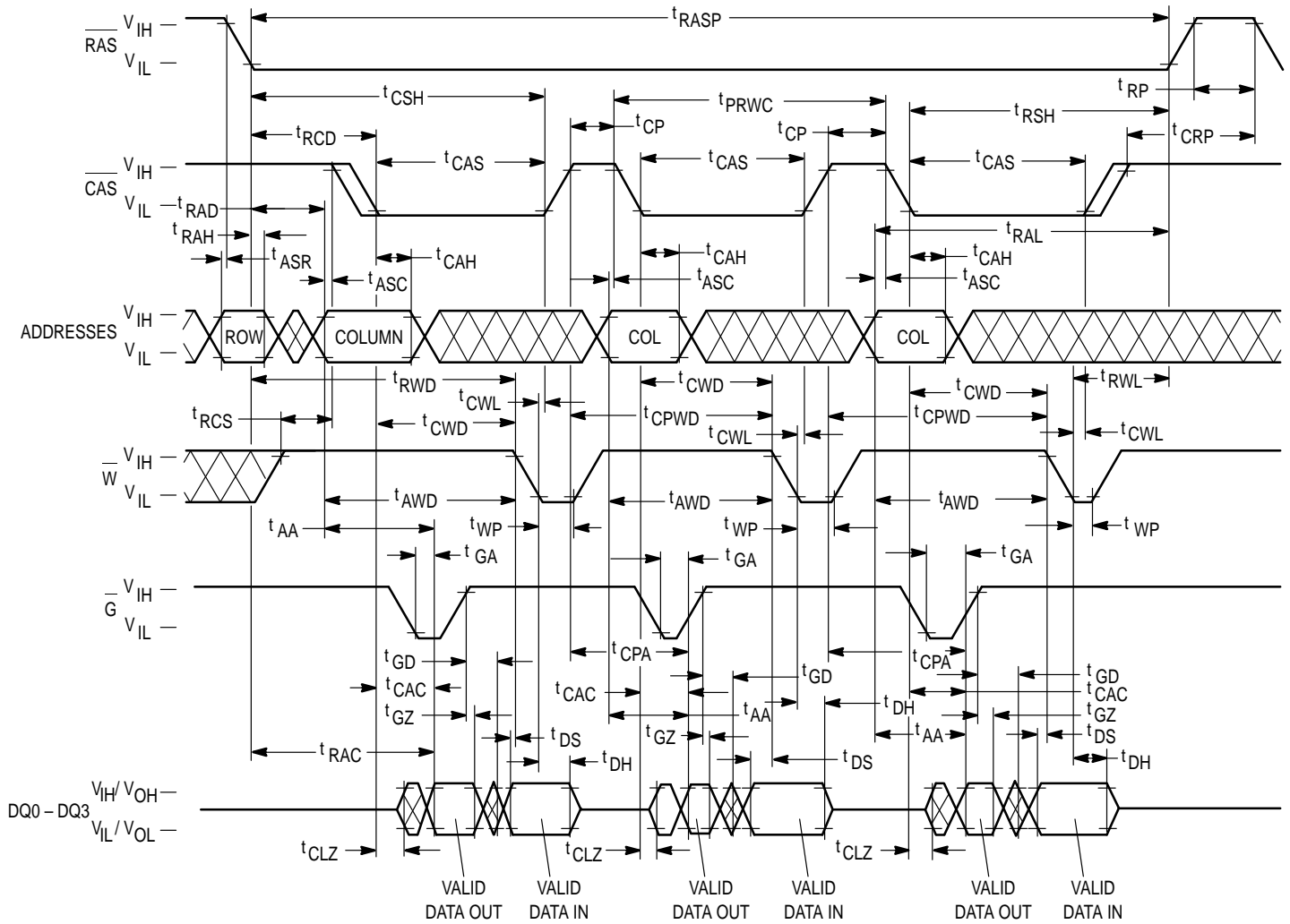
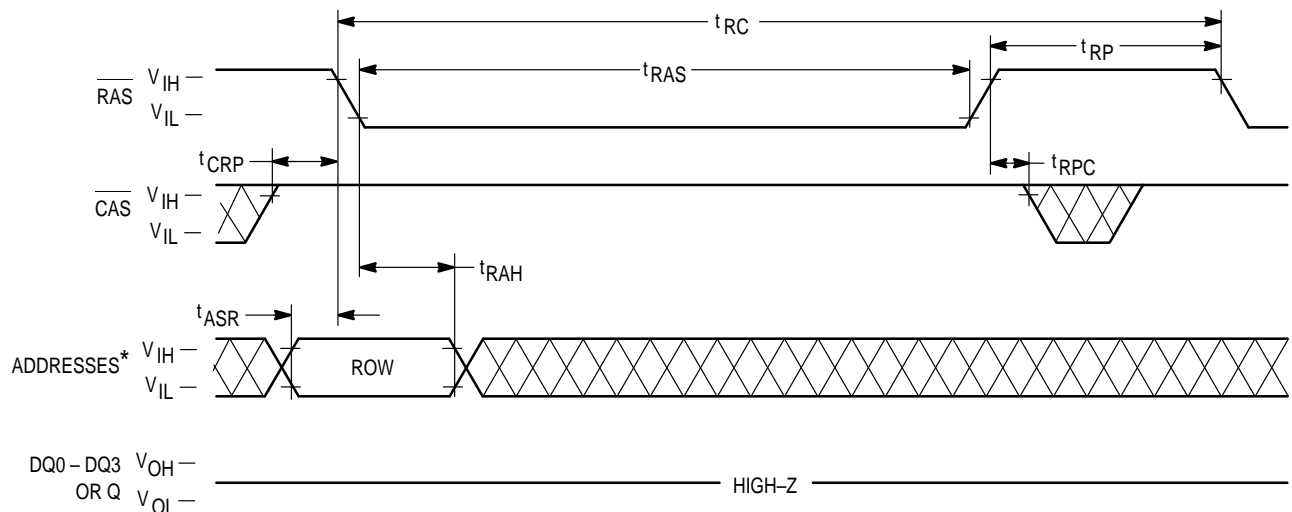**READ – WRITE CYCLE**

## FAST PAGE MODE READ CYCLE



## FAST PAGE MODE EARLY WRITE CYCLE



---

# FAST PAGE MODE READ – WRITE CYCLE



## RAS ONLY REFRESH CYCLE
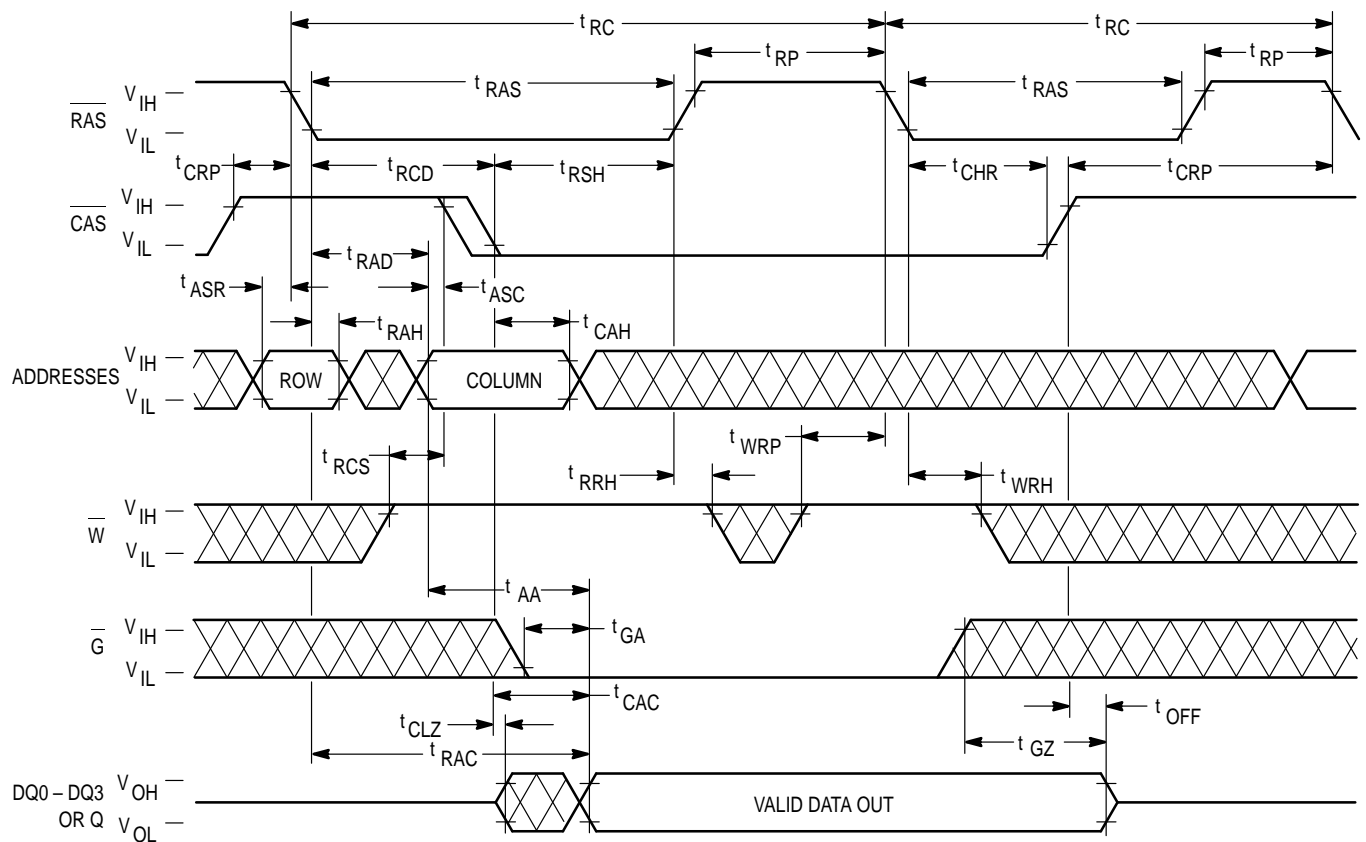### (W and G are Don't Care)
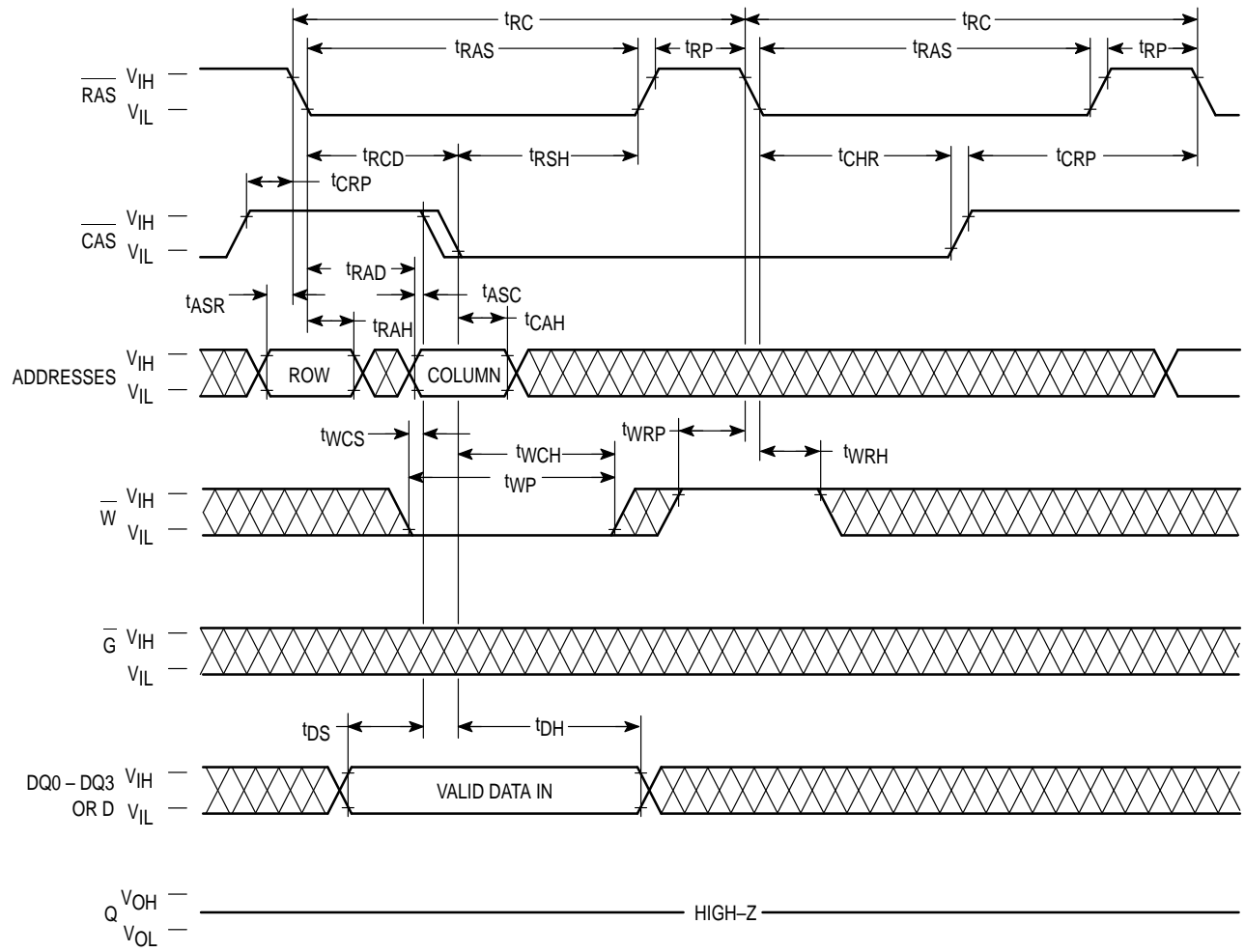


*MCM516400B – A0 – A11; MCM517400B – A0 – A10.

---

## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
### ($\overline{\text{G}}$ and A0 – A10 or A11 are Don't Care)

$t_{RC}$

$t_{RAS}$   $t_{RP}$

$\overline{\text{RAS}}$  $V_{IH}$ — $V_{IL}$ —

$t_{CSR}$

$t_{RPC}$

$t_{CP}$

$\overline{\text{CAS}}$  $V_{IH}$ — $V_{IL}$ —

$t_{CHR}$

$t_{WRP}$   $t_{WRH}$

$\overline{\text{W}}$  $V_{IH}$ — $V_{IL}$ —

$t_{OFF}$

DQ0 – DQ3  $V_{OH}$ — OR Q  $V_{OL}$ —

HIGH–Z

## HIDDEN REFRESH CYCLE (READ)

$t_{RC}$   $t_{RC}$

$t_{RP}$   $t_{RP}$

$\overline{\text{RAS}}$  $V_{IH}$ — $V_{IL}$ —

$t_{RAS}$   $t_{RAS}$

$t_{CRP}$   $t_{RCD}$   $t_{RSH}$   $t_{CHR}$   $t_{CRP}$

$\overline{\text{CAS}}$  $V_{IH}$ — $V_{IL}$ —

$t_{RAD}$

$t_{ASR}$   $t_{ASC}$

$t_{RAH}$   $t_{CAH}$

ADDRESSES  $V_{IH}$ — $V_{IL}$ —

ROW   COLUMN

$t_{RCS}$

$t_{RRH}$   $t_{WRP}$   $t_{WRH}$

$\overline{\text{W}}$  $V_{IH}$ — $V_{IL}$ —

$t_{AA}$

$\overline{\text{G}}$  $V_{IH}$ — $V_{IL}$ —

$t_{GA}$

$t_{CAC}$

$t_{CLZ}$   $t_{OFF}$

$t_{RAC}$   $t_{GZ}$

DQ0 – DQ3  $V_{OH}$ — OR Q  $V_{OL}$ —

VALID DATA OUT
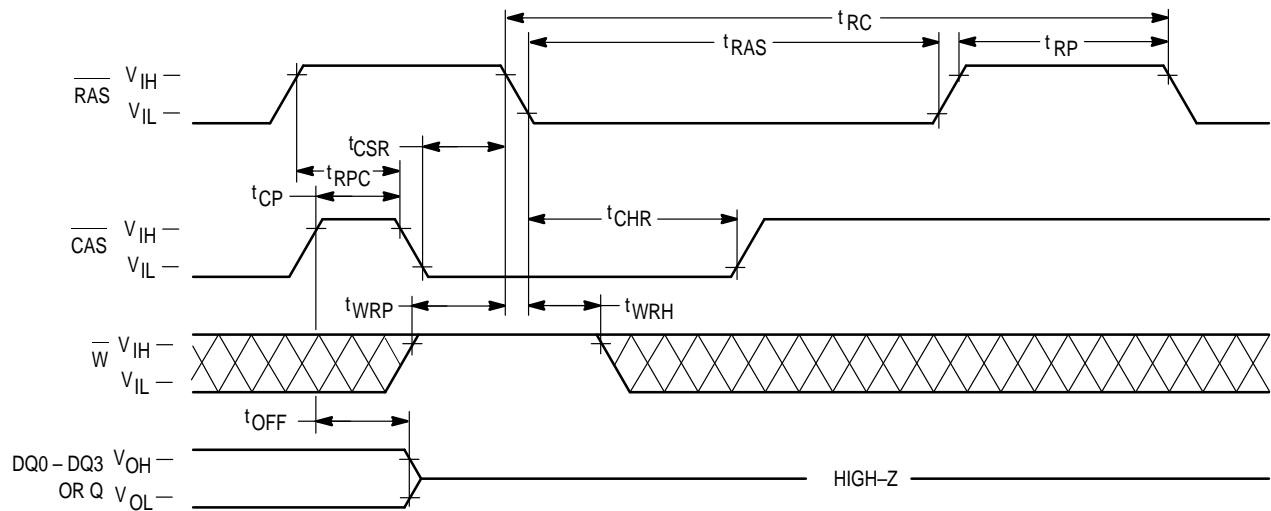
# HIDDEN REFRESH CYCLE (EARLY WRITE)

# $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE
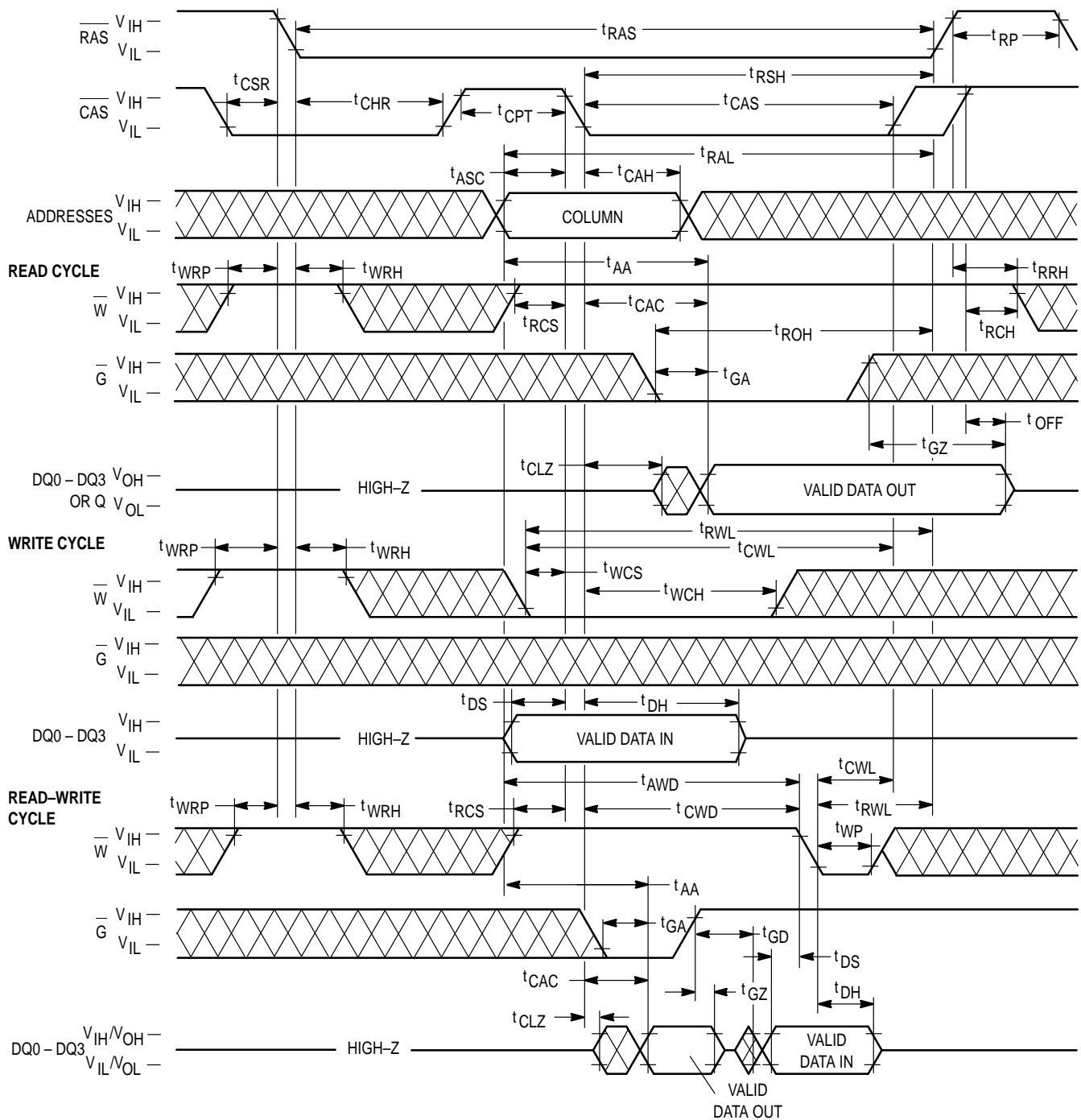
## DEVICE INITIALIZATION

On power–up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 32 milliseconds or 64 milliseconds, for MCM517400B and MCM516400B, respectively), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

## ADDRESSING THE RAM

**MCM516400B**: The twelve address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS) and column address strobe (CAS), into two separate address fields. A total of twenty two address bits, twelve rows and ten columns, will decode one of the 4,194,304 four bit word locations in the device. RAS active transition is followed by CAS active transition (active = $V_{IL}$, $t_{RCD}$ minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This "gate" feature on the external CAS clock enables the internal CAS line as soon as the row address hold time ($t_{RAH}$) specification is met (and defines $t_{RCD}$ minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

**MCM517400B**: The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS ) and column address strobe (CAS), into two separate 11–bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 four bit word locations in the device. RAS active transition is followed by CAS active transition (active = $V_{IL}$, $t_{RCD}$ minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This "gate" feature on the external CAS clock enables the internal CAS line as soon as the row address hold time ($t_{RAH}$) specification is met (and defines $t_{RCD}$ minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

There are three other variations in addressing the 16M DRAM Family per device: RAS–only refresh cycle, CAS before RAS refresh cycle, and page mode. All are discussed in separate sections that follow.

## READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, fast page mode read cycle, read–write cycle, and fast page mode read–write cycle. The normal read cycle is outlined here,while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (W) input level must be high

($V_{IH}$), $t_{RCS}$ (minimum) before the CAS or active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

For **MCM516400B and MCM517400B**, both CAS and output enable (G) control read access time: CAS must be active before or at $t_{RCD}$ maximum and G must be active $t_{RAC}$–$t_{GA}$ (both minimum) after RAS active transition to guarantee valid data out (Q) at $t_{RAC}$. If the $t_{RCD}$ maximum is exceeded and/or G active transition does not occur in time, read access time is determined by either the CAS or G clock active transition ($t_{CAC}$ or $t_{GA}$).

## WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, fast page mode early write, and fast page mode read–write. Early and late write modes are discussed here, while fast page mode write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of W to active ($V_{IL}$). Early and late write modes are distinguished by the active transition of W, with respect to CAS. Minimum active time $t_{RAS}$ and $t_{CAS}$, and precharge time $t_{RP}$, apply to write mode, as in the read mode.

An early write cycle is characterized by W active transition at minimum time $t_{WCS}$ before CAS active transition. Column address setup and hold times ($t_{ASC}$, $t_{CAH}$) and data in (D) setup and hold times ($t_{DS}$, $t_{DH}$) are referenced to CAS in an early write cycle. RAS and CAS clocks must stay active for $t_{RWL}$ and $t_{CWL}$, respectively, after the start of the early write operation to complete the cycle.

A late–write cycle (referred to as G–controlled write) occurs when W active transition is made after CAS active transition. W active transition could be delayed for almost 10 microseconds after CAS active transition, ($t_{RCD}$ + $t_{CWD}$ + $t_{RWL}$ + $2t_T$) ≤ $t_{RAS}$, if other timing minimums ($t_{RCD}$, $t_{RWL}$, and $t_T$) are maintained. D timing parameters are referenced to W active transition in a late write cycle. Output buffers are enabled by CAS active transition. 4M x 4 outputs are switched off by G inactive transition, which is required to write to the device. Q may be indeterminate (see note 12 of AC Operating Conditions table). RAS and CAS must remain active for $t_{RWL}$ and $t_{CWL}$, respectively, after W active transition to complete the write cycle. G (4M x 4) devices must remain inactive for $t_{GH}$ after W active transition to complete the write cycle.

## READ–WRITE CYCLE

A read–write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except W must remain high for $t_{CWD}$ and/or $t_{AWD}$ minimum, to guarantee valid Q before writing the bit.

## PAGE MODE CYCLES

Page mode allows fast successive data operations at all column locations (MCM516400B: 1024 columns; and MCM517400B: 2048 columns) on a selected row of the 16M DRAM family. Read access time in page mode ($t_{CAC}$) is typically half the regular RAS clock access time, $t_{RAC}$. Page mode operation consists of keeping RAS active while toggling CAS

between $V_{IH}$ and $V_{IL}$. The row is latched by $\overline{RAS}$ active transition, while each CAS active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read–write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum $t_{CP}$, while RAS remains low ($V_{IL}$). The second CAS active transition while RAS is low initiates the first page mode cycle ($t_{PC}$ or $t_{PRWC}$). Either a read, write, or read–write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by $t_{RASP}$. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

### REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM516400B require refresh every 64 milliseconds, while refresh time for the MCM517400B is 32 milliseconds.

This is accomplished by cycling through the 4096 and 2048 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the 16M DRAM device family. Burst refresh, a refresh of all rows consecutively, must be performed every 64 milliseconds on the MCM516400B, and 32 milliseconds on the MCM517400B.

A normal read, write, or read–write operation to the RAM will refresh all the bits (4096 or 2048) associated with the particular row decodes. Three other methods of refresh, **RAS–only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

### RAS–Only Refresh

RAS–only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while CAS remains high ($V_{IH}$) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

### CAS Before RAS Refresh

$\overline{CAS}$ before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time $t_{WRP}$ before and time $t_{WRH}$ after RAS active transition to prevent switching the device into a **test mode cycle**.

### Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle while RAS cycles inactive for $t_{RP}$ and back to active starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode entry) as in CAS before RAS refresh.

### CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read–write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 4096 or 2048 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **CAS before RAS** initialization cycles. Test procedure:

1. Write 0s into all memory cells with normal write mode.
2. Select a column address, read 0 out and write 1 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation 4096 or 2048 times, depending on device type.
3. Read the 1s that were written in step two in normal read mode.
4. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation 4096 or 2048 times, depending on device type.
5. Read 0s which were written in step four in normal read mode.
6. Repeat steps one through five using complement data.

**TEST MODE**

The internal organization of the MCM516400B and MCM517400B allows the device to be tested as if it were a 1M x 16 DRAM. In **Test Mode** operation, column addresses A1 and A0 are ignored. A test mode cycle reads and/or writes data to a bit in each of the sixteen 1M blocks in parallel. During a write cycle, data is written using only DQ0, while during a read cycle, if all 16 bits are equal (all 0s or all 1s), DQ3 will indicate a 1. Otherwise, DQ3 will indicate a 0. DQ0, DQ1, and DQ2 always indicate a 1 during test mode read cycle. See Test Mode block diagram.

W, CAS before RAS timing puts the device in **Test Mode**, as shown in the test mode timing diagram. A **CAS before RAS** refresh cycle or a **RAS on**ly refresh cycle places the device back in normal mode. Refresh is performed in test mode by using a **W, CAS before RAS** refresh cycle which uses the internal refresh address counter.
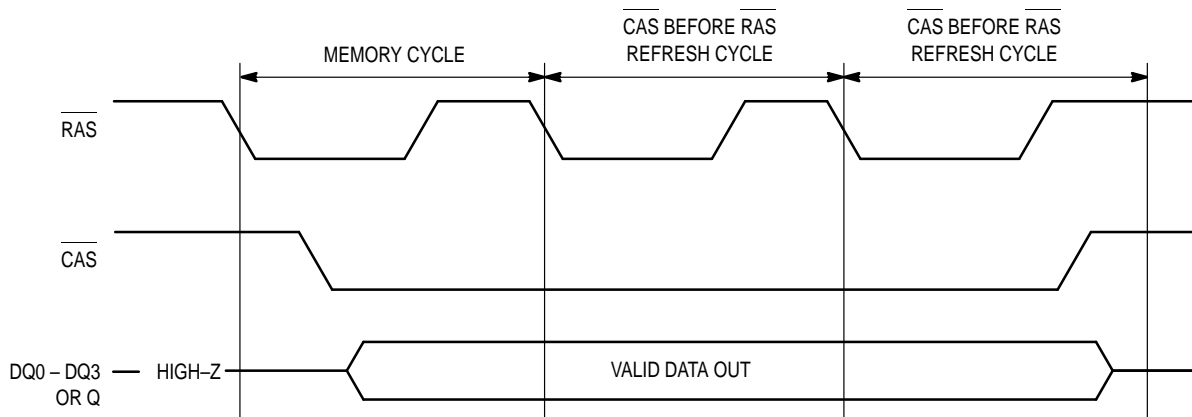


**Figure 1. Hidden Refresh Cycle**

## TEST MODE AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V $\pm$ 10%, $T_A$ = 0 to 70°C, Unless Otherwise Noted)

**READ, WRITE, AND READ–WRITE CYCLES**

| Parameter | Symbol | | MCM51x400B–50 | | MCM51x400B–60 | | MCM51x400B–70 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | Min | Max | | |
| Random Read or Write Cycle Time | $t_{RELREL}$ | $t_{RC}$ | 95 | — | 115 | — | 135 | — | ns | |
| Fast Page Mode Cycle Time   MCM516400B   MCM517400B | $t_{CELCEL}$ | $t_{PC}$ | 35<br>40 | —<br>— | 45<br>45 | —<br>— | 50<br>50 | —<br> | ns | |
| Access Time from RAS | $t_{RELQV}$ | $t_{RAC}$ | — | 55 | — | 65 | — | 75 | ns | |
| Access Time from CAS | $t_{CELQV}$ | $t_{CAC}$ | — | 18 | — | 20 | — | 25 | ns | |
| Access Time from Column Address | $t_{AVQV}$ | $t_{AA}$ | — | 30 | — | 35 | — | 40 | ns | |
| Access Time from Precharge CAS | $t_{CEHQV}$ | $t_{CPA}$ | — | 35 | — | 40 | — | 45 | ns | |
| RAS Pulse Width | $t_{RELREH}$ | $t_{RAS}$ | 55 | 10 k | 65 | 10 k | 75 | 10 k | ns | |
| RAS Pulse Width (Fast Page Mode) | $t_{RELREH}$ | $t_{RASP}$ | 55 | 200 k | 65 | 200 k | 75 | 200 k | ns | |
| RAS Hold Time | $t_{CELREH}$ | $t_{RSH}$ | 18 | — | 20 | — | 25 | — | ns | |
| CAS Hold Time | $t_{RELCEH}$ | $t_{CSH}$ | 55 | — | 65 | — | 75 | — | ns | |
| CAS Precharge to RAS Hold Time   MCM516400B   MCM517400B | $t_{CEHREH}$ | $t_{RHCP}$ | 40<br>35 | —<br>— | 40<br>40 | —<br>— | 45<br>45 | —<br>— | ns | |
| CAS Pulse Width | $t_{CELCEH}$ | $t_{CAS}$ | 18 | 10 k | 20 | 10 k | 25 | 10 k | ns | |
| Column Address to RAS Lead Time | $t_{AVREH}$ | $t_{RAL}$ | 30 | — | 35 | — | 40 | — | ns | |

# TEST MODE TIMING DIAGRAMS

## WRITE OR $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE (TEST MODE ENTRY)
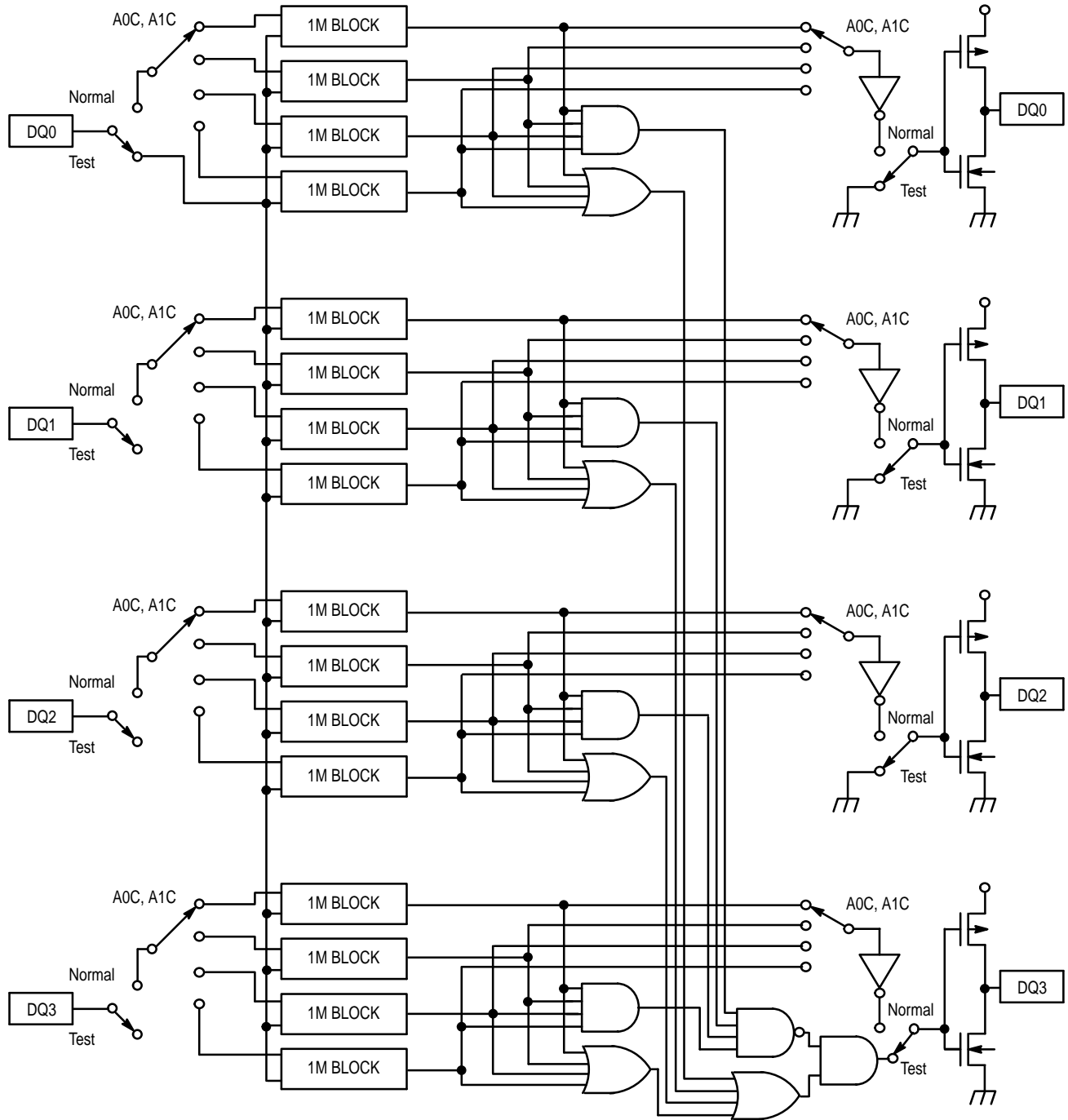### (G and A0 – A10 or 11 are Don't Care)
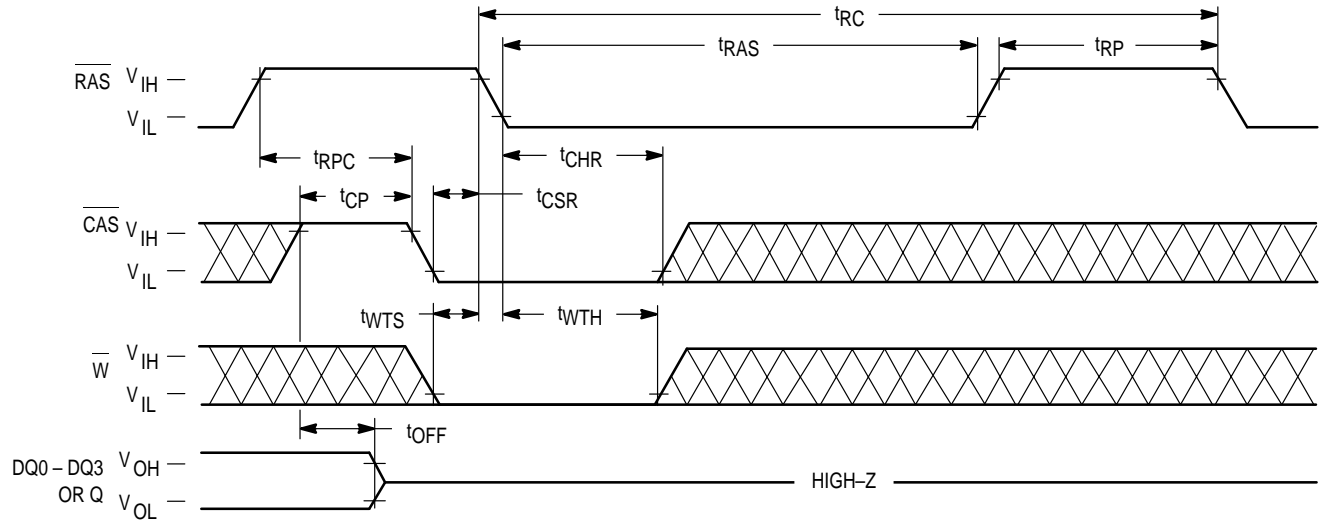


NOTE: Once the device is put into Test Mode with the Test Mode Entry Cycle, any of the standard cycles (Read, Write, Fast Page Mode, etc.) may be used to test the part, providing that the timing parameters are modified as described in the Test Mode AC Operating Conditions and Characteristics table. The timing diagrams previously presented are valid for all cycles performed in Test Mode.

## MODE DEPENDENT ON $\overline{CAS}$ AND $\overline{W}$ WHEN $\overline{RAS}$ FALLS

| Mode | CAS | W* |
|------|-----|-----|
| Read, Write, RMW, FPM | 1 | 0 |
| CBR Refresh, Test Mode Exit | 0 | 1 |
| Test Mode Entry | 0 | 0 |

*Logic state when RAS transitions low.

# TEST MODE BLOCK DIAGRAM
## (MCM516400B, MCM517400B)
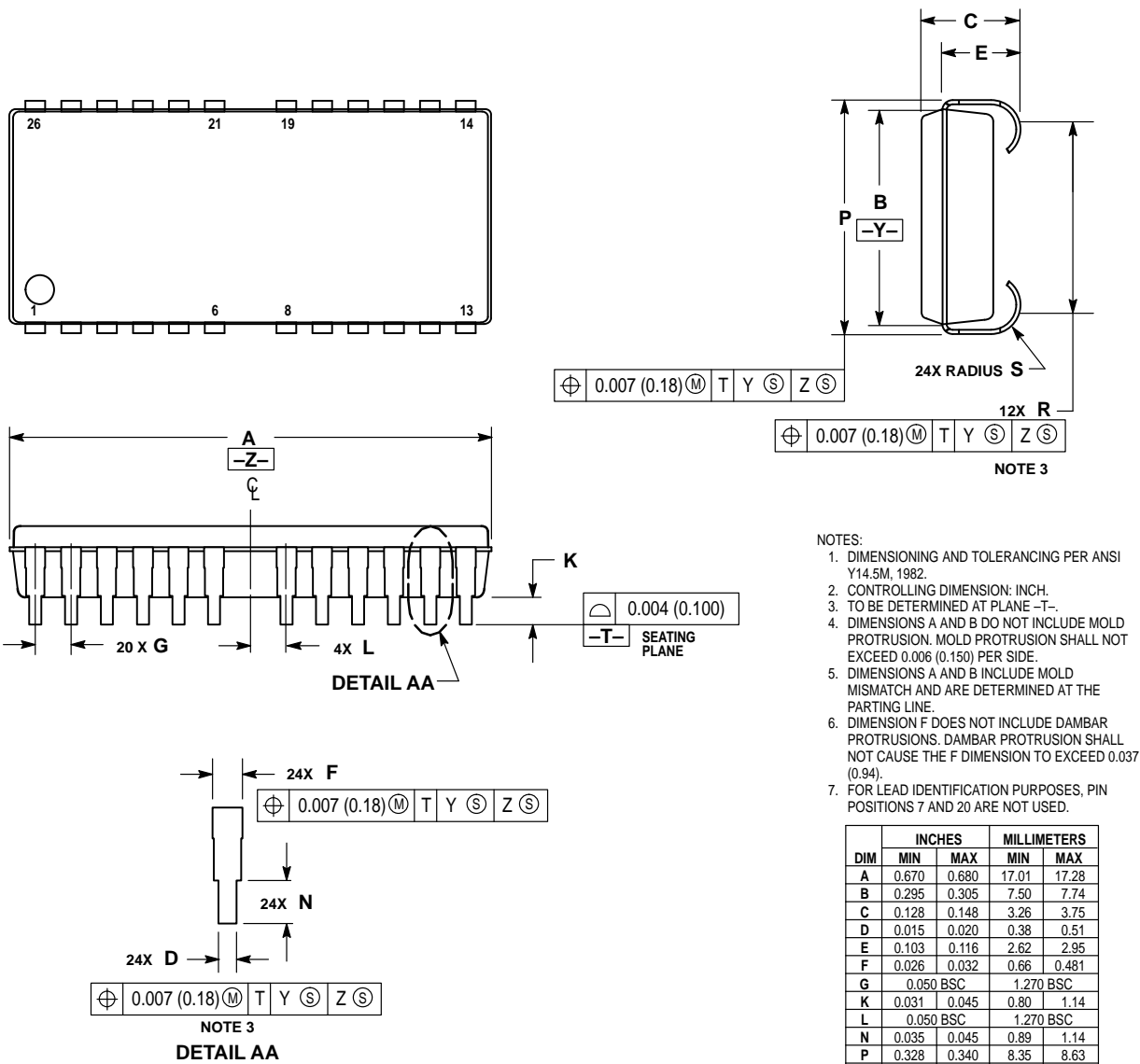
## ORDERING INFORMATION
### (Order by Full Part Number)

```
                   516400
         MCM       517400   X  X  XX   X
```

Motorola Memory Prefix ──────┘          │  │  │    └──── Shipping Method (R = Tape and Reel, Blank = Rails for SOJ,
                                        │  │  │                          Trays for TSOP II)
Part Number ───────────────────────────┘  │  └───────── Speed (50 = 50 ns, 60 = 60 ns, 70 = 70 ns)
Die Revision ──────────────────────────────┘
Package (J = 300 mil SOJ, T = 300 mil TSOP II)
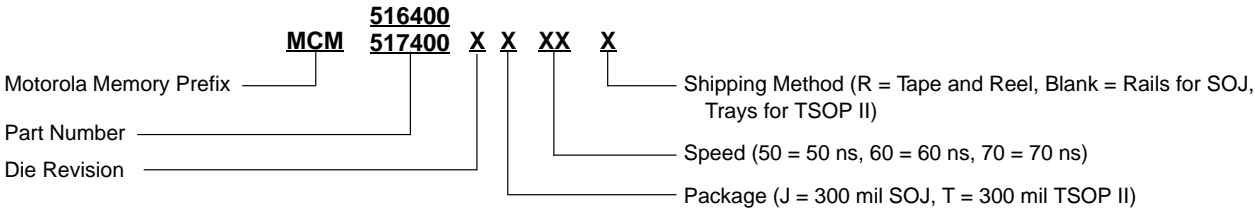
### 16M DEVICE NUMBERS

| | |
|---|---|
| MCM516400BJ50 | MCM517400BJ50 |
| MCM516400BJ60 | MCM517400BJ60 |
| MCM516400BJ70 | MCM517400BJ70 |
| | |
| MCM516400BT50 | MCM517400BT50 |
| MCM516400BT60 | MCM517400BT60 |
| MCM516400BT70 | MCM517400BT70 |
| | |
| MCM516400BJ50R | MCM517400BJ50R |
| MCM516400BJ60R | MCM517400BJ60R |
| MCM516400BJ70R | MCM517400BJ70R |
| | |
| MCM516400BT50R | MCM517400BT50R |
| MCM516400BT60R | MCM517400BT60R |
| MCM516400BT70R | MCM517400BT70R |

# PACKAGE DIMENSIONS

**J PACKAGE**
**300 MIL SOJ**
**CASE 880A–02**



| ⊕ | 0.007 (0.18) Ⓜ | T | Y Ⓢ | Z Ⓢ |

**24X RADIUS S**

**12X R**

| ⊕ | 0.007 (0.18) Ⓜ | T | Y Ⓢ | Z Ⓢ |

**NOTE 3**

| ⌓ | 0.004 (0.100) |
**–T–** SEATING PLANE

**DETAIL AA**

**24X F**

| ⊕ | 0.007 (0.18) Ⓜ | T | Y Ⓢ | Z Ⓢ |

**24X N**

**24X D**

| ⊕ | 0.007 (0.18) Ⓜ | T | Y Ⓢ | Z Ⓢ |

**NOTE 3**

**DETAIL AA**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE –T–.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 (0.150) PER SIDE.
5. DIMENSIONS A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.
6. DIMENSION F DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE F DIMENSION TO EXCEED 0.037 (0.94).
7. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 7 AND 20 ARE NOT USED.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|--------|-------------|--------|
| | MIN | MAX | MIN | MAX |
| A | 0.670 | 0.680 | 17.01 | 17.28 |
| B | 0.295 | 0.305 | 7.50 | 7.74 |
| C | 0.128 | 0.148 | 3.26 | 3.75 |
| D | 0.015 | 0.020 | 0.38 | 0.51 |
| E | 0.103 | 0.116 | 2.62 | 2.95 |
| F | 0.026 | 0.032 | 0.66 | 0.481 |
| G | 0.050 BSC | | 1.270 BSC | |
| K | 0.031 | 0.045 | 0.80 | 1.14 |
| L | 0.050 BSC | | 1.270 BSC | |
| N | 0.035 | 0.045 | 0.89 | 1.14 |
| P | 0.328 | 0.340 | 8.35 | 8.63 |
| R | 0.260 | 0.275 | 6.61 | 6.99 |
| S | 0.030 | 0.040 | 0.77 | 1.01 |

**T PACKAGE**
**300 MIL TSOP II**
**CASE 892A–02**

DETAIL AA



12X **S**

$\oplus$ | 0.008 (0.200) Ⓜ | T | Y Ⓢ

**B**
**–Y–**

**AB**  **AB**

26   21   19   14

1   6   8   13

**A**
**–Z–**

**C**

$\mathbb{C}_L$

$\bigcirc$ | 0.004 (0.100)

**–T–**  SEATING PLANE

4X **R**

20 X **G**

BASE METAL

**F**

**J**

**N**

**D**

$\oplus$ | 0.008 (0.200) Ⓜ | T | Z Ⓢ

**SECTION AB–AB**
**24 PLACES**

RADIUS **V**

RADIUS **T**

**L**

**K**

**W**

**DETAIL AA**
ROTATED 90° CLOCKWISE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.006 (0.150) PER SIDE.
4. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.025 (0.635).
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 7 AND 20 ARE NOT USED.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|--------|-------------|--------|
| | MIN | MAX | MIN | MAX |
| A | 0.671 | 0.679 | 17.04 | 17.25 |
| B | 0.296 | 0.304 | 7.520 | 7.720 |
| C | — | 0.047 | — | 1.200 |
| D | 0.014 | 0.020 | 0.350 | 0.510 |
| F | 0.014 | 0.018 | 0.350 | 0.460 |
| G | 0.050 BSC | | 1.270 BSC | |
| J | 0.004 | 0.008 | 0.100 | 0.200 |
| K | 0.016 | 0.024 | 0.400 | 0.600 |
| L | 0.002 | 0.008 | 0.050 | 0.200 |
| N | 0.0045 | 0.0055 | 0.100 | 0.140 |
| R | 0.050 BSC | | 1.270 BSC | |
| S | 0.355 | 0.371 | 9.020 | 9.420 |
| T | 0.004 REF | | 0.100 REF | |
| V | 0.004 REF | | 0.100 REF | |
| W | 0° | 10° | 0° | 10° |

🅜 **MOTOROLA**

◊

**MCM516400B/D**