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## 32 Bit PCI Target

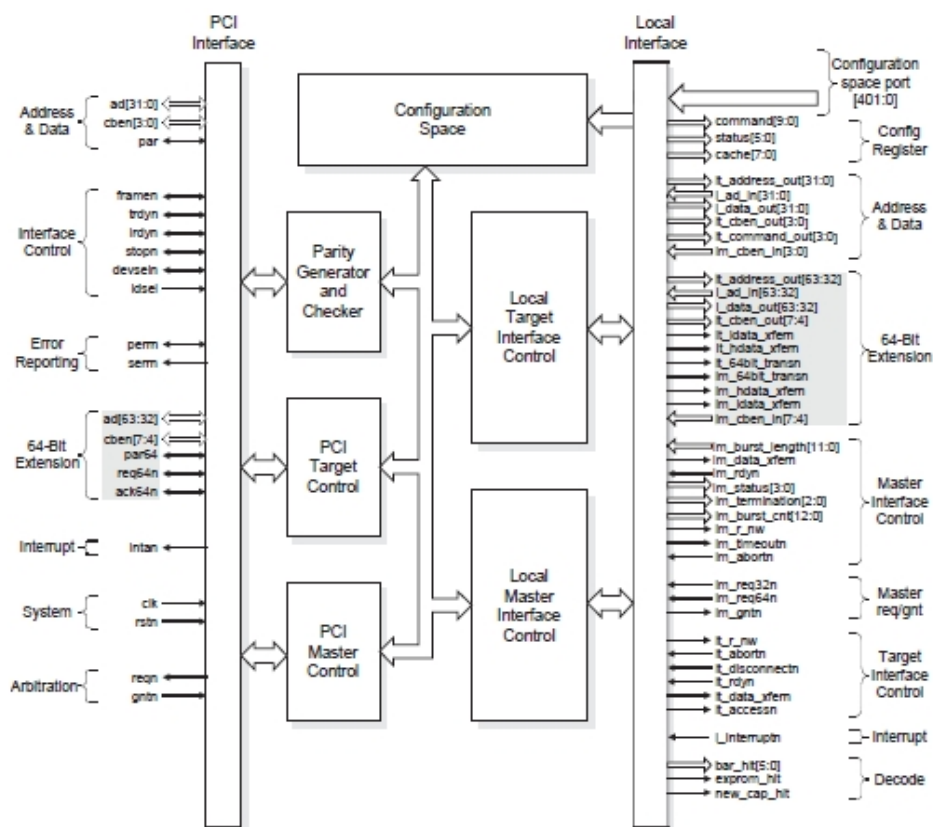
### Overview

**Peripheral Component Interconnect (PCI)** is a widely accepted bus standard that is used in many applications including telecommunications, embedded systems, high performance peripheral cards, and networking.



**Lattice's PCI IP core** provides an ideal solution that meets the needs of today's high performance PCI applications. It is fully compliant with the PCI Local Bus Specification, revision 2.2 for speeds up to 66MHz. The PCI core provides a **customizable 32/64-bit master/target** or target solution. The core bridges the gap between the PCI interface and a specific design application, providing an integrated PCI solution. The PCI solution allows designers to focus on the application rather than on the PCI specification, resulting in a faster time-to-market.

The Lattice PCI offering is available in a number of configurations covering 32-bit PCI, 64-bit PCI, 32-bit local bus, 64-bit local bus, master/target and target applications. In this document, details of 64-bit operation and master operation only apply when relevant. The appendix to the user's guide shows what cores are available on which devices.



Note: Signals in shaded boxes are used for 64-bit PCI Cores.

### Features

Available as 32/64-Bit PCI Bus and 32/64-Bit Local Bus  
PCI SIG Local Bus Specification, Revision 3.0 Compliant  
64-Bit Addressing Support (Dual Address Cycle)

Fast Back-to-Back Transaction Support  
Supports Zero Wait State Transactions  
Special Cycle Transaction Support

Capabilities List Pointer Support

Customizable Configuration Space

Parity Error Detection

Up to 66MHz PCI

Up to Six Base Address Registers (BARs)

Fully Synchronous Design

## Performance and Resource Utilization

LatticeECP3<sup>1</sup>

| Bus Width | IPexpress Mode | Slices | LUTs | Registers | sysMEM EBRs | External Pins | f <sub>MAX</sub> (MHz) |
|-----------|----------------|--------|------|-----------|-------------|---------------|------------------------|
| 32-bit    | Target 33 MHz  | 483    | 706  | 470       | -           | 48            | 33                     |
| 32-bit    | Target 66 MHz  | 589    | 963  | 491       | -           | 48            | 66                     |

1. Performance and utilization data are generated using an LFE3-95EA-7FN1156CES device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

LatticeECP2M<sup>1</sup>

| Bus Width | IPexpress Mode | Slices | LUTs | Registers | sysMEM EBRs | External Pins | f <sub>MAX</sub> (MHz) |
|-----------|----------------|--------|------|-----------|-------------|---------------|------------------------|
| 32-bit    | Target 33 MHz  | 593    | 717  | 472       | -           | 48            | 33                     |
| 32-bit    | Target 66 MHz  | 606    | 972  | 493       | -           | 48            | 66                     |

1. Performance and utilization data are generated using an LFE2M-35E-6F672C device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M family.

LatticeECP2<sup>1</sup>

| Bus Width | IPexpress Mode | Slices | LUTs | Registers | sysMEM EBRs | External Pins | f <sub>MAX</sub> (MHz) |
|-----------|----------------|--------|------|-----------|-------------|---------------|------------------------|
| 32-bit    | Target 33 MHz  | 593    | 717  | 472       | -           | 48            | 33                     |
| 32-bit    | Target 66 MHz  | 606    | 972  | 493       | -           | 48            | 66                     |

1. Performance and utilization data are generated using an LFE2-20E-6F672C device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2 family.

LatticeEC/P<sup>1</sup>

| Bus Width | IPexpress Mode | Slices | LUTs | Registers | sysMEM EBRs | External Pins | f <sub>MAX</sub> (MHz) |
|-----------|----------------|--------|------|-----------|-------------|---------------|------------------------|
| 32-bit    | Target 33 MHz  | 586    | 703  | 472       | -           | 48            | 33                     |
| 32-bit    | Target 66 MHz  | 606    | 966  | 493       | -           | 48            | 66                     |

1. Performance and utilization data are generated using an LFEC33E-5F672C device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP/EC family.

LatticeSC<sup>1</sup>

| Bus Width | IPexpress Mode | Slices | LUTs | Registers | sysMEM EBRs | External Pins | f <sub>MAX</sub> (MHz) |
|-----------|----------------|--------|------|-----------|-------------|---------------|------------------------|
| 32-bit    | Target 33 MHz  | 488    | 679  | 470       | -           | 48            | 33                     |
| 32-bit    | Target 66 MHz  | 618    | 990  | 493       | -           | 48            | 66                     |

Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeSC family.

#### MachXO2<sup>1</sup>

| Bus Width | IPexpress Mode | Slices | LUTs | Registers | sysMEM EBRs | External Pins | f <sub>MAX</sub> (MHz) |
|-----------|----------------|--------|------|-----------|-------------|---------------|------------------------|
| 32-bit    | Target 33 MHz  | 304    | 601  | 422       | -           | 48            | 33                     |

1. Preliminary information. Performance and utilization characteristics are generated using LCMXO2-1200HC-6TG144CES device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the MachXO2 family.

#### MachXO<sup>1</sup>

| Bus Width | IPexpress Mode | Slices | LUTs | Registers | sysMEM EBRs | External Pins | f <sub>MAX</sub> (MHz) |
|-----------|----------------|--------|------|-----------|-------------|---------------|------------------------|
| 32-bit    | Target 33 MHz  | 359    | 703  | 472       | -           | 48            | 33                     |
| 32-bit    | Target 66 MHz  | 517    | 966  | 493       | -           | 48            | 66                     |

1. Performance and utilization data are generated using an LCMXO2280C-5FT324C device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the MachXO family.

#### LatticeXP2<sup>1</sup>

| Bus Width | IPexpress Mode | Slices | LUTs | Registers | sysMEM EBRs | External Pins | f <sub>MAX</sub> (MHz) |
|-----------|----------------|--------|------|-----------|-------------|---------------|------------------------|
| 32-bit    | Target 33 MHz  | 588    | 709  | 470       | -           | 48            | 33                     |
| 32-bit    | Target 66 MHz  | 601    | 964  | 491       | -           | 48            | 66                     |

1. Performance and utilization data are generated using an LFXP2-17E-6F484C device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP2 family.

#### LatticeXP<sup>1</sup>

| Bus Width | IPexpress Mode | Slices | LUTs | Registers | sysMEM EBRs | External Pins | f <sub>MAX</sub> (MHz) |
|-----------|----------------|--------|------|-----------|-------------|---------------|------------------------|
| 32-bit    | Target 33 MHz  | 586    | 703  | 472       | -           | 48            | 33                     |
| 32-bit    | Target 66 MHz  | 606    | 966  | 493       | -           | 48            | 66                     |

1. Performance and utilization data are generated using an LFXP20C-5F484C device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP family.

## Ordering Information

| Family        | Bus Width | Bus Speed    | Target Part Number |
|---------------|-----------|--------------|--------------------|
| LatticeECP3   | 32-bit    | 33MHz, 66MHz | PCI-T32-E3-U6      |
| LatticeECP2M  | 32-bit    | 33MHz, 66MHz | PCI-T32-PM-U6      |
| LatticeECP2   | 32-bit    | 33MHz, 66MHz | PCI-T32-P2-U6      |
| LatticeECP/EC | 32-bit    | 33MHz, 66MHz | PCI-T32-E2-U6      |
| LatticeSC     | 32-bit    | 33MHz, 66MHz | PCI-T32-SC-U6      |
| MachXO2       | 32-bit    | 33MHz        | PCI-T32-M2-U1      |
| MachXO        | 32-bit    | 33MHz        | PCI-T32-XO-U6      |
| LatticeXP2    | 32-bit    | 33MHz, 66MHz | PCI-T32-X2-U6      |
| LatticeXP     | 32-bit    | 33MHz, 66MHz | PCI-T32-XM-U6      |

**IP Version:** PCI Target 33MHz = 6.5, PCI Target 66MHz = 6.3

**Evaluate:** To download a full evaluation version of this IP, go to the Lattice IP Server tab in the IPexpress Main Window. All ispLeverCORE IP cores and modules available for download are visible on this tab. \*PCI cores for ORCA and ispXPGA, devices are supported by the Lattice factory-configurable design flow.

**Purchase:** To find out how to purchase the IP Core, please contact your [local Lattice Sales Office](#).