

Overview

The M16C/62 group (M16C/62P) of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

Applications

Audio, cameras, office/communications/portable/industrial equipment, etc

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

Performance Outline

Table 1.1.1 lists performance outline of M16C/62P group.

Table 1.1.1. Performance outline of M16C/62P group

Item		Performance	
Number of basic instructions		91 instructions	
Shortest instruction execution time		41.7 ns (f(BCLK)= 24MHz, Vcc1= 3.0V to 5.5V) 100 ns (f(BCLK)= 10MHz, Vcc1= 2.7V to 5.5V)	
Memory capacity	ROM RAM	(See the product list) (See the product list)	
I/O port	100-pin version P0 to P10 (except P85)	8 bits x 10, 7 bits x 1	P0 to P5: Vcc2 ports P6 to P10: Vcc1 ports
	128-pin version P0 to P14 (except P85)	8 bits x 13, 7 bits x 1, 2 bits x 1	P0 to P5, P12, P13: Vcc2 ports P6 to P10, P11, P14: Vcc1 ports
Input port	P85	1 bit x 1 (NMI pin level judgment): Vcc1 ports	
Multifunction timer			
Output		16 bits x 5 channels (TA0, TA1, TA2, TA3, TA4)	
Input		16 bits x 6 channels (TB0, TB1, TB2, TB3, TB4, TB5)	
Serial I/O		3 channels (UART0, UART1, UART2) UART, clock synchronous, I ² C bus ¹ (option ⁴), or IEBus ² (option ⁴) 2 channels (SI/O3, SI/O4) Clock synchronous	
A-D converter		10 bits x (8 x 3 + 2) channels	
D-A converter		8 bits x 2	
DMAC		2 channels (trigger: 25 sources)	
CRC calculation circuit		CRC-CCITT	
Watchdog timer		15 bits x 1 (with prescaler)	
Interrupt		29 internal and 8 external sources, 4 software sources, 7 levels	
Clock generation circuit		4 circuits • Main clock • Sub-clock • Ring oscillator(main-clock oscillation stop detect function) • PLL frequency synthesizer (These circuits contain a built-in feedback resistor and external ceramic/quartz oscillator)	
Voltage detection circuit		Present (option ⁴)	
Power supply voltage		Vcc1=3.0V to 5.5V, Vcc2=3.0V to Vcc1(f(BCLK)=24MHz) Vcc1=Vcc2=2.7V to 5.5V (f(BCLK)=10MHz)	
Flash memory	Program/erase voltage	3.3V ± 0.3V or 5.0V ± 0.5V	
	Number of program/erase	100 times, 10000 times ³ (option ⁴)	
Power consumption		14mA (Vcc1=Vcc2=5V, f(BCLK)=24MHz) 8mA (Vcc1=Vcc2=3V, f(BCLK)=10MHz) 1.8μA (Vcc1=Vcc2=3V, f(XCIN)=32kHz, when wait mode)	
I/O characteristics	I/O withstand voltage	5.0V	
	Output current	5mA	
Memory expansion		Available (to 4M bytes)	
Operating ambient temperature		-20 to 85°C -40 to 85°C (option ⁴)	
Device configuration		CMOS high performance silicon gate	
Package		100-pin and 128-pin plastic mold QFP	

Notes:

1. I²C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. Block 1 and block A are a 10,000 times of programming and erasure. All other blocks are guaranteed of 1,000 times of programming and erasure. (Under development; mass production scheduled to start in the 3rd quarter of 2003)
4. If you desire this option, please so specify.

Block Diagram

Figure 1.1.1 is a block diagram of the M16C/62P group.

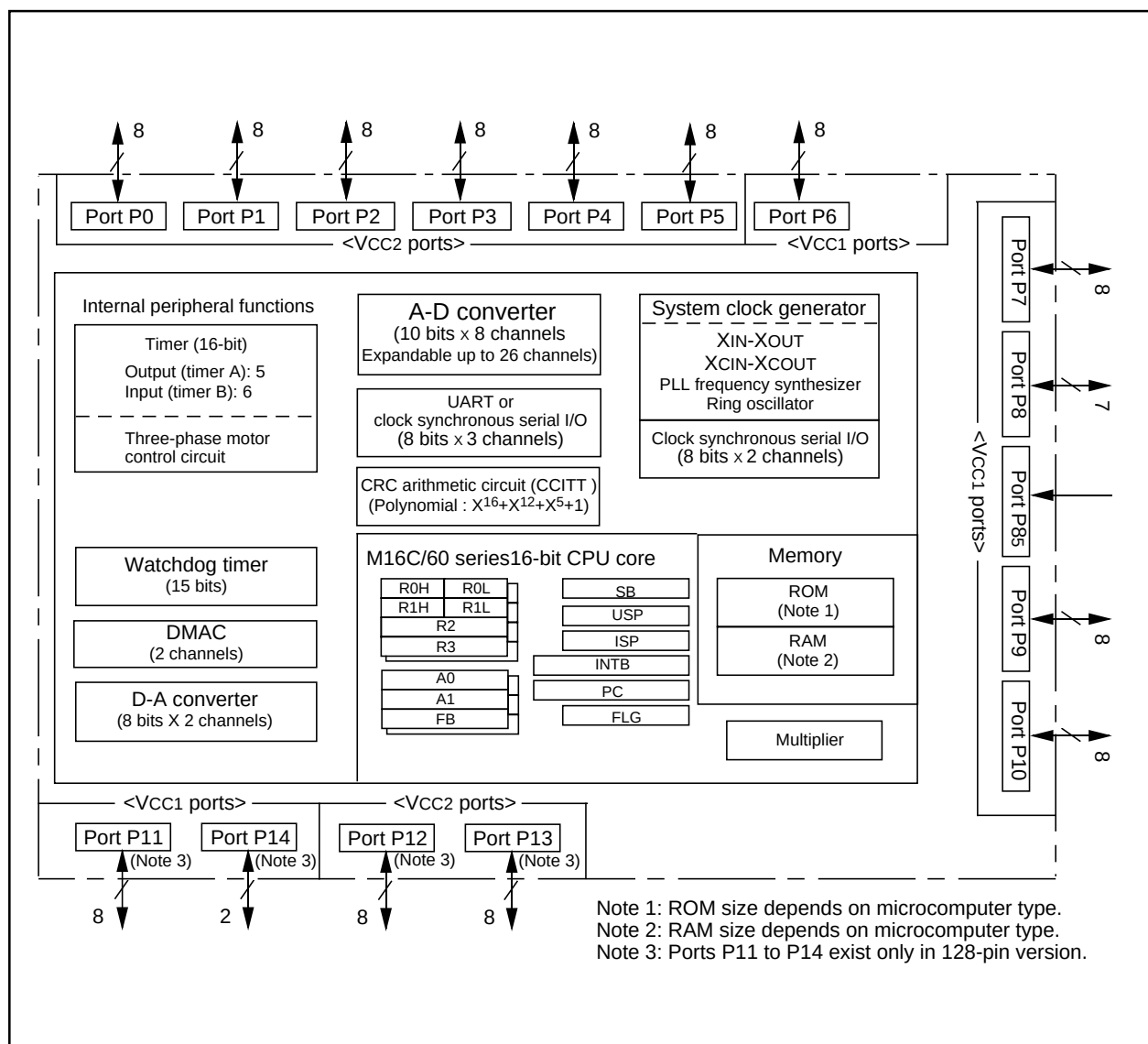


Figure 1.1.1. Block Diagram

Product List

Tables 1.1.2 and 1.1.3 list the M16C/62P group products and Figure 1.1.2 shows the type numbers, memory sizes and packages.

Table 1.1.2. Product List (1)

As of April 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30622M6P-XXXFP ★	48K bytes	4K bytes	100P6S-A	MASK ROM version
M30622M6P-XXXGP ★			100P6Q-A	
M30622M8P-XXXFP ★	64K bytes	4K bytes	100P6S-A	
M30622M8P-XXXGP ★			100P6Q-A	
M30622MAP-XXXFP ★	96K bytes	5K bytes	100P6S-A	
M30622MAP-XXXGP ★			100P6Q-A	
M30620MCP-XXXFP ★	128K bytes	10K bytes	100P6S-A	
M30620MCP-XXXGP ★			100P6Q-A	
M30622MEP-XXXFP ★	192K bytes	12K bytes	100P6S-A	
M30622MEP-XXXGP ★			100P6Q-A	
M30623MEP-XXXGP ★			128P6Q-A	
M30622MGP-XXXFP ★	256K bytes	12K bytes	100P6S-A	
M30622MGP-XXXGP ★			100P6Q-A	
M30623MGP-XXXGP ★			128P6Q-A	
M30624MGP-XXXFP ★		20K bytes	100P6S-A	
M30624MGP-XXXGP ★			100P6Q-A	
M30625MGP-XXXGP ★			128P6Q-A	
M30622MWP-XXXFP ★	320K bytes	16K bytes	100P6S-A	
M30622MWP-XXXGP ★			100P6Q-A	
M30623MWP-XXXGP ★			128P6Q-A	
M30624MWP-XXXFP		24K bytes	100P6S-A	
M30624MWP-XXXGP			100P6Q-A	
M30625MWP-XXXGP ★			128P6Q-A	
M30626MWP-XXXFP ★		31K bytes	100P6S-A	
M30626MWP-XXXGP ★			100P6Q-A	
M30627MWP-XXXGP ★			128P6Q-A	
M30622MHP-XXXFP ★	384K bytes	16K bytes	100P6S-A	
M30622MHP-XXXGP ★			100P6Q-A	
M30623MHP-XXXGP ★			128P6Q-A	
M30624MHP-XXXFP ★		24K bytes	100P6S-A	
M30624MHP-XXXGP			100P6Q-A	
M30625MHP-XXXGP ★			128P6Q-A	
M30626MHP-XXXFP		31K bytes	100P6S-A	
M30626MHP-XXXGP			100P6Q-A	
M30627MHP-XXXGP ★			128P6Q-A	

★ : Under development
 ★★ : Under planning

Table 1.1.3. Product List (2)

As of April 2003

Type No.		ROM capacity	RAM capacity	Package type	Remarks
M30622F8PFP	★	64K bytes	4K bytes	100P6S-A	Flash memory version
M30622F8PGP	★			100P6Q-A	
M30620FCPFP	★	128K bytes	10K bytes	100P6S-A	
M30620FCPGP	★			100P6Q-A	
M30624FGPFP		256K bytes	20K bytes	100P6S-A	
M30624FGPGP				100P6Q-A	
M30625FGPGP	★			128P6Q-A	
M30626FHPFP		384K bytes	31K bytes	100P6S-A	
M30626FHPPGP				100P6Q-A	
M30627FHPPGP				128P6Q-A	
M30626FJPFP	★★	512K bytes	31K bytes	100P6S-A	
M30626FJPGP	★★			100P6Q-A	
M30627FJPGP	★★			128P6Q-A	
M30620SPFP	★		10K bytes	100P6S-A	External ROM version
M30620SPGP	★			100P6Q-A	
M30622SPFP	★		4K bytes	100P6S-A	
M30622SPGP	★			100P6Q-A	

★ : Under development
 ★★ : Under planning

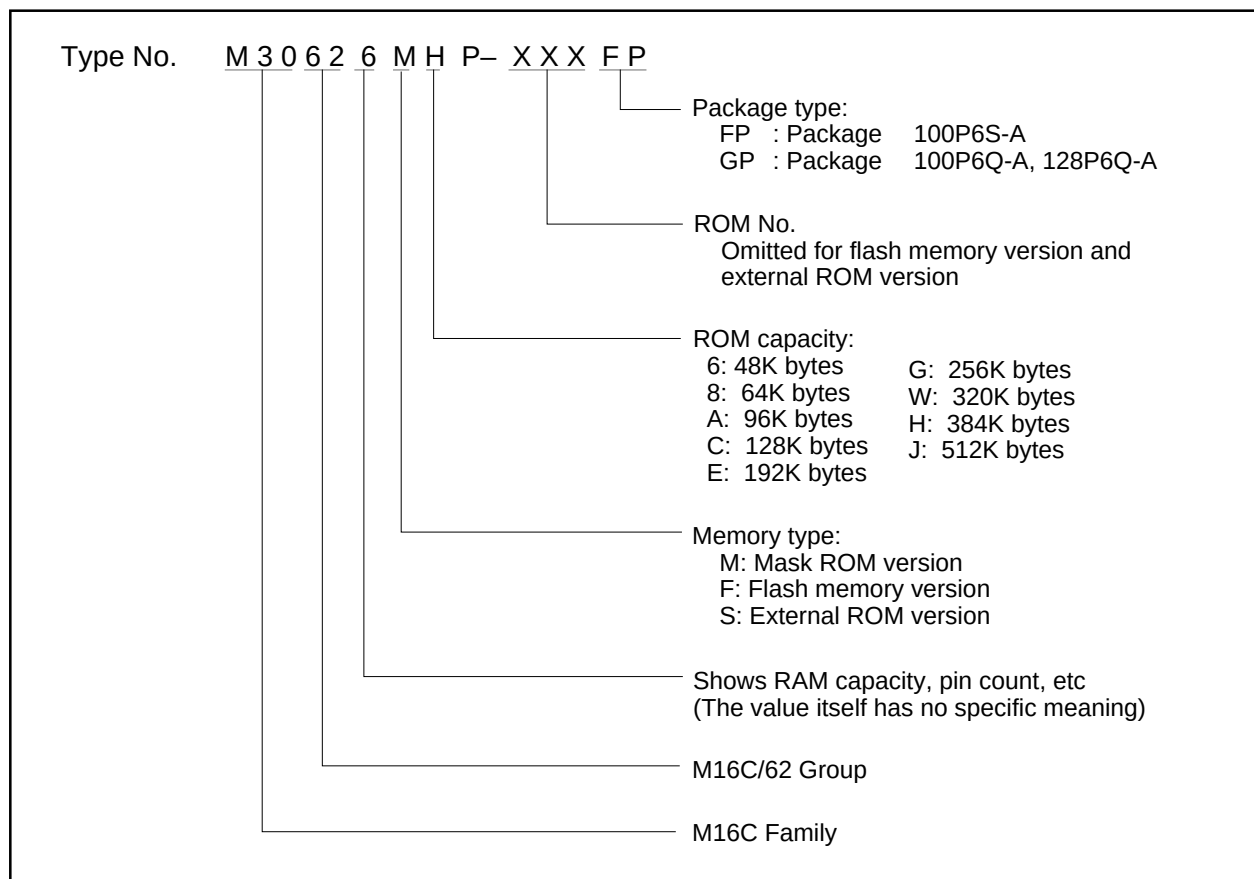


Figure 1.1.2. Type No., Memory Size, and Package

Pin Configuration

Figures 1.1.3 to 1.1.5 show the pin configurations (top view).

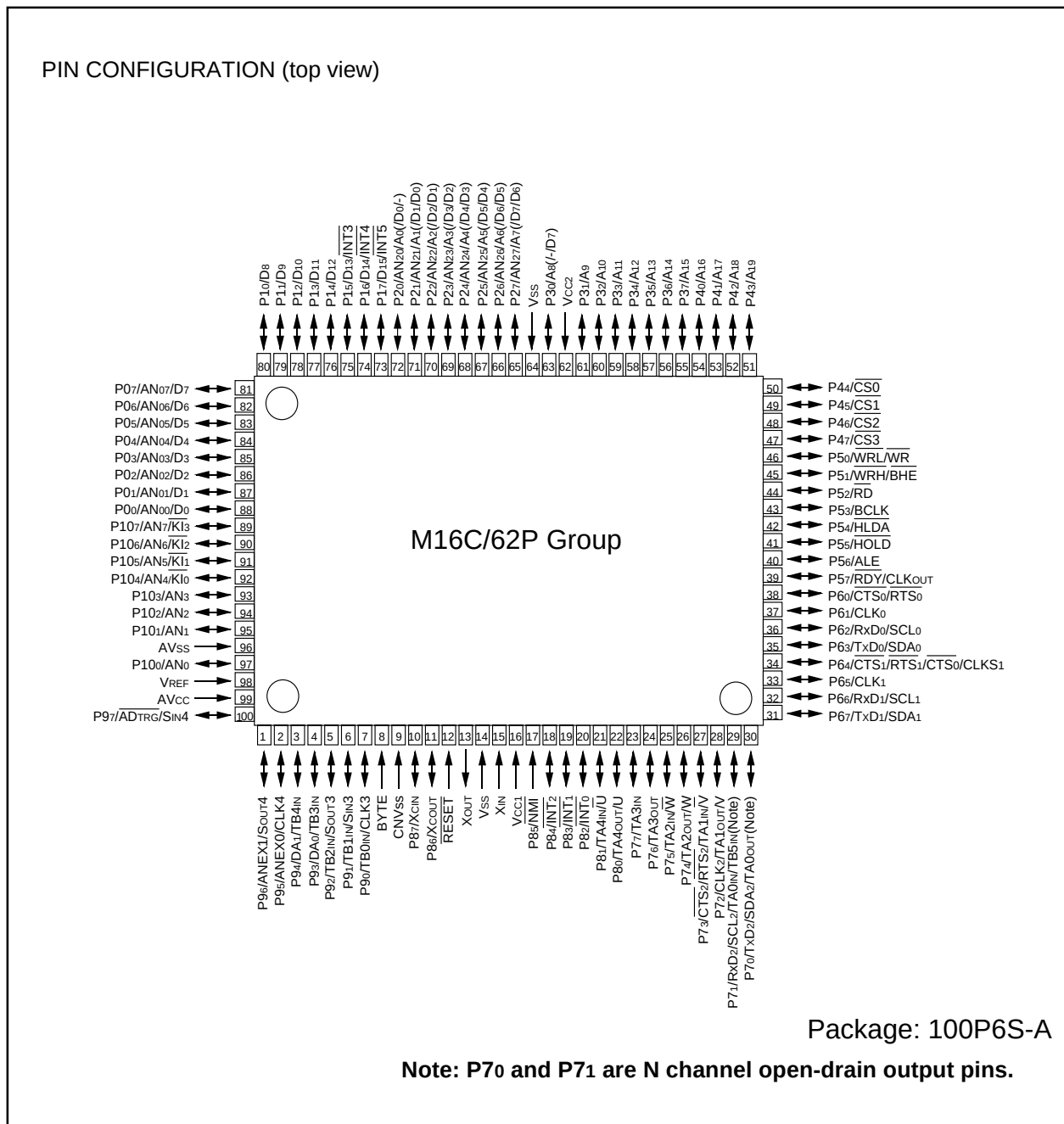


Figure 1.1.3. Pin Configuration (Top View)

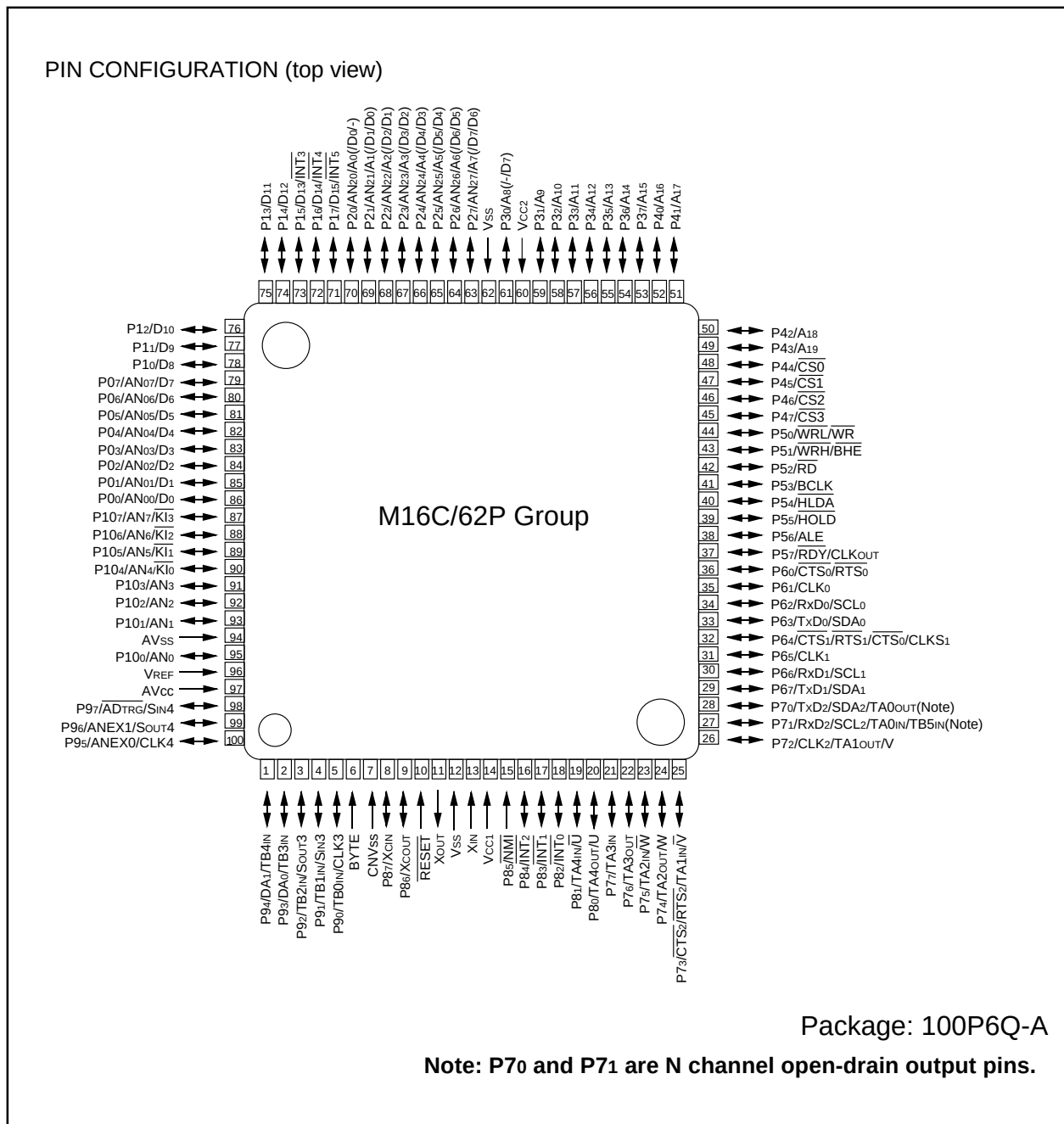


Figure 1.1.4. Pin Configuration (Top View)

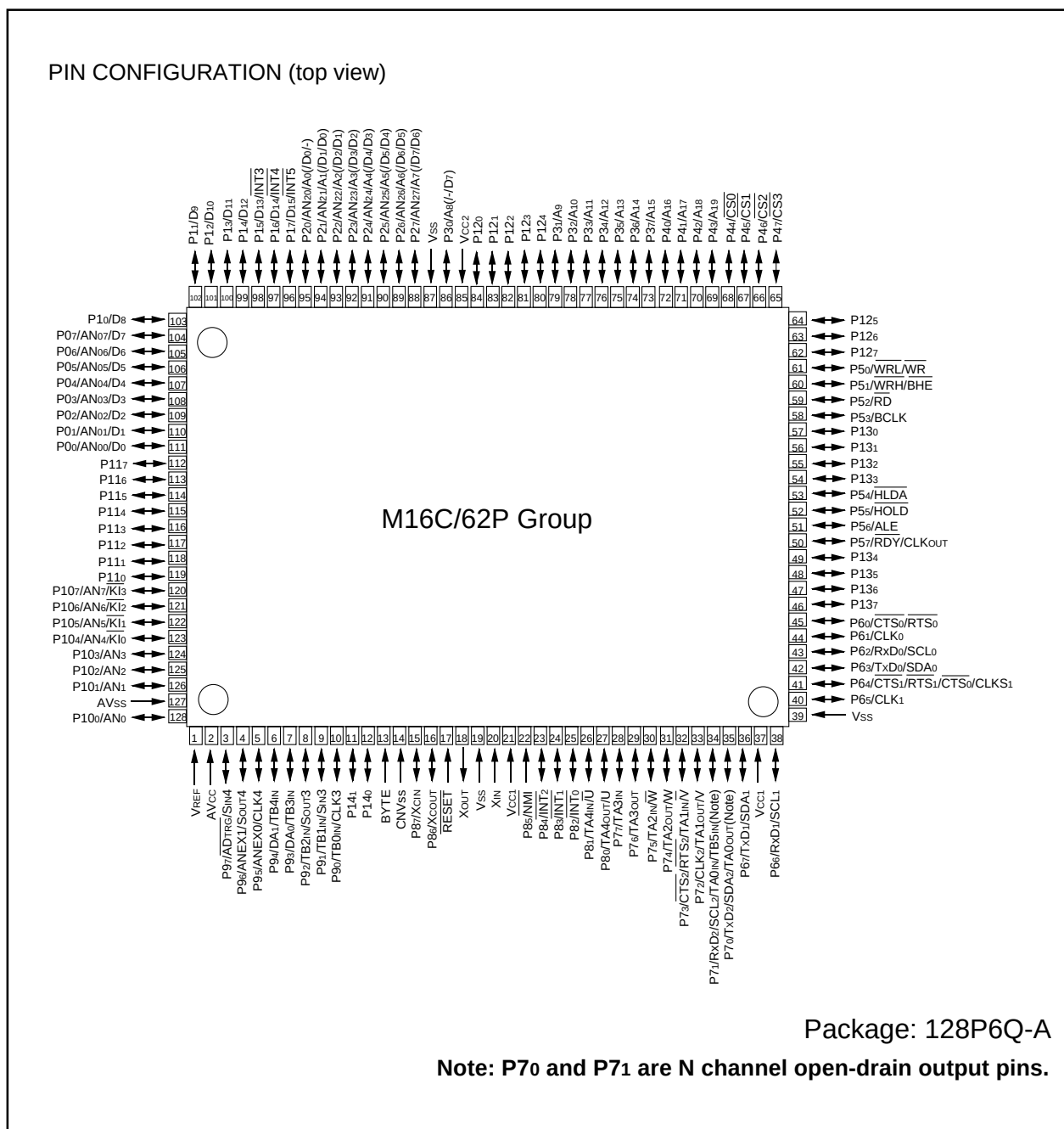


Figure 1.1.5. Pin Configuration (Top View)

Table 1.1.4 Pin Description (100-pin and 128-pin Packages)

Pin name	Signal name	I/O type	Power supply	Function
VCC1, VCC2, VSS	Power supply input		—	Apply 2.7V to 5.5 V to the VCC1 and VCC2 pins and 0 V to the VSS pin. The Vcc apply condition is that $VCC2 \leq VCC1$ (Note)
CNVSS	CNVSS	Input	VCC1	This pin switches between processor modes. Connect this pin to VSS pin when after a reset you want to start operation in single-chip mode (memory expansion mode) or the VCC1 pin when starting operation in microprocessor mode.
RESET	Reset input	Input	VCC1	"L" on this input resets the microcomputer.
XIN XOUT	Clock input Clock output	Input Output	VCC1	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or crystal between the XIN and the XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
BYTE	External data bus width select input	Input		This pin selects the width of an external data bus. A 16-bit width is selected when this input is "L"; an 8-bit width is selected when this input is "H". This input must be fixed to either "H" or "L". Connect this pin to the VSS pin when operating in single-chip mode.
AVCC	Analog power supply input			This pin is a power supply input for the A-D converter. Connect this pin to VCC1.
AVSS	Analog power supply input			This pin is a power supply input for the A-D converter. Connect this pin to VSS.
VREF	Reference voltage input	Input		This pin is a reference voltage input for the A-D converter.
P00 to P07	I/O port P0	Input/output	VCC2	This is an 8-bit CMOS I/O port. This port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. If any port is set for input, selection can be made for it in a program whether or not to have a pull-up resistor in 4 bit units. This selection is unavailable in memory extension and microprocessor modes. This port can function as input pins for the A-D converter when so selected in a program.
D0 to D7		Input/output		When set as a separate bus, these pins input and output data (D0–D7).
P10 to P17	I/O port P1	Input/output	VCC2	This is an 8-bit I/O port equivalent to P0. P15 to P17 also function as INT interrupt input pins as selected by a program.
D8 to D15		Input/output		When set as a separate bus, these pins input and output data (D8–D15).
P20 to P27	I/O port P2	Input/output	VCC2	This is an 8-bit I/O port equivalent to P0. This port can function as input pins for the A-D converter when so selected in a program.
A0 to A7		Output		These pins output 8 low-order address bits (A0 to A7).
A0/D0 to A7/D7		Input/output		If the external bus is set as an 8-bit wide multiplexed bus, these pins input and output data (D0 to D7) and output 8 low-order address bits (A0 to A7) separated in time by multiplexing.
A0 A1/D0 to A7/D6		Output Input/output		If the external bus is set as a 16-bit wide multiplexed bus, these pins input and output data (D0 to D6) and output address (A1 to A7) separated in time by multiplexing. They also output address (A0).
P30 to P37	I/O port P3	Input/output	VCC2	This is an 8-bit I/O port equivalent to P0.
A8 to A15		Output		These pins output 8 middle-order address bits (A8 to A15).
A8/D7, A9 to A15		Input/output Output		If the external bus is set as a 16-bit wide multiplexed bus, these pins input and output data (D7) and output address (A8) separated in time by multiplexing. They also output address (A9 to A15).
P40 to P47	I/O port P4	Input/output	VCC2	This is an 8-bit I/O port equivalent to P0.
A16 to A19, CS0 to CS3		Output Output		These pins output A16 to A19 and CS0 to CS3 signals. A16 to A19 are 4 high-order address bits. CS0 to CS3 are chip select signals used to specify an access space.

Note: In this manual, hereafter, Vcc refers to VCC1 unless otherwise noted.

Table 1.1.5 Pin Description (100-pin and 128-pin Packages) (Continued)

Pin name	Signal name	I/O type	Power supply	Function
P50 to P57	I/O port P5	Input/output	VCC2	This is an 8-bit I/O port equivalent to P0. In single-chip mode, P57 in this port outputs a divide-by-8 or divide-by-32 clock of XIN or a clock of the same frequency as XCIN as selected by program.
WRL / WR, WRH / BHE, RD, BCLK, HLDA, HOLD, ALE, RDY		Output Output Output Output Input Output Input		Output WRL/WR, WRH/BHE, RD, BCLK, HLDA, and ALE signals. WRL/WR and WRH/BHE are switchable in a program. Note that WRL and WRH are always used as a pair, so as WR and BHE. ■ WRL, WRH, and RD selected If the external data bus is 16 bits wide, data are written to even addresses when the WRL signal is low, and written to odd addresses when the WRH signal is low. Data are read out when the RD signal is low. ■ WR, BHE, and RD selected Data are written when the WR signal is low, or read out when the RD signal is low. Odd addresses are accessed when the BHE signal is low. Use this mode when the external data bus is 8 bits wide. The microcomputer goes to a hold state when input to the HOLD pin is held low. While in the hold state, HLDA outputs a low level. ALE is used to latch the address. While the input level of the RDY pin is low, the bus of the microcomputer goes to a wait state.
P60 to P67	I/O port P6	Input/output	VCC1	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as UART0 and UART1 I/O pins as selected by program.
P70 to P77	I/O port P7	Input/output	VCC1	This is an 8-bit I/O port equivalent to P0 (P70 and P71 are N channel open-drain output). This port can function as input/output pins for timers A0 to A3 when so selected in a program. Furthermore, P70 to P75, P71, and P72 to P75 can also function as input/output pins for UART2, an input pin for timer B5, and output pins for the three-phase motor control timer, respectively.
P80 to P84, P86, P87, P85	I/O port P8 I/O port P85	Input/output Input/output Input/output Input	VCC1	P80 to P84, P86, and P87 are I/O ports with the same functions as P0. When so selected in a program, P80 to P81 and P82 to P84 can function as input/output pins for timer A4 or output pins for the three-phase motor control timer and INT interrupt input pins, respectively. P86 and P87, when so selected in a program, both can function as input/output pins for the subclock oscillator circuit. In that case, connect a crystal resonator between P86 (XCOUT pin) and P87 (XCIN pin). P85 is an input-only port shared with NMI. An NMI interrupt request is generated when input on this pin changes state from high to low. The NMI function cannot be disabled in a program. A pull-up cannot be set for this pin.
P90 to P97	I/O port P9	Input/output	VCC1	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as SI/O3 and SI/O4 I/O pins, Timer B0 to B4 input pins, D-A converter output pins, A-D converter input pins, or A-D trigger input pins as selected by program.
P100 to P107	I/O port P10	Input/output	VCC1	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as A-D converter input pins as selected by program. Furthermore, P104 to P107 also function as input pins for the key input interrupt function.

Table 1.1.6 Pin Description (128-pin Package)

Pin name	Signal name	I/O type	Power supply circuit block	Function
P110 to P117	I/O port P11	Input/output	VCC1	This is an 8-bit I/O port equivalent to P0.
P120 to P127	I/O port P12	Input/output	VCC2	This is an 8-bit I/O port equivalent to P0.
P130 to P137	I/O port P13	Input/output	VCC2	This is an 8-bit I/O port equivalent to P0.
P140, P141	I/O port P14	Input/output	VCC1	This is a 2-bit I/O port equivalent to P0.

Memory

Figure 1.2.1 is a memory map of the M16C/62P group. The address space extends the 1M bytes from address 00000₁₆ to FFFFF₁₆.

The internal ROM is allocated in a lower address direction beginning with address FFFFF₁₆. For example, a 64-Kbyte internal ROM is allocated to the addresses from F0000₁₆ to FFFFF₁₆.

The fixed interrupt vector table is allocated to the addresses from FFFDC₁₆ to FFFFF₁₆. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400₁₆. For example, a 10-Kbytes internal RAM is allocated to the addresses from 00400₁₆ to 02BFF₁₆. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SRF is allocated to the addresses from 00000₁₆ to 003FF₁₆. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from FFE00₁₆ to FFFDB₁₆. This vector is used by the JMPS or JSRS instruction. For details, refer to the “M16C/60 and M16C/20 Series Software Manual.” In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users.

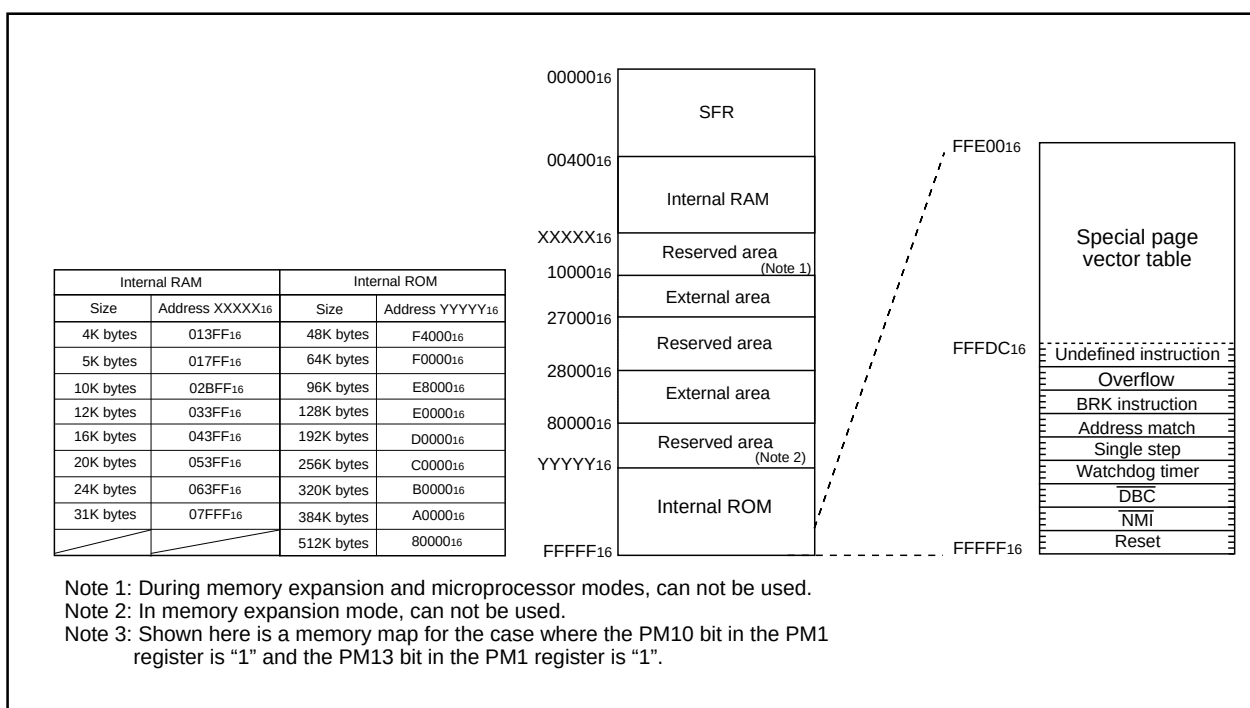


Figure 1.2.1. Memory Map

Central Processing Unit (CPU)

Figure 1.3.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

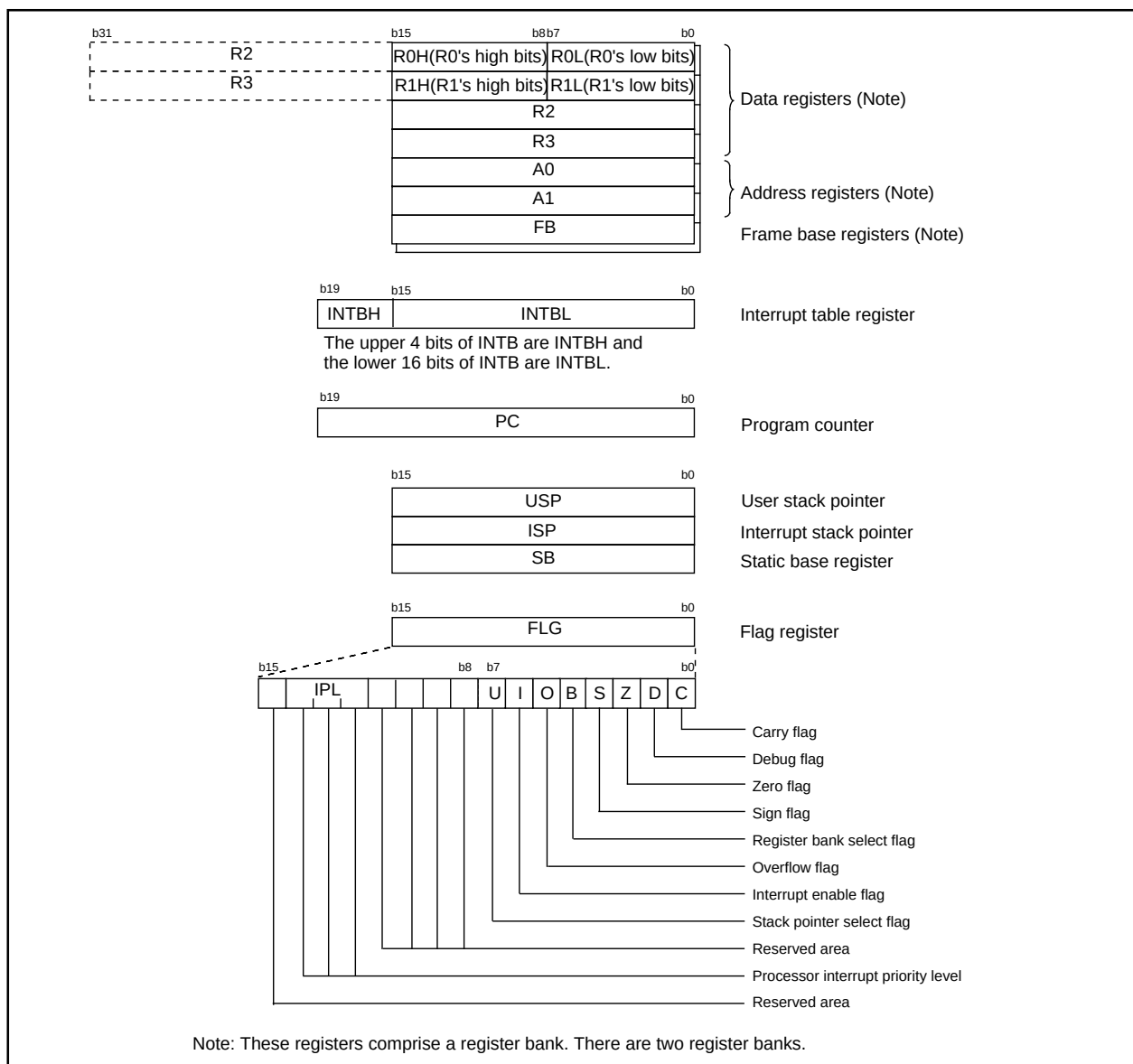


Figure 1.3.1. Central Processing Unit Register

(1) Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

(2) Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

(3) Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

(4) Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

(5) Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

(6) User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

(7) Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

(8) Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

- **Carry Flag (C Flag)**

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

- **Debug Flag (D Flag)**

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

- **Zero Flag (Z Flag)**

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

- **Sign Flag (S Flag)**

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

- **Register Bank Select Flag (B Flag)**

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

- **Overflow Flag (O Flag)**

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

- **Interrupt Enable Flag (I Flag)**

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

- **Stack Pointer Select Flag (U Flag)**

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

- **Processor Interrupt Priority Level (IPL)**

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

- **Reserved Area**

When write to this bit, write "0". When read, its content is indeterminate.

Address	Register	Symbol	After reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0 (Note 2)	PM0	00000000 ₂ (CNV _{ss} pin is "L") 00000011 ₂ (CNV _{ss} pin is "H")
0005 ₁₆	Processor mode register 1	PM1	00001000 ₂
0006 ₁₆	System clock control register 0	CM0	01001000 ₂
0007 ₁₆	System clock control register 1	CM1	00100000 ₂
0008 ₁₆	Chip select control register	CSR	00000001 ₂
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXX00 ₂
000A ₁₆	Protect register	PRCR	XX000000 ₂
000B ₁₆	Data bank register	DBR	0016
000C ₁₆	Oscillation stop detection register (Note 3)	CM2	0000X000 ₂
000D ₁₆			
000E ₁₆	Watchdog timer start register	WDTS	XX16
000F ₁₆	Watchdog timer control register	WDC	00XXXXXX ₂ (Note 4)
0010 ₁₆	Address match interrupt register 0	RMAD0	0016
0011 ₁₆			0016
0012 ₁₆			X016
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	0016
0015 ₁₆			0016
0016 ₁₆			X016
0017 ₁₆			
0018 ₁₆			
0019 ₁₆	Voltage detection register 1 (Note 5)	VCR1	00001000 ₂
001A ₁₆	Voltage detection register 2 (Note 5)	VCR2	0016
001B ₁₆	Chip select expansion control register	CSE	0016
001C ₁₆	PLL control register 0	PLC0	0001X010 ₂
001D ₁₆			
001E ₁₆	Processor mode register 2	PM2	XXX00000 ₂
001F ₁₆	Voltage down detection interrupt register	D4INT	0016
0020 ₁₆	DMA0 source pointer	SAR0	XX16
0021 ₁₆			XX16
0022 ₁₆			XX16
0023 ₁₆			
0024 ₁₆	DMA0 destination pointer	DAR0	XX16
0025 ₁₆			XX16
0026 ₁₆			XX16
0027 ₁₆			
0028 ₁₆	DMA0 transfer counter	TCR0	XX16
0029 ₁₆			XX16
002A ₁₆			
002B ₁₆			
002C ₁₆	DMA0 control register	DM0CON	00000X00 ₂
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆	DMA1 source pointer	SAR1	XX16
0031 ₁₆			XX16
0032 ₁₆			XX16
0033 ₁₆			
0034 ₁₆	DMA1 destination pointer	DAR1	XX16
0035 ₁₆			XX16
0036 ₁₆			XX16
0037 ₁₆			
0038 ₁₆	DMA1 transfer counter	TCR1	XX16
0039 ₁₆			XX16
003A ₁₆			
003B ₁₆			
003C ₁₆	DMA1 control register	DM1CON	00000X00 ₂
003D ₁₆			
003E ₁₆			
003F ₁₆			

Note 1: The blank areas are reserved and cannot be accessed by users.

Note 2: The PM00 and PM01 bits do not change at software reset, watchdog timer reset and oscillation stop detection reset.

Note 3: The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.

Note 4: The WDC5 bit is "0" (cold start) immediately after power-on. It can only be set to "1" in a program. It is set to "0" when the input voltage at the V_{cc1} pin drops to V_{det2} or less while the VC25 bit in the VCR2 register is set to "1" (RAM retention limit detection circuit enable).

Note 5: This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆	INT3 interrupt control register	INT3IC	XX00X0002
0045 ₁₆	Timer B5 interrupt control register	TB5IC	XXXXX0002
0046 ₁₆	Timer B4 interrupt control register, UART1 BUS collision detection interrupt control register	TB4IC, U1BCNIC	XXXXX0002
0047 ₁₆	Timer B3 interrupt control register, UART0 BUS collision detection interrupt control register	TB3IC, U0BCNIC	XXXXX0002
0048 ₁₆	SI/O4 interrupt control register (S4IC), INT5 interrupt control register	S4IC, INT5IC	XX00X0002
0049 ₁₆	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00X0002
004A ₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX0002
004B ₁₆	DMA0 interrupt control register	DM0IC	XXXXX0002
004C ₁₆	DMA1 interrupt control register	DM1IC	XXXXX0002
004D ₁₆	Key input interrupt control register	KUPIC	XXXXX0002
004E ₁₆	A-D conversion interrupt control register	ADIC	XXXXX0002
004F ₁₆	UART2 transmit interrupt control register	S2TIC	XXXXX0002
0050 ₁₆	UART2 receive interrupt control register	S2RIC	XXXXX0002
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055 ₁₆	Timer A0 interrupt control register	TA0IC	XXXXX0002
0056 ₁₆	Timer A1 interrupt control register	TA1IC	XXXXX0002
0057 ₁₆	Timer A2 interrupt control register	TA2IC	XXXXX0002
0058 ₁₆	Timer A3 interrupt control register	TA3IC	XXXXX0002
0059 ₁₆	Timer A4 interrupt control register	TA4IC	XXXXX0002
005A ₁₆	Timer B0 interrupt control register	TB0IC	XXXXX0002
005B ₁₆	Timer B1 interrupt control register	TB1IC	XXXXX0002
005C ₁₆	Timer B2 interrupt control register	TB2IC	XXXXX0002
005D ₁₆	INT0 interrupt control register	INT0IC	XX00X0002
005E ₁₆	INT1 interrupt control register	INT1IC	XX00X0002
005F ₁₆	INT2 interrupt control register	INT2IC	XX00X0002
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆			
0069 ₁₆			
006A ₁₆			
006B ₁₆			
006C ₁₆			
006D ₁₆			
006E ₁₆			
006F ₁₆			
0070 ₁₆			
0071 ₁₆			
0072 ₁₆			
0073 ₁₆			
0074 ₁₆			
0075 ₁₆			
0076 ₁₆			
0077 ₁₆			
0078 ₁₆			
0079 ₁₆			
007A ₁₆			
007B ₁₆			
007C ₁₆			
007D ₁₆			
007E ₁₆			
007F ₁₆			

Note :The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0080 ₁₆			
0081 ₁₆			
0082 ₁₆			
0083 ₁₆			
0084 ₁₆			
0085 ₁₆			
0086 ₁₆			
≈			
01B0 ₁₆			
01B1 ₁₆			
01B2 ₁₆			
01B3 ₁₆			
01B4 ₁₆	Flash identification register (Note 2)	FIDR	XXXXXX002
01B5 ₁₆	Flash memory control register 1 (Note 2)	FMR1	0X00XX0X2
01B6 ₁₆			
01B7 ₁₆	Flash memory control register 0 (Note 2)	FMR0	XX0000012
01B8 ₁₆	Address match interrupt register 2	RMAD2	0016
01B9 ₁₆			0016
01BA ₁₆			X016
01BB ₁₆	Address match interrupt enable register 2	AIER2	XXXXXX002
01BC ₁₆	Address match interrupt register 3	RMAD3	0016
01BD ₁₆			0016
01BE ₁₆			X016
01BF ₁₆			
≈			
0250 ₁₆			
0251 ₁₆			
0252 ₁₆			
0253 ₁₆			
0254 ₁₆			
0255 ₁₆			
0256 ₁₆			
0257 ₁₆			
0258 ₁₆			
0259 ₁₆			
025A ₁₆			
025B ₁₆			
025C ₁₆			
025D ₁₆			
025E ₁₆	Peripheral clock select register	PCLKR	000000112
025F ₁₆			
≈			
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆			
0335 ₁₆			
0336 ₁₆			
0337 ₁₆			
0338 ₁₆			
0339 ₁₆			
033A ₁₆			
033B ₁₆			
033C ₁₆			
033D ₁₆			
033E ₁₆			
033F ₁₆			

Note 1: The blank areas are reserved and cannot be accessed by users.

Note 2: This register is included in the flash memory version.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0340 ₁₆	Timer B3, 4, 5 count start flag	TBSR	000XXXXX2
0341 ₁₆			
0342 ₁₆	Timer A1-1 register	TA11	XX16
0343 ₁₆			XX16
0344 ₁₆	Timer A2-1 register	TA21	XX16
0345 ₁₆			XX16
0346 ₁₆	Timer A4-1 register	TA41	XX16
0347 ₁₆			XX16
0348 ₁₆	Three-phase PWM control register 0	INVC0	0016
0349 ₁₆	Three-phase PWM control register 1	INVC1	0016
034A ₁₆	Three-phase output buffer register 0	IDB0	0016
034B ₁₆	Three-phase output buffer register 1	IDB1	0016
034C ₁₆	Dead time timer	DTT	XX16
034D ₁₆	Timer B2 interrupt occurrence frequency set counter	ICTB2	XX16
034E ₁₆			
034F ₁₆			
0350 ₁₆	Timer B3 register	TB3	XX16
0351 ₁₆			XX16
0352 ₁₆	Timer B4 register	TB4	XX16
0353 ₁₆			XX16
0354 ₁₆	Timer B5 register	TB5	XX16
0355 ₁₆			XX16
0356 ₁₆			
0357 ₁₆			
0358 ₁₆			
0359 ₁₆			
035A ₁₆			
035B ₁₆	Timer B3 mode register	TB3MR	00XX00002
035C ₁₆	Timer B4 mode register	TB4MR	00XX00002
035D ₁₆	Timer B5 mode register	TB5MR	00XX00002
035E ₁₆	Interrupt cause select register 2	IFSR2A	00XXXXXX2
035F ₁₆	Interrupt cause select register	IFSR	0016
0360 ₁₆	SI/O3 transmit/receive register	S3TRR	XX16
0361 ₁₆			
0362 ₁₆	SI/O3 control register	S3C	010000002
0363 ₁₆	SI/O3 bit rate generator	S3BRG	XX16
0364 ₁₆	SI/O4 transmit/receive register	S4TRR	XX16
0365 ₁₆			
0366 ₁₆	SI/O4 control register	S4C	010000002
0367 ₁₆	SI/O4 bit rate generator	S4BRG	XX16
0368 ₁₆			
0369 ₁₆			
036A ₁₆			
036B ₁₆			
036C ₁₆	UART0 special mode register 4	U0SMR4	0016
036D ₁₆	UART0 special mode register 3	U0SMR3	000X0X0X2
036E ₁₆	UART0 special mode register 2	U0SMR2	X00000002
036F ₁₆	UART0 special mode register	U0SMR	X00000002
0370 ₁₆	UART1 special mode register 4	U1SMR4	0016
0371 ₁₆	UART1 special mode register 3	U1SMR3	000X0X0X2
0372 ₁₆	UART1 special mode register 2	U1SMR2	X00000002
0373 ₁₆	UART1 special mode register	U1SMR	X00000002
0374 ₁₆	UART2 special mode register 4	U2SMR4	0016
0375 ₁₆	UART2 special mode register 3	U2SMR3	000X0X0X2
0376 ₁₆	UART2 special mode register 2	U2SMR2	X00000002
0377 ₁₆	UART2 special mode register	U2SMR	X00000002
0378 ₁₆	UART2 transmit/receive mode register	U2MR	0016
0379 ₁₆	UART2 bit rate generator	U2BRG	XX16
037A ₁₆	UART2 transmit buffer register	U2TB	XXXXXXXXX2
037B ₁₆			XXXXXXXXX2
037C ₁₆	UART2 transmit/receive control register 0	U2C0	000010002
037D ₁₆	UART2 transmit/receive control register 1	U2C1	000000102
037E ₁₆	UART2 receive buffer register	U2RB	XXXXXXXXX2
037F ₁₆			XXXXXXXXX2

Note : The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0380 ₁₆	Count start flag	TABSR	0016
0381 ₁₆	Clock prescaler reset flag	CPSRF	0XXXXXXXX2
0382 ₁₆	One-shot start flag	ONSF	0016
0383 ₁₆	Trigger select register	TRGSR	0016
0384 ₁₆	Up-down flag	UDF	0016
0385 ₁₆			
0386 ₁₆ 0387 ₁₆	Timer A0 register	TA0	XX16 XX16
0388 ₁₆ 0389 ₁₆	Timer A1 register	TA1	XX16 XX16
038A ₁₆ 038B ₁₆	Timer A2 register	TA2	XX16 XX16
038C ₁₆ 038D ₁₆	Timer A3 register	TA3	XX16 XX16
038E ₁₆ 038F ₁₆	Timer A4 register	TA4	XX16 XX16
0390 ₁₆ 0391 ₁₆	Timer B0 register	TB0	XX16 XX16
0392 ₁₆ 0393 ₁₆	Timer B1 register	TB1	XX16 XX16
0394 ₁₆ 0395 ₁₆	Timer B2 register	TB2	XX16 XX16
0396 ₁₆	Timer A0 mode register	TA0MR	0016
0397 ₁₆	Timer A1 mode register	TA1MR	0016
0398 ₁₆	Timer A2 mode register	TA2MR	0016
0399 ₁₆	Timer A3 mode register	TA3MR	0016
039A ₁₆	Timer A4 mode register	TA4MR	0016
039B ₁₆	Timer B0 mode register	TB0MR	00XX00002
039C ₁₆	Timer B1 mode register	TB1MR	00XX00002
039D ₁₆	Timer B2 mode register	TB2MR	00XX00002
039E ₁₆ 039F ₁₆	Timer B2 special mode register	TB2SC	XXXXXX002
03A0 ₁₆	UART0 transmit/receive mode register	U0MR	0016
03A1 ₁₆	UART0 bit rate generator	U0BRG	XX16
03A2 ₁₆ 03A3 ₁₆	UART0 transmit buffer register	U0TB	XXXXXXXXX2 XXXXXXXXX2
03A4 ₁₆	UART0 transmit/receive control register 0	U0C0	000010002
03A5 ₁₆	UART0 transmit/receive control register 1	U0C1	000000102
03A6 ₁₆ 03A7 ₁₆	UART0 receive buffer register	U0RB	XXXXXXXXX2 XXXXXXXXX2
03A8 ₁₆ 03A9 ₁₆	UART1 transmit/receive mode register	U1MR	0016
03AA ₁₆ 03AB ₁₆	UART1 bit rate generator	U1BRG	XX16
03AC ₁₆ 03AD ₁₆	UART1 transmit buffer register	U1TB	XXXXXXXXX2 XXXXXXXXX2
03AE ₁₆ 03AF ₁₆	UART1 transmit/receive control register 0	U1C0	000010002
03B0 ₁₆	UART1 transmit/receive control register 1	U1C1	000000102
03B1 ₁₆ 03B2 ₁₆ 03B3 ₁₆ 03B4 ₁₆ 03B5 ₁₆ 03B6 ₁₆ 03B7 ₁₆	UART1 receive buffer register	U1RB	XXXXXXXXX2 XXXXXXXXX2
03B8 ₁₆ 03B9 ₁₆	UART transmit/receive control register 2	UCON	X00000002
03BA ₁₆ 03BB ₁₆			
03BC ₁₆ 03BD ₁₆	DMA0 request cause select register	DM0SL	0016
03BE ₁₆ 03BF ₁₆	DMA1 request cause select register	DM1SL	0016
	CRC data register	CRCD	XX16 XX16
	CRC input register	CRCIN	XX16

Note : The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
03C0 ₁₆ 03C1 ₁₆	A-D register 0	AD0	XXXXXXXX2 XXXXXXXX2
03C2 ₁₆ 03C3 ₁₆	A-D register 1	AD1	XXXXXXXX2 XXXXXXXX2
03C4 ₁₆ 03C5 ₁₆	A-D register 2	AD2	XXXXXXXX2 XXXXXXXX2
03C6 ₁₆ 03C7 ₁₆	A-D register 3	AD3	XXXXXXXX2 XXXXXXXX2
03C8 ₁₆ 03C9 ₁₆	A-D register 4	AD4	XXXXXXXX2 XXXXXXXX2
03CA ₁₆ 03CB ₁₆	A-D register 5	AD5	XXXXXXXX2 XXXXXXXX2
03CC ₁₆ 03CD ₁₆	A-D register 6	AD6	XXXXXXXX2 XXXXXXXX2
03CE ₁₆ 03CF ₁₆	A-D register 7	AD7	XXXXXXXX2 XXXXXXXX2
03D0 ₁₆			
03D1 ₁₆			
03D2 ₁₆			
03D3 ₁₆			
03D4 ₁₆	A-D control register 2	ADCON2	0016
03D5 ₁₆			
03D6 ₁₆	A-D control register 0	ADCON0	00000XXX2
03D7 ₁₆	A-D control register 1	ADCON1	0016
03D8 ₁₆	D-A register 0	DA0	XX16
03D9 ₁₆			
03DA ₁₆	D-A register 1	DA1	XX16
03DB ₁₆			
03DC ₁₆	D-A control register	DACON	0016
03DD ₁₆			
03DE ₁₆	Port P14 control register	PC14	XX00XXXX2
03DF ₁₆	Pull-up control register 3	PUR3	0016
03E0 ₁₆	Port P0 register	P0	XX16
03E1 ₁₆	Port P1 register	P1	XX16
03E2 ₁₆	Port P0 direction register	PD0	0016
03E3 ₁₆	Port P1 direction register	PD1	0016
03E4 ₁₆	Port P2 register	P2	XX16
03E5 ₁₆	Port P3 register	P3	XX16
03E6 ₁₆	Port P2 direction register	PD2	0016
03E7 ₁₆	Port P3 direction register	PD3	0016
03E8 ₁₆	Port P4 register	P4	XX16
03E9 ₁₆	Port P5 register	P5	XX16
03EA ₁₆	Port P4 direction register	PD4	0016
03EB ₁₆	Port P5 direction register	PD5	0016
03EC ₁₆	Port P6 register	P6	XX16
03ED ₁₆	Port P7 register	P7	XX16
03EE ₁₆	Port P6 direction register	PD6	0016
03EF ₁₆	Port P7 direction register	PD7	0016
03F0 ₁₆	Port P8 register	P8	XX16
03F1 ₁₆	Port P9 register	P9	XX16
03F2 ₁₆	Port P8 direction register	PD8	00X000002
03F3 ₁₆	Port P9 direction register	PD9	0016
03F4 ₁₆	Port P10 register	P10	XX16
03F5 ₁₆	Port P11 register	P11	XX16
03F6 ₁₆	Port P10 direction register	PD10	0016
03F7 ₁₆	Port P11 direction register	PD11	0016
03F8 ₁₆	Port P12 register	P12	XX16
03F9 ₁₆	Port P13 register	P13	XX16
03FA ₁₆	Port P12 direction register	PD12	0016
03FB ₁₆	Port P13 direction register	PD13	0016
03FC ₁₆	Pull-up control register 0	PUR0	0016
03FD ₁₆	Pull-up control register 1	PUR1	00000000 ₂ 00000010 ₂ (Note 2)
03FE ₁₆	Pull-up control register 2	PUR2	0016
03FF ₁₆	Port control register	PCR	0016

Note 1: The blank areas are reserved and cannot be accessed by users.

Note 2: At hardware reset 1 or hardware reset 2, the register is as follows:

- "00000000₂" where "L" is inputted to the CNV_{ss} pin
- "00000010₂" where "H" is inputted to the CNV_{ss} pin

At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:

- "00000000₂" where the PM01 to PM00 bits in the PM0 register are "00₂" (single-chip mode)
- "00000010₂" where the PM01 to PM00 bits in the PM0 register are "01₂" (memory expansion mode) or "11₂" (microprocessor mode)

X : Nothing is mapped to this bit

Electrical Characteristics

Table 1.5.1. Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated value	Unit
Vcc1, Vcc2	Supply voltage		Vcc1=AVcc	-0.3 to 6.5	V
Vcc2	Supply voltage		Vcc2	-0.3 to Vcc1+0.1	V
AVcc	Analog supply voltage		Vcc1=AVcc	-0.3 to 6.5	V
Vi	Input voltage	RESET, CNVss, BYTE, P60 to P67, P72 to P77, P80 to P87, P90 to P97, P100 to P107, P110 to P117, P140, P141, VREF, XIN		-0.3 to Vcc1+0.3	V
		P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P120 to P127, P130 to P137		-0.3 to Vcc2+0.3	V
		P70, P71		-0.3 to 6.5	V
Vo	Output voltage	P60 to P67, P72 to P77, P80 to P84, P86, P87, P90 to P97, P100 to P107, P110 to P117, P140, P141, XOUT		-0.3 to Vcc1+0.3	V
		P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P120 to P127, P130 to P137		-0.3 to Vcc2+0.3	V
		P70, P71		-0.3 to 6.5	V
Pd	Power dissipation		Topr=25 °C	300	mW
Topr	Operating ambient temperature			-20 to 85 / -40 to 85	°C
Tstg	Storage temperature			-65 to 150	°C

Table 1.5.2. Recommended Operating Conditions (Note 1)

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
V _{CC1} , V _{CC2}	Supply voltage(V _{CC1} ≥V _{CC2})	2.7	5.0	5.5	V
AV _{CC}	Analog supply voltage		V _{CC1}		V
V _{SS}	Supply voltage		0		V
AV _{SS}	Analog supply voltage		0		V
V _{IH}	HIGH input voltage	P3 ₁ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇	0.8V _{CC2}	V _{CC2}	V
		P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ (during single-chip mode)	0.8V _{CC2}	V _{CC2}	V
		P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ (data input during memory expansion and microprocessor modes)	0.5V _{CC2}	V _{CC2}	V
		P6 ₀ to P6 ₇ , P7 ₂ to P7 ₇ , P8 ₀ to P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P14 ₀ , P14 ₁ , X _{IN} , RESET, CNV _{SS} , BYTE	0.8V _{CC1}	V _{CC1}	V
		P7 ₀ , P7 ₁	0.8V _{CC1}	6.5	V
V _{IL}	LOW input voltage	P3 ₁ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇	0	0.2V _{CC2}	V
		P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ (during single-chip mode)	0	0.2V _{CC2}	V
		P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ (data input during memory expansion and microprocessor modes)	0	0.16V _{CC2}	V
		P6 ₀ to P6 ₇ , P7 ₀ to P7 ₇ , P8 ₀ to P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P14 ₀ , P14 ₁ , X _{IN} , RESET, CNV _{SS} , BYTE	0	0.2V _{CC1}	V
I _{OH} (peak)	HIGH peak output current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P6 ₀ to P6 ₇ , P7 ₂ to P7 ₇ , P8 ₀ to P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇ , P14 ₀ , P14 ₁		-10.0	mA
I _{OH} (avg)	HIGH average output current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P6 ₀ to P6 ₇ , P7 ₂ to P7 ₇ , P8 ₀ to P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇ , P14 ₀ , P14 ₁		-5.0	mA
I _{OL} (peak)	LOW peak output current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P6 ₀ to P6 ₇ , P7 ₀ to P7 ₇ , P8 ₀ to P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇ , P14 ₀ , P14 ₁		10.0	mA
I _{OL} (avg)	LOW average output current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P6 ₀ to P6 ₇ , P7 ₀ to P7 ₇ , P8 ₀ to P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇ , P14 ₀ , P14 ₁		5.0	mA
f (X _{IN})	Main clock input oscillation frequency (Note 4)	V _{CC1} =3.0 to 5.5V	0	16	MHz
		V _{CC1} =2.7 to 3.0V	0	20 X V _{CC1} -44	MHz
f (X _{CIN})	Sub-clock oscillation frequency		32.768	50	kHz
f (Ring)	Ring oscillation frequency		1		MHz
f (PLL)	PLL clock oscillation frequency (Note 4)	V _{CC1} =3.0 to 5.5V	10	24	MHz
		V _{CC1} =2.7 to 3.0V	10	46.67 X V _{CC1} -116	MHz
f (BCLK)	CPU operation clock		0	24	MHz
T _{su} (PLL)	PLL frequency synthesizer stabilization wait time	V _{CC1} =5.0V		20	ms
		V _{CC1} =3.0V		50	ms

Note 1: Referenced to V_{CC} = V_{CC1} = V_{CC2} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C unless otherwise specified.

Note 2: The mean output current is the mean value within 100ms.

Note 3: The total I_{OL} (peak) for ports P0, P1, P2, P8₆, P8₇, P9, P10, P11, P14₀ and P14₁ must be 80mA max. The total I_{OL} (peak) for ports P3, P4, P5, P6, P7, P8₀ to P8₄, P12, and P13 must be 80mA max. The total I_{OH} (peak) for ports P0, P1, and P2 must be -40mA max. The total I_{OH} (peak) for ports P3, P4, P5, P12, and P13 must be -40mA max. The total I_{OH} (peak) for ports P6, P7, and P8₀ to P8₄ must be -40mA max. The total I_{OH} (peak) for ports P8₆, P8₇, P9, P10, P11, P14₀, and P14₁ must be -40mA max.

Note 4: Relationship between main clock oscillation frequency, PLL clock oscillation frequency and supply voltage.

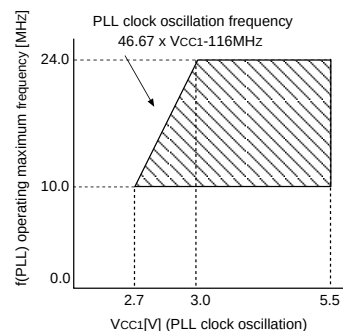
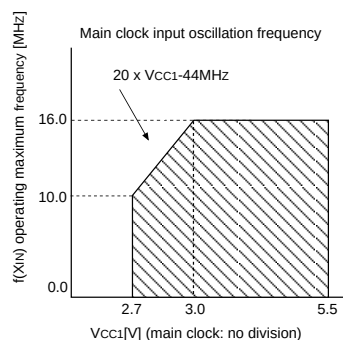


Table 1.5.3. A-D Conversion Characteristics (Note 1)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		$V_{REF} = V_{CC1}$			10	Bits
INL	Integral non-linearity error	10 bit	$V_{REF} = V_{CC1} = 5V$	AN0 to AN7 input		± 3	LSB
				ANEX0, ANEX1 input External operation amp connection mode AN00 to AN07 input AN20 to AN27 input		± 7	LSB
			$V_{REF} = V_{CC1} = 3.3V$	AN0 to AN7 input		± 5	LSB
				ANEX0, ANEX1 input External operation amp connection mode AN00 to AN07 input AN20 to AN27 input		± 7	LSB
		8 bit	$V_{REF} = V_{CC1} = 3.3V$			± 2	LSB
–	Absolute accuracy	10 bit	$V_{REF} = V_{CC1} = 5V$	AN0 to AN7 input		± 3	LSB
				ANEX0, ANEX1 input External operation amp connection mode AN00 to AN07 input AN20 to AN27 input		± 7	LSB
			$V_{REF} = V_{CC1} = 3.3V$	AN0 to AN7 input		± 5	LSB
				ANEX0, ANEX1 input External operation amp connection mode AN00 to AN07 input AN20 to AN27 input		± 7	LSB
		8 bit	$V_{REF} = V_{CC1} = 3.3V$			± 2	LSB
DNL	Differential non-linearity error					± 1	LSB
–	Offset error					± 3	LSB
–	Gain error					± 3	LSB
R_{LADDER}	Ladder resistance		$V_{REF} = V_{CC1}$	10		40	k Ω
t_{CONV}	Conversion time(10bit), Sample & hold function available		$V_{REF} = V_{CC1} = 5V, \emptyset_{AD} = 10MHz$	3.3			μs
t_{CONV}	Conversion time(8bit), Sample & hold function available		$V_{REF} = V_{CC1} = 5V, \emptyset_{AD} = 10MHz$	2.8			μs
t_{SAMP}	Sampling time			0.3			μs
V_{REF}	Reference voltage			2.0		V_{CC1}	V
V_{IA}	Analog input voltage			0		V_{REF}	V

Note 1: Referenced to $V_{CC1} = AV_{CC} = V_{REF} = 3.3$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified.

Note 2: If $V_{CC1} > V_{CC2}$, do not use AN00 to AN07 and AN20 to AN27 as analog input pins.

Note 3: AD operation clock frequency ($\emptyset_{AD}$ frequency) must be 10 MHz or less. And divide the f_{AD} if V_{CC1} is less than 4.2V, and make $\emptyset_{AD}$ frequency equal to or lower than $f_{AD}/2$.

Note 4: A case without sample & hold function turn $\emptyset_{AD}$ frequency into 250 kHz or more in addition to a limit of Note 3.
A case with sample & hold function turn $\emptyset_{AD}$ frequency into 1MHz or more in addition to a limit of Note 3.

Table 1.5.4. D-A Conversion Characteristics (Note 1)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
t_{su}	Setup time				3	μs
R_O	Output resistance		4	10	20	k Ω
I_{VREF}	Reference power supply input current	(Note 2)			1.5	mA

Note 1: Referenced to $V_{CC1} = V_{REF} = 3.3$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified.

Note 2: This applies when using one D-A converter, with the D-A register for the unused D-A converter set to "0016". The A-D converter's ladder resistance is not included. Also, when D-A register contents are not "0016", the current I_{VREF} always flows even though V_{ref} may have been set to be unconnected by the A-D control register.

Table 1.5.5. Flash Memory Version Electrical Characteristics (Note 1) 100 times guarantee article

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Word program time			30	200	μs
–	Block erase time			1	4	s
–	Erase all unlocked blocks time			1 X n	4 X n	s
–	Lock bit program time			30	200	μs
t _{ps}	Flash memory circuit stabilization wait time				15	μs

Note 1: Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at T_{opr} = 0 to 60 °C unless otherwise specified.

Note 2: n denotes the number of block erases.

Table 1.5.6. Flash Memory Version Electrical Characteristics (Note 1) 10,000 times guarantee article (block1 and block A(Note 3))

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Word program time			30	T.B.D	μs
–	Block erase time			1	T.B.D	s
–	Erase all unlocked blocks time			1 X n	T.B.D	s
–	Lock bit program time			30	T.B.D	μs
t _{ps}	Flash memory circuit stabilization wait time				15	μs

Note 1: Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at T_{opr} = 0 to 60 °C unless otherwise specified.

Note 2: n denotes the number of block erases.

Note 3: Shown here are the rated values for block 1 and block A when they have been programmed and erased more than 1,000 times. The rated values up to 1,000 times of programming and erasure are the same for all blocks as those products that are guaranteed of 100 times of programming and erasure.

Table 1.5.7. Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at T_{opr} = 0 to 60°C)

Flash program, erase voltage	Flash read operation voltage
V _{CC1} = 3.3 V ± 0.3 V or 5.0 V ± 0.5 V	V _{CC1} =2.7 to 5.5 V

Table 1.5.8. Low Voltage Detection Circuit Electrical Characteristics (Note 1)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Voltage down detection voltage (Note 1)	V _{CC1} =0.8 to 5.5V	3.3	3.8	4.4	V
Vdet3	Reset level detection voltage (Notes 1, 2)		2.2	2.8	3.6	V
Vdet3s	Low voltage reset retention voltage		0.8			V
Vdet3r	Low voltage reset release voltage (Note 3)		2.2	2.9	4.0	V
Vdet2	RAM retention limit detection voltage (Note 1)		1.4	2.0	2.7	V

Note 1: Vdet4 > Vdet3 > Vdet2

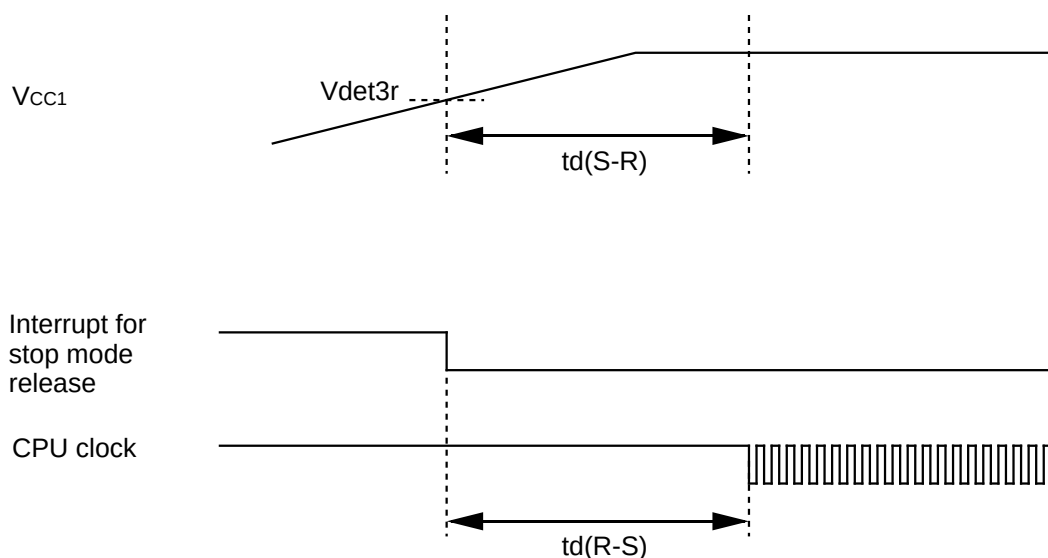
Note 2: Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the operation at f(BCLK) ≤ 10MHz is guaranteed.

Note 3: Vdet3r > Vdet3 is not guaranteed.

Table 1.5.9. Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on	V _{CC1} =2.7 to 5.5V			2	ms
td(R-S)	STOP release time				150	μs
td(W-S)	Low power dissipation mode wait mode release time				150	μs
td(M-L)	Time for internal power supply stabilization when main clock oscillation starts				50	μs
td(S-R)	Hardware reset 2 release wait time	V _{CC1} =Vdet3r to 5.5V		6 (Note)	20	ms
td(E-A)	Low voltage detection circuit operation start time	V _{CC1} =2.7 to 5.5V			20	μs

Note : When V_{CC1} = 5V



$$V_{CC1} = V_{CC2} = 5V$$

Table 1.5.10. Electrical Characteristics (Note 1)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	HIGH output voltage	P6 ₀ to P6 ₇ , P7 ₂ to P7 ₇ , P8 ₀ to P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P14 ₀ , P14 ₁	I _{OH} =-5mA	V _{CC1} -2.0		V _{CC1}	V
		P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇	I _{OH} =-5mA(Note 2)	V _{CC2} -2.0		V _{CC2}	
V _{OH}	HIGH output voltage	P6 ₀ to P6 ₇ , P7 ₂ to P7 ₇ , P8 ₀ to P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P14 ₀ , P14 ₁	I _{OH} =-200μA	V _{CC1} -0.3		V _{CC1}	V
		P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇	I _{OH} =-200μA(Note 2)	V _{CC2} -0.3		V _{CC2}	
V _{OH}	HIGH output voltage	X _{OUT}	HIGHPOWER	I _{OH} =-1mA	V _{CC1} -2.0	V _{CC1}	V
			LOWPOWER	I _{OH} =-0.5mA	V _{CC1} -2.0	V _{CC1}	
	HIGH output voltage	X _{COUT}	HIGHPOWER	With no load applied		2.5	V
			LOWPOWER	With no load applied		1.6	
V _{OL}	LOW output voltage	P6 ₀ to P6 ₇ , P7 ₀ to P7 ₇ , P8 ₀ to P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P14 ₀ , P14 ₁	I _{OL} =5mA			2.0	V
		P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇	I _{OL} =5mA(Note 2)			2.0	
V _{OL}	LOW output voltage	P6 ₀ to P6 ₇ , P7 ₀ to P7 ₇ , P8 ₀ to P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P14 ₀ , P14 ₁	I _{OL} =200μA			0.45	V
		P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇	I _{OL} =200μA(Note 2)			0.45	
V _{OL}	LOW output voltage	X _{OUT}	HIGHPOWER	I _{OL} =1mA		2.0	V
			LOWPOWER	I _{OL} =0.5mA		2.0	
	LOW output voltage	X _{COUT}	HIGHPOWER	With no load applied		0	V
			LOWPOWER	With no load applied		0	
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0 _{IN} to TA4 _{IN} , TB0 _{IN} to TB5 _{IN} , INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, SCL, SDA, CLK0 to CLK4, TA2 _{OUT} to TA4 _{OUT} , K10 to K13, RxD0 to RxD2, SIn3, SIn4		0.2		1.0	V
V _{T+} -V _{T-}	Hysteresis	RESET		0.2		2.2	V
I _{IH}	HIGH input current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P6 ₀ to P6 ₇ , P7 ₀ to P7 ₇ , P8 ₀ to P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇ , P14 ₀ , P14 ₁ , X _{IN} , RESET, CNVss, BYTE	V _I =5V			5.0	μA
I _{IL}	LOW input current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P6 ₀ to P6 ₇ , P7 ₀ to P7 ₇ , P8 ₀ to P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇ , P14 ₀ , P14 ₁ , X _{IN} , RESET, CNVss, BYTE	V _I =0V			-5.0	μA
R _{PULLUP}	Pull-up resistance	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P6 ₀ to P6 ₇ , P7 ₂ to P7 ₇ , P8 ₀ to P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇ , P14 ₀ , P14 ₁	V _I =0V	30	50	170	kΩ
R _{XIN}	Feedback resistance	X _{IN}			1.5		MΩ
R _{XCIN}	Feedback resistance	X _{CIN}			15		MΩ
V _{RAM}	RAM retention voltage		At stop mode	2.0			V

Note 1: Referenced to V_{CC}=V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(BCLK)=24MHz unless otherwise specified.

Note 2: Where the product is used at V_{CC1} = 5 V and V_{CC2} = 3 V, refer to the 3 V version value for the pin specified value on the V_{CC2} port side.

$$V_{CC1} = V_{CC2} = 5V$$

Table 1.5.11. Electrical Characteristics (2) (Note 1)

Symbol	Parameter		Measuring condition		Standard			Unit	
					Min.	Typ.	Max.		
Icc	Power supply current (VCC1=4.0 to 5.5V)	In single-chip mode, the output pins are open and other pins are Vss	Mask ROM	f(BCLK)=24MHz, No division, PLL operation		14	20	mA	
				No division, Ring oscillation		1		mA	
			Flash memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA	
				No division, Ring oscillation		1.8		mA	
			Flash memory Program	f(BCLK)=10MHz, VCC1=5.0V		15		mA	
			Flash memory Erase	f(BCLK)=10MHz, VCC1=5.0V		25		mA	
			Mask ROM	f(Xcin)=32kHz, Low power dissipation mode, ROM(Note 3)		25		μA	
			Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM(Note 3)		25		μA	
				f(BCLK)=32kHz Low power dissipation mode, Flash memory(Note 3)		420		μA	
				Ring oscillation, Wait mode		50		μA	
				Mask ROM Flash memory	f(BCLK)=32kHz, Wait mode (Note 2), Oscillation capacity High		7.5		μA
			f(BCLK)=32kHz, Wait mode(Note 2), Oscillation capacity Low			2.0		μA	
			Stop mode, T _{opr} =25°C			0.8	3.0	μA	
Idet4	Voltage down detection dissipation current (Note 4)					0.7	4	μA	
Idet3	Reset area detection dissipation current (Note 4)					1.2	8	μA	
Idet2	RAM retention limit detection dissipation current (Note 4)					1.1	6	μA	

Note 1: Referenced to Vcc=Vcc1=Vcc2=4.2 to 5.5V, Vss=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=24MHz unless otherwise specified.

Note 2: With one timer operated using fc32.

Note 3: This indicates the memory in which the program to be executed exists.

Note 4: I_{det} is dissipation current when the following bit is set to "1" (detection circuit enabled).

Idet4: VC27 bit of VCR2 register

Idet3: VC26 bit of VCR2 register

Idet2: VC25 bit of VCR2 register

$$V_{CC1} = V_{CC2} = 5V$$

Timing Requirements

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.12. External Clock Input (X_{IN} input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c	External clock input cycle time	62.5		ns
t _{w(H)}	External clock input HIGH pulse width	25		ns
t _{w(L)}	External clock input LOW pulse width	25		ns
t _r	External clock rise time		15	ns
t _f	External clock fall time		15	ns

Table 1.5.13. Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{ac1} (RD-DB)	Data input access time (for setting with no wait)		(Note 1)	ns
t _{ac2} (RD-DB)	Data input access time (for setting with wait)		(Note 2)	ns
t _{ac3} (RD-DB)	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
t _{su} (DB-RD)	Data input setup time	40		ns
t _{su} (RDY-BCLK)	RDY input setup time	30		ns
t _{su} (HOLD-BCLK)	HOLD input setup time	40		ns
t _h (RD-DB)	Data input hold time	0		ns
t _h (BCLK-RDY)	RDY input hold time	0		ns
t _h (BCLK-HOLD)	HOLD input hold time	0		ns
t _d (BCLK-HLDA)	HLDA output delay time		40	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 45 \quad [\text{ns}]$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 45 \quad [\text{ns}] \quad \text{n is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.}$$

Note 3: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 45 \quad [\text{ns}] \quad \text{n is "2" for 2-wait setting, "3" for 3-wait setting.}$$

$$V_{CC1} = V_{CC2} = 5V$$

Timing Requirements

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.14. Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TA _{IIN} input cycle time	100		ns
t _w (TAH)	TA _{IIN} input HIGH pulse width	40		ns
t _w (TAL)	TA _{IIN} input LOW pulse width	40		ns

Table 1.5.15. Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TA _{IIN} input cycle time	400		ns
t _w (TAH)	TA _{IIN} input HIGH pulse width	200		ns
t _w (TAL)	TA _{IIN} input LOW pulse width	200		ns

Table 1.5.16. Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TA _{IIN} input cycle time	200		ns
t _w (TAH)	TA _{IIN} input HIGH pulse width	100		ns
t _w (TAL)	TA _{IIN} input LOW pulse width	100		ns

Table 1.5.17. Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _w (TAH)	TA _{IIN} input HIGH pulse width	100		ns
t _w (TAL)	TA _{IIN} input LOW pulse width	100		ns

Table 1.5.18. Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (UP)	TA _{IOUT} input cycle time	2000		ns
t _w (UPH)	TA _{IOUT} input HIGH pulse width	1000		ns
t _w (UPL)	TA _{IOUT} input LOW pulse width	1000		ns
t _{su} (UP-TIN)	TA _{IOUT} input setup time	400		ns
t _h (TIN-UP)	TA _{IOUT} input hold time	400		ns

Table 1.5.19. Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TA _{IIN} input cycle time	800		ns
t _{su} (TA _{IIN} -TA _{IOUT})	TA _{IOUT} input setup time	200		ns
t _{su} (TA _{IOUT} -TA _{IIN})	TA _{IIN} input setup time	200		ns

$$V_{CC1} = V_{CC2} = 5V$$

Timing Requirements(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = – 20 to 85°C / – 40 to 85°C unless otherwise specified)**Table 1.5.20. Timer B Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TB _{IN} input cycle time (counted on one edge)	100		ns
t _w (TBH)	TB _{IN} input HIGH pulse width (counted on one edge)	40		ns
t _w (TBL)	TB _{IN} input LOW pulse width (counted on one edge)	40		ns
t _c (TB)	TB _{IN} input cycle time (counted on both edges)	200		ns
t _w (TBH)	TB _{IN} input HIGH pulse width (counted on both edges)	80		ns
t _w (TBL)	TB _{IN} input LOW pulse width (counted on both edges)	80		ns

Table 1.5.21. Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TB _{IN} input cycle time	400		ns
t _w (TBH)	TB _{IN} input HIGH pulse width	200		ns
t _w (TBL)	TB _{IN} input LOW pulse width	200		ns

Table 1.5.22. Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TB _{IN} input cycle time	400		ns
t _w (TBH)	TB _{IN} input HIGH pulse width	200		ns
t _w (TBL)	TB _{IN} input LOW pulse width	200		ns

Table 1.5.23. A-D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (AD)	AD _{TRG} input cycle time (trigger able minimum)	1000		ns
t _w (ADL)	AD _{TRG} input LOW pulse width	125		ns

Table 1.5.24. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (CK)	CLK _i input cycle time	200		ns
t _w (CKH)	CLK _i input HIGH pulse width	100		ns
t _w (CKL)	CLK _i input LOW pulse width	100		ns
t _d (C-Q)	TxD _i output delay time		80	ns
t _h (C-Q)	TxD _i hold time	0		ns
t _{su} (D-C)	RxD _i input setup time	30		ns
t _h (C-D)	RxD _i input hold time	90		ns

Table 1.5.25. External Interrupt INT_i Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _w (INH)	INT _i input HIGH pulse width	250		ns
t _w (INL)	INT _i input LOW pulse width	250		ns

$$V_{CC1} = V_{CC2} = 5V$$

Switching Characteristics

(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.26. Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address output delay time	Figure 1.5.1		25	ns
t _h (BCLK-AD)	Address output hold time (refers to BCLK)		4		ns
t _h (RD-AD)	Address output hold time (refers to RD)		0		ns
t _h (WR-AD)	Address output hold time (refers to WR)		(Note 2)		ns
t _d (BCLK-CS)	Chip select output delay time			25	ns
t _h (BCLK-CS)	Chip select output hold time (refers to BCLK)		4		ns
t _d (BCLK-ALE)	ALE signal output delay time			25	ns
t _h (BCLK-ALE)	ALE signal output hold time		–4		ns
t _d (BCLK-RD)	RD signal output delay time			25	ns
t _h (BCLK-RD)	RD signal output hold time		0		ns
t _d (BCLK-WR)	WR signal output delay time			25	ns
t _h (BCLK-WR)	WR signal output hold time		0		ns
t _d (BCLK-DB)	Data output delay time (refers to BCLK)			40	ns
t _h (BCLK-DB)	Data output hold time (refers to BCLK)(Note 3)		4		ns
t _d (DB-WR)	Data output delay time (refers to WR)		(Note 1)		ns
t _h (WR-DB)	Data output hold time (refers to WR)(Note 3)		(Note 2)		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40 \quad [\text{ns}] \quad f(\text{BCLK}) \text{ is } 12.5\text{MHz or less.}$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \quad [\text{ns}]$$

Note 3: This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$$

by a circuit of the right figure.

For example, when V_{OL} = 0.2V_{CC2}, C = 30pF, R = 1kΩ, hold time of output “L” level is

$$t = -30\text{pF} \times 1\text{k}\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2}) \\ = 6.7\text{ns.}$$

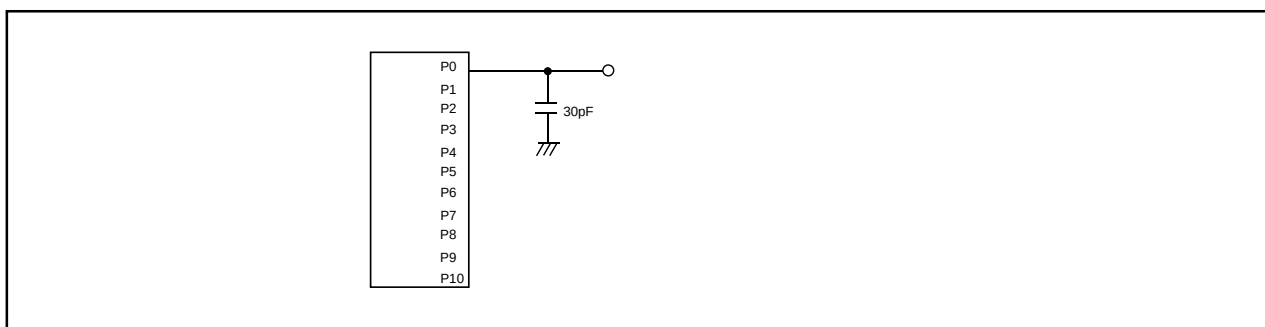
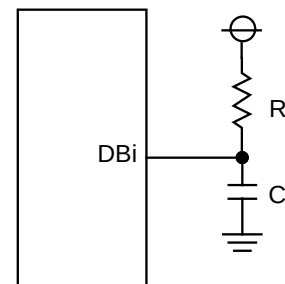


Figure 1.5.1. Ports P0 to P10 Measurement Circuit

$$V_{CC1} = V_{CC2} = 5V$$

Switching Characteristics

(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.27. Memory Expansion and Microprocessor Modes
(for 1- to 3-wait setting and external area access)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address output delay time	Figure 1.5.1		25	ns
t _h (BCLK-AD)	Address output hold time (refers to BCLK)		4		ns
t _h (RD-AD)	Address output hold time (refers to RD)		0		ns
t _h (WR-AD)	Address output hold time (refers to WR)		(Note 2)		ns
t _d (BCLK-CS)	Chip select output delay time			25	ns
t _h (BCLK-CS)	Chip select output hold time (refers to BCLK)		4		ns
t _d (BCLK-ALE)	ALE signal output delay time			25	ns
t _h (BCLK-ALE)	ALE signal output hold time		–4		ns
t _d (BCLK-RD)	RD signal output delay time			25	ns
t _h (BCLK-RD)	RD signal output hold time		0		ns
t _d (BCLK-WR)	WR signal output delay time			25	ns
t _h (BCLK-WR)	WR signal output hold time		0		ns
t _d (BCLK-DB)	Data output delay time (refers to BCLK)			40	ns
t _h (BCLK-DB)	Data output hold time (refers to BCLK)(Note 3)		4		ns
t _d (DB-WR)	Data output delay time (refers to WR)		(Note 1)		ns
t _h (WR-DB)	Data output hold time (refers to WR)(Note 3)		(Note 2)		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 40 \quad [\text{ns}]$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
When n=1, f(BCLK) is 12.5MHz or less.

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \quad [\text{ns}]$$

Note 3: This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

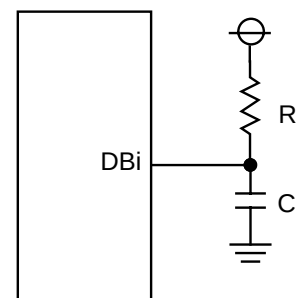
Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$$

by a circuit of the right figure.

For example, when V_{OL} = 0.2V_{CC2}, C = 30pF, R = 1kΩ, hold time of output “L” level is

$$t = -30\text{pF} \times 1\text{k}\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2}) \\ = 6.7\text{ns}.$$



$$V_{CC1} = V_{CC2} = 5V$$

Switching Characteristics

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.28. Memory Expansion and Microprocessor Modes
(for 2- to 3-wait setting, external area access and multiplex bus selection)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address output delay time	Figure 1.5.1		25	ns
t _h (BCLK-AD)	Address output hold time (refers to BCLK)		4		ns
t _h (RD-AD)	Address output hold time (refers to RD)		(Note 1)		ns
t _h (WR-AD)	Address output hold time (refers to WR)		(Note 1)		ns
t _d (BCLK-CS)	Chip select output delay time			25	ns
t _h (BCLK-CS)	Chip select output hold time (refers to BCLK)		4		ns
t _h (RD-CS)	Chip select output hold time (refers to RD)		(Note 1)		ns
t _h (WR-CS)	Chip select output hold time (refers to WR)		(Note 1)		ns
t _d (BCLK-RD)	RD signal output delay time			25	ns
t _h (BCLK-RD)	RD signal output hold time		0		ns
t _d (BCLK-WR)	WR signal output delay time			25	ns
t _h (BCLK-WR)	WR signal output hold time		0		ns
t _d (BCLK-DB)	Data output delay time (refers to BCLK)			40	ns
t _h (BCLK-DB)	Data output hold time (refers to BCLK)		4		ns
t _d (DB-WR)	Data output delay time (refers to WR)		(Note 2)		ns
t _h (WR-DB)	Data output hold time (refers to WR)		(Note 1)		ns
t _d (BCLK-ALE)	ALE signal output delay time (refers to BCLK)			25	ns
t _h (BCLK-ALE)	ALE signal output hold time (refers to BCLK)		– 4		ns
t _d (AD-ALE)	ALE signal output delay time (refers to Address)		(Note 3)		ns
t _h (ALE-AD)	ALE signal output hold time (refers to Address)		(Note 4)		ns
t _d (AD-RD)	RD signal output delay from the end of Address		0		ns
t _d (AD-WR)	WR signal output delay from the end of Address		0		ns
t _d (RD-AD)	Address output floating start time			8	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \quad [\text{ns}]$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 40 \quad [\text{ns}] \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

Note 3: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 25 \quad [\text{ns}]$$

Note 4: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 15 \quad [\text{ns}]$$

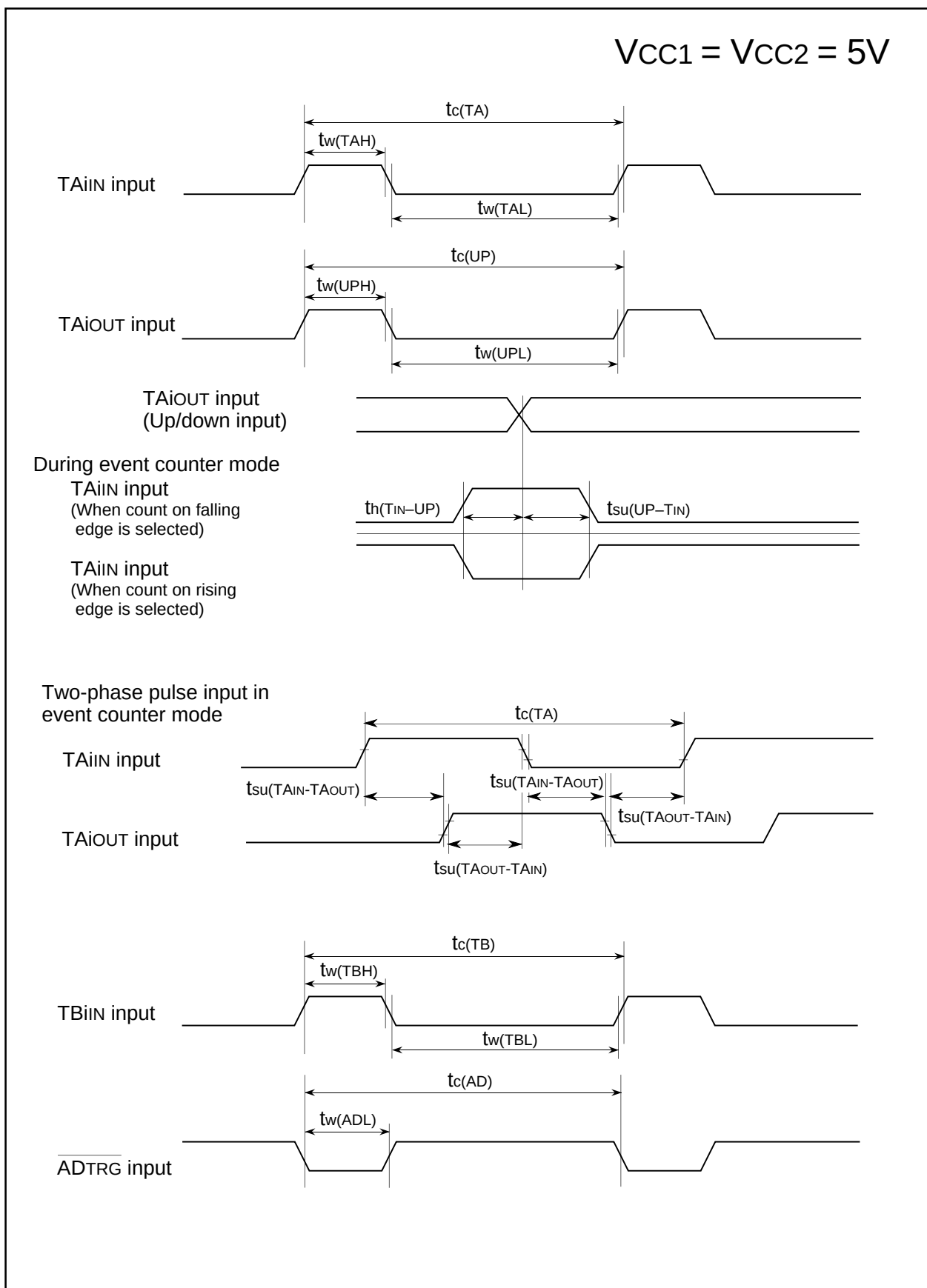
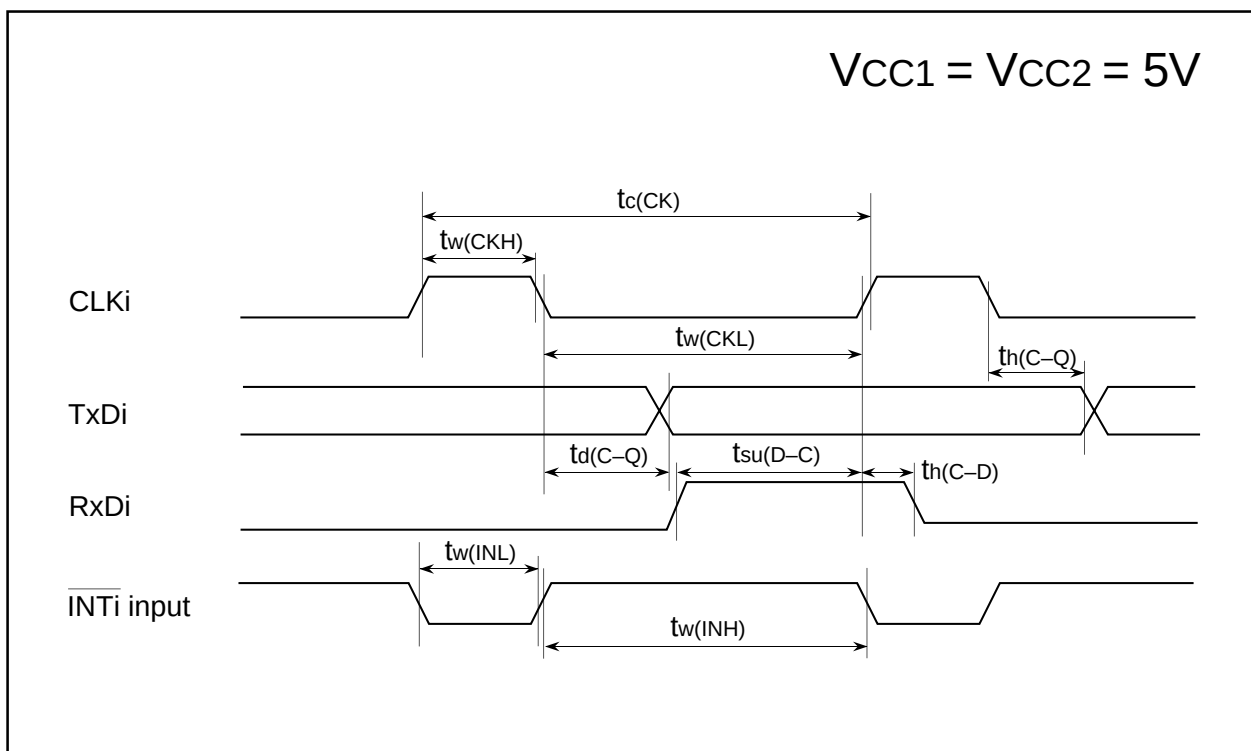
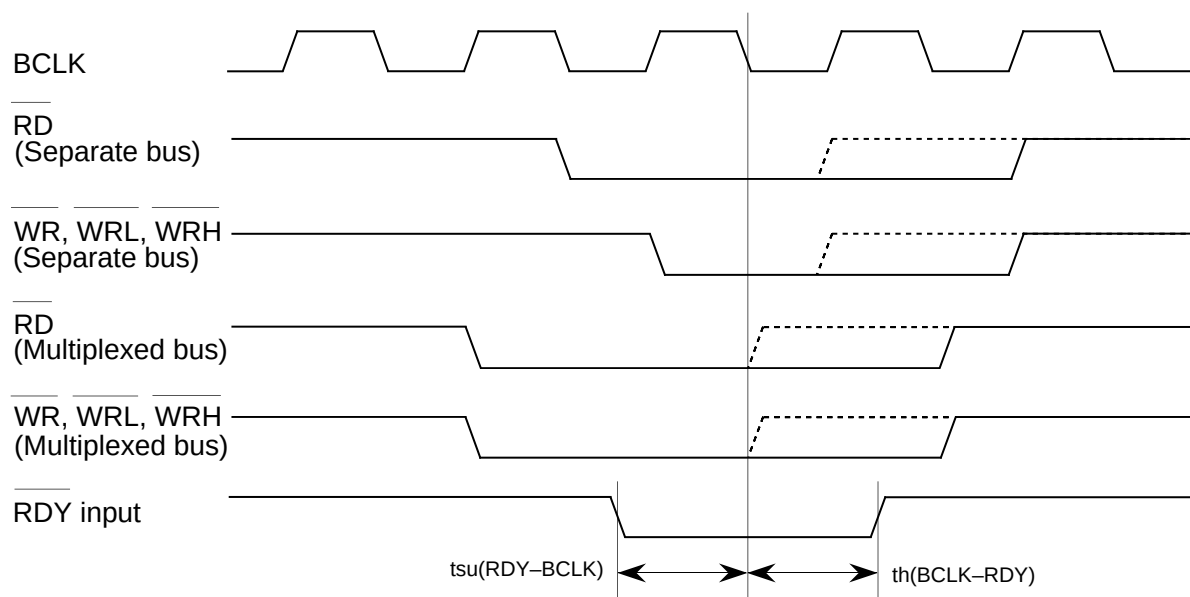


Figure 1.5.2. Timing Diagram (1)

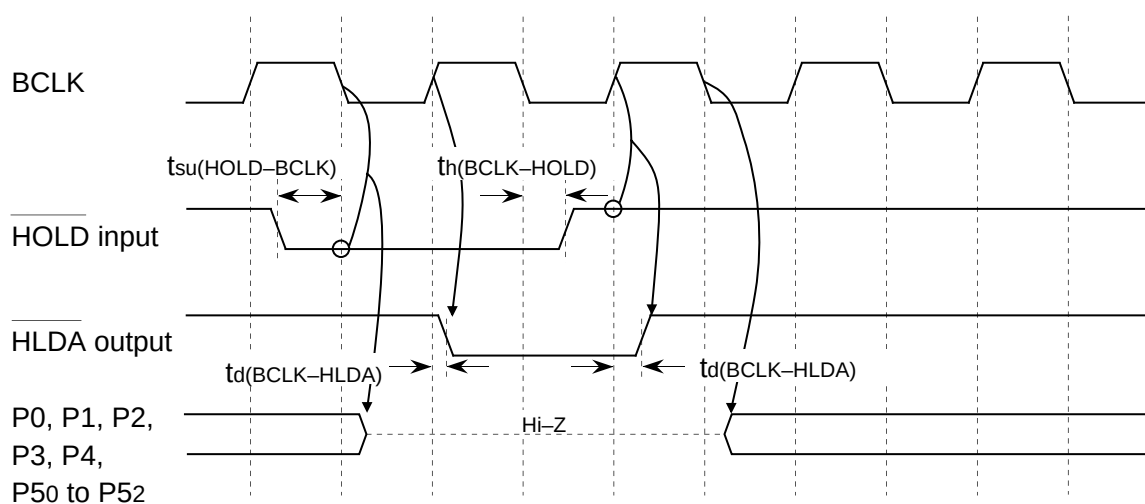
**Figure 1.5.3. Timing Diagram (2)**

Memory Expansion Mode, Microprocessor Mode

(Effective for setting with wait)

 $V_{CC1} = V_{CC2} = 5V$ 

(Common to setting with wait and setting without wait)



Note: The above pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

Measuring conditions :

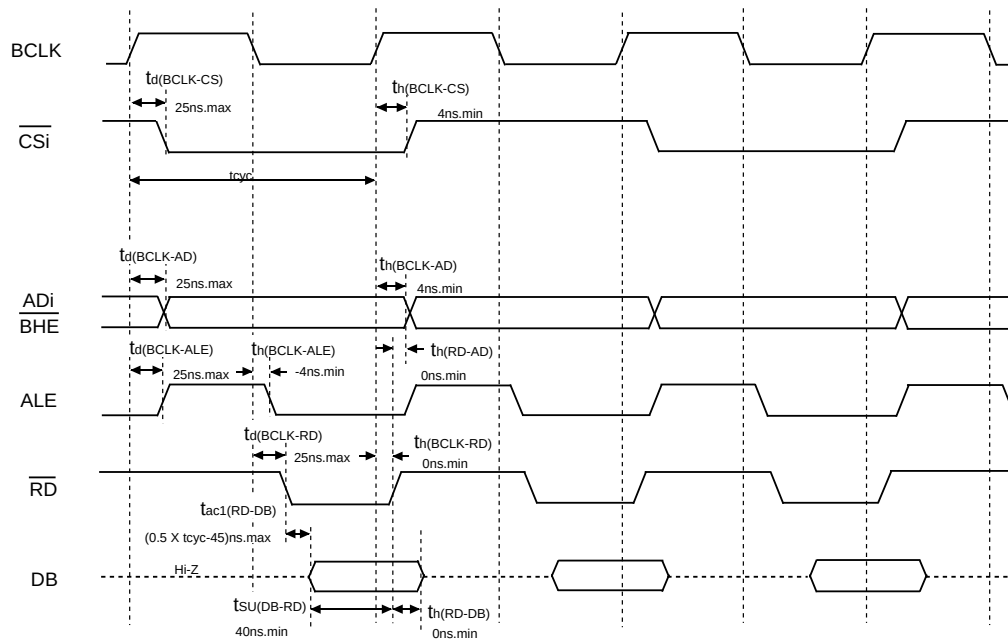
- $V_{CC1}=V_{CC2}=5V$
- Input timing voltage : Determined with $V_{IL}=1.0V$, $V_{IH}=4.0V$
- Output timing voltage : Determined with $V_{OL}=2.5V$, $V_{OH}=2.5V$

Figure 1.5.4. Timing Diagram (3)

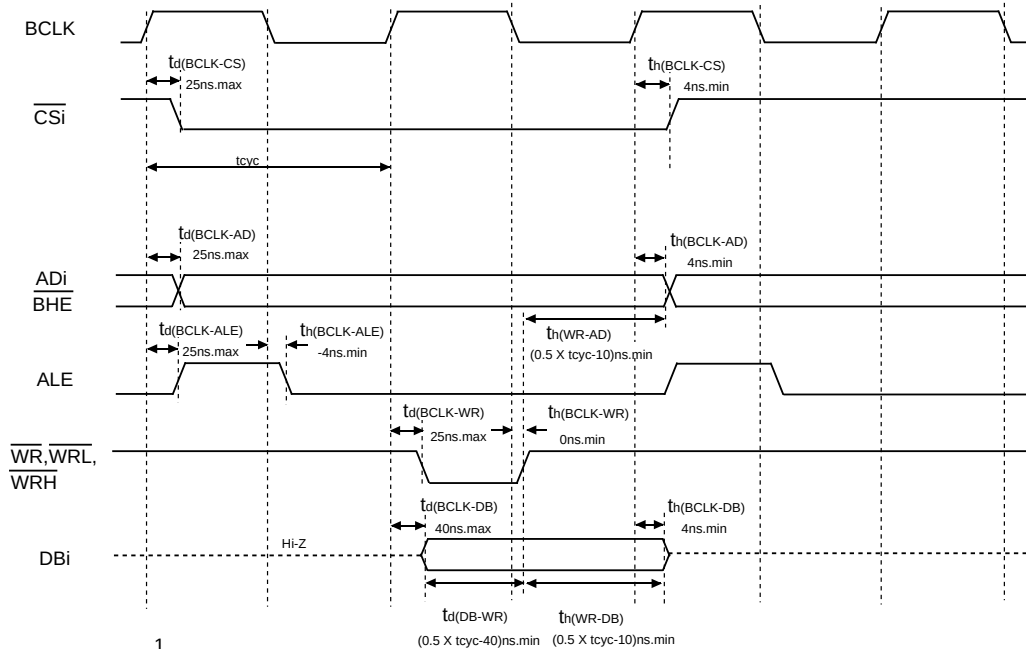
VCC1 = VCC2 = 5V

Memory Expansion Mode, Microprocessor Mode (For setting with no wait)

Read timing



Write timing



$$t_{\text{cyc}} = \frac{1}{f(\text{BCLK})}$$

Measuring conditions

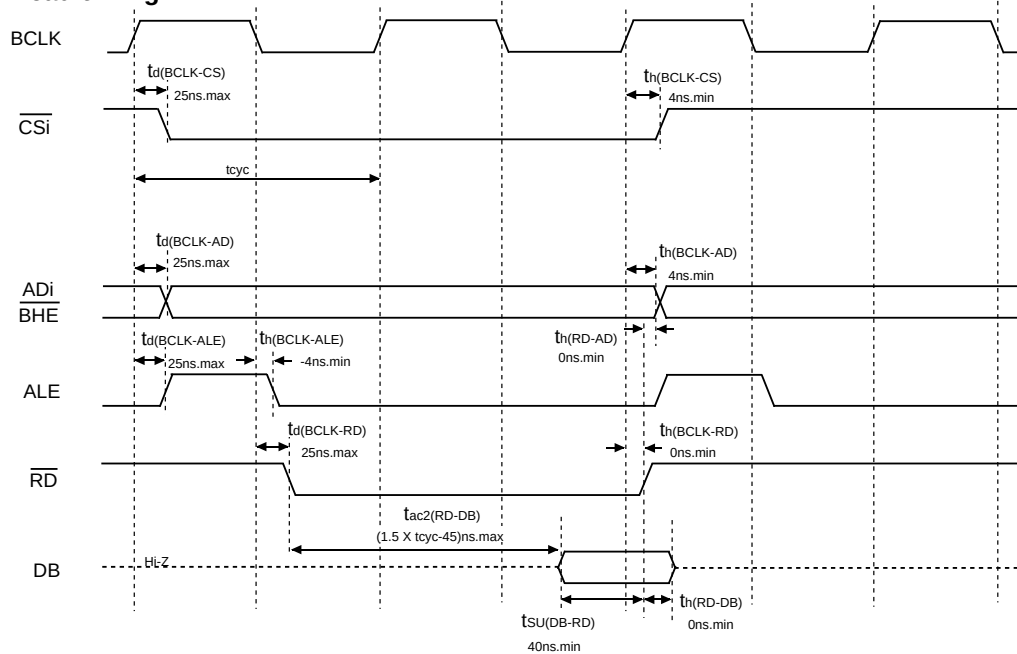
- VCC1=VCC2=5V
- Input timing voltage : $V_{\text{IL}}=0.8\text{V}$, $V_{\text{IH}}=2.0\text{V}$
- Output timing voltage : $V_{\text{OL}}=0.4\text{V}$, $V_{\text{OH}}=2.4\text{V}$

Figure 1.5.5. Timing Diagram (4)

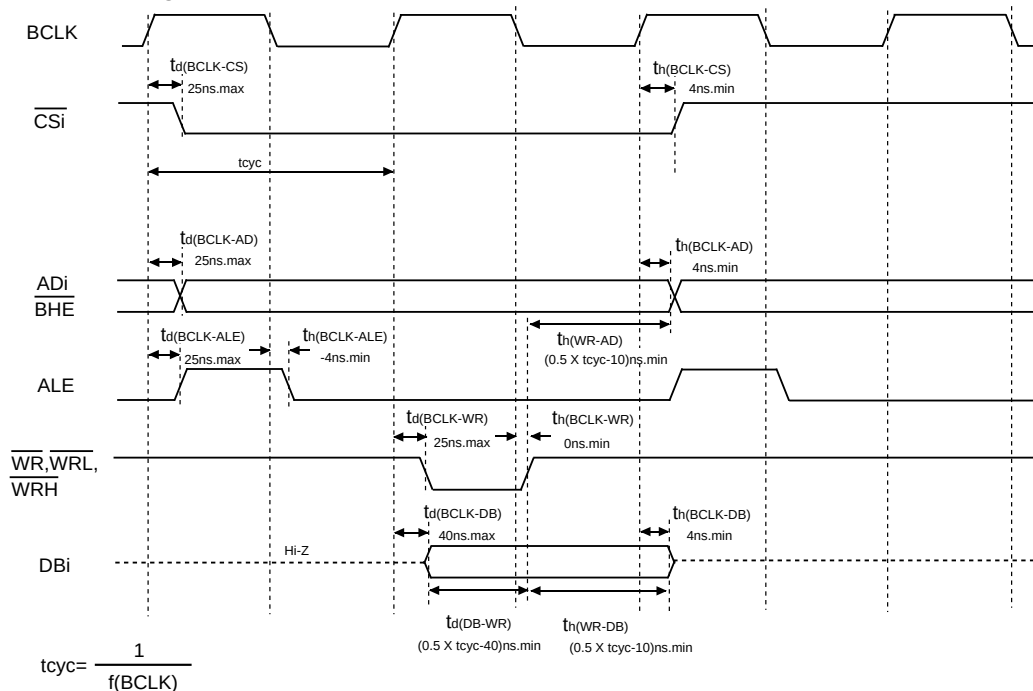
$$V_{CC1} = V_{CC2} = 5V$$

Memory Expansion Mode, Microprocessor Mode (for 1-wait setting and external area access)

Read timing



Write timing



Measuring conditions

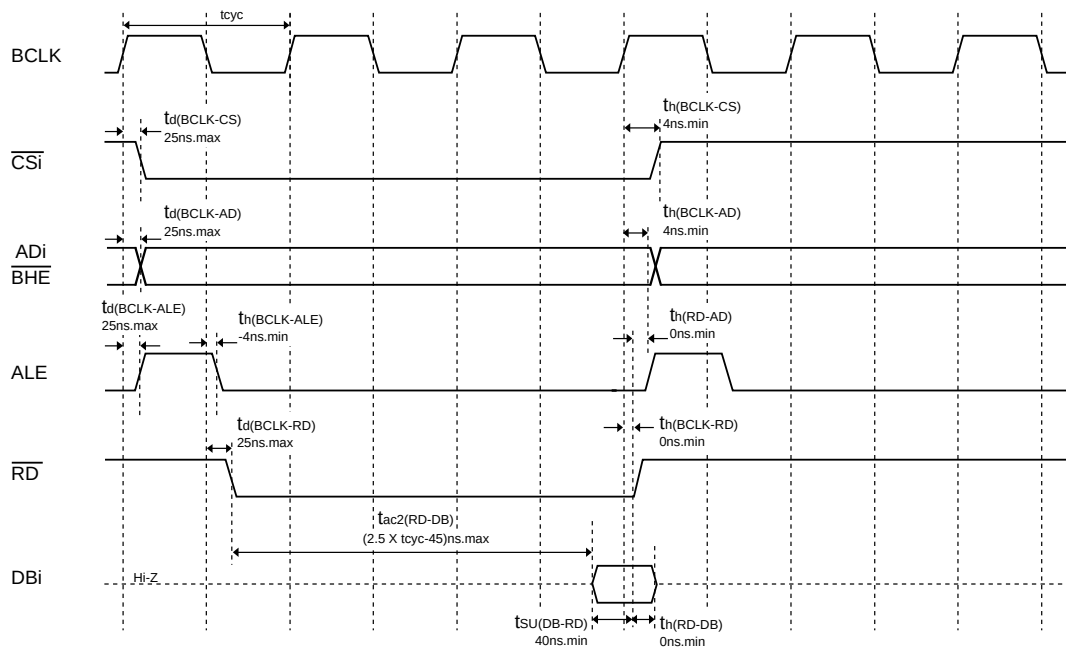
- VCC1=VCC2=5V
- Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
- Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 1.5.6. Timing Diagram (5)

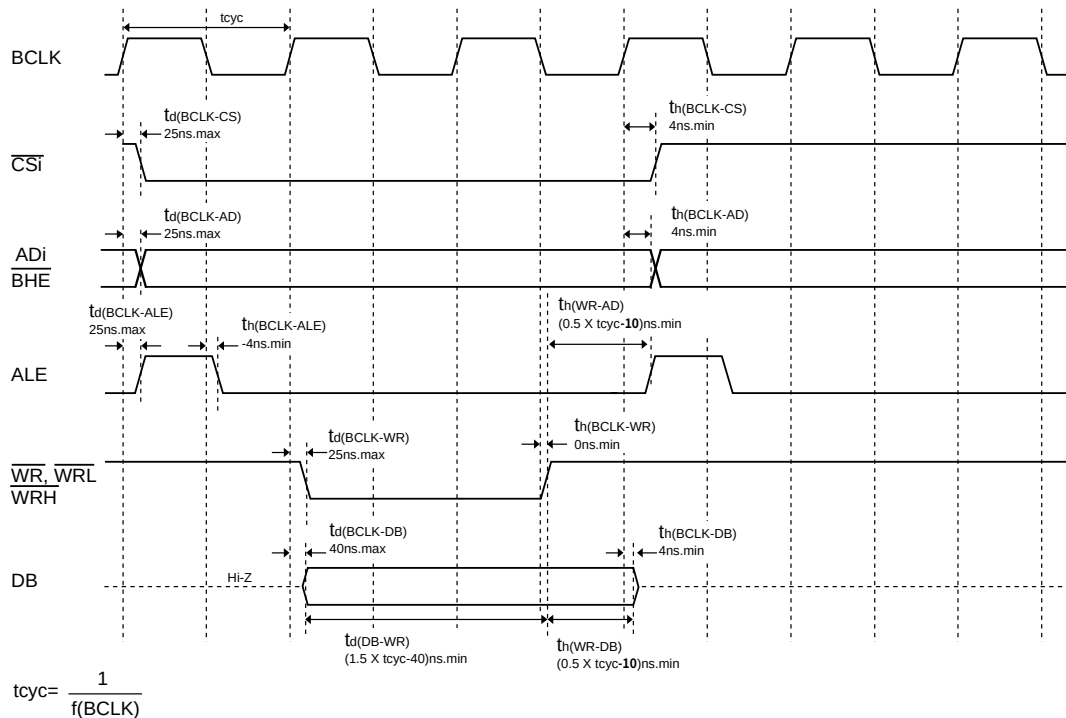
VCC1 = VCC2 = 5V

Memory Expansion Mode, Microprocessor Mode (for 2-wait setting and external area access)

Read timing



Write timing



Measuring conditions

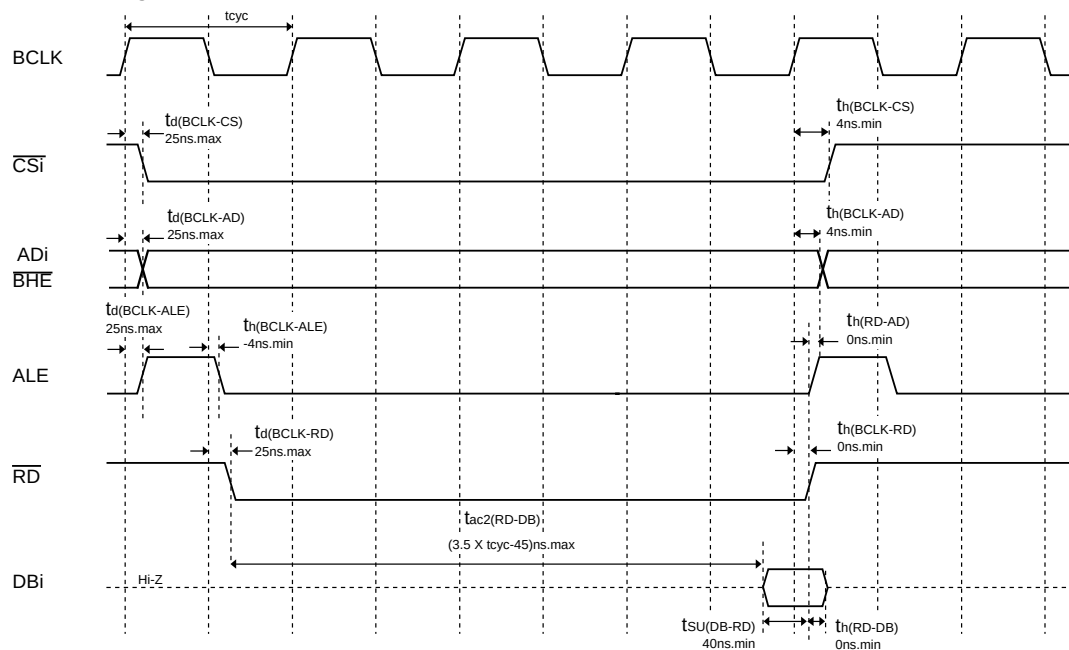
- VCC1=VCC2=5V
- Input timing voltage : VIL=0.8V, VIH=2.0V

Figure 1.5.7. Timing Diagram (6)

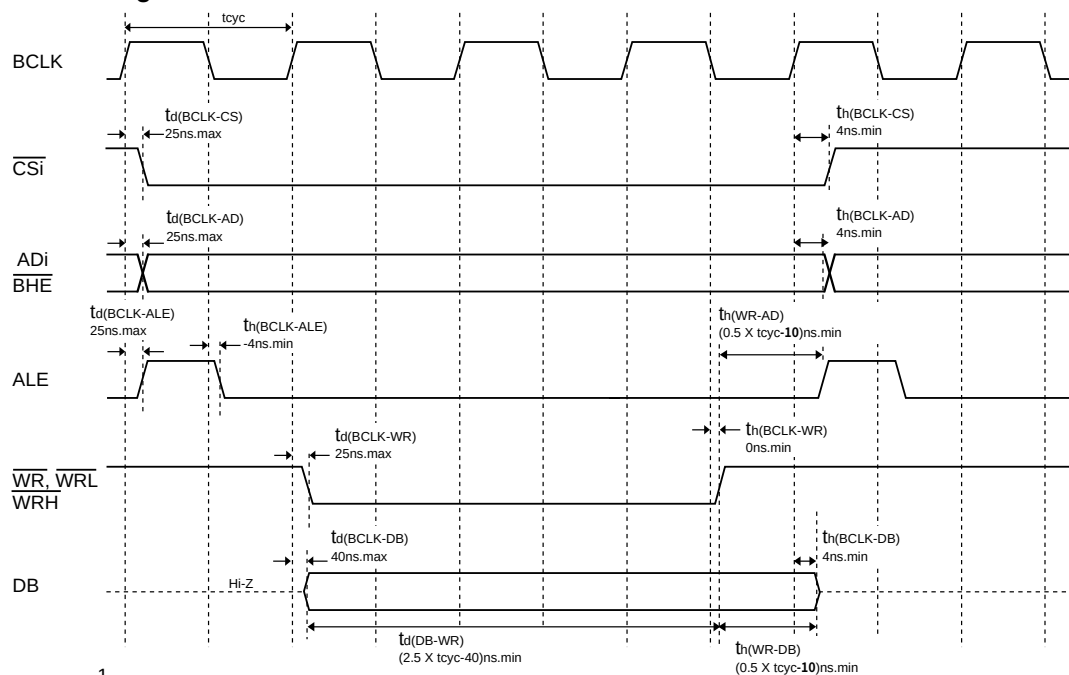
V_{CC1} = V_{CC2} = 5V

Memory Expansion Mode, Microprocessor Mode (for 3-wait setting and external area access)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

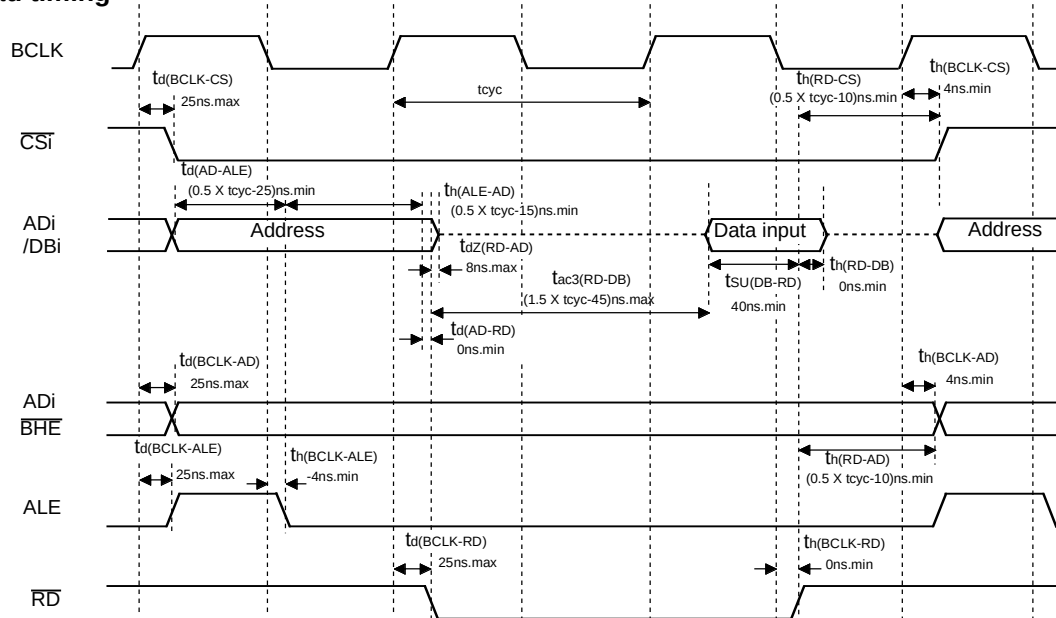
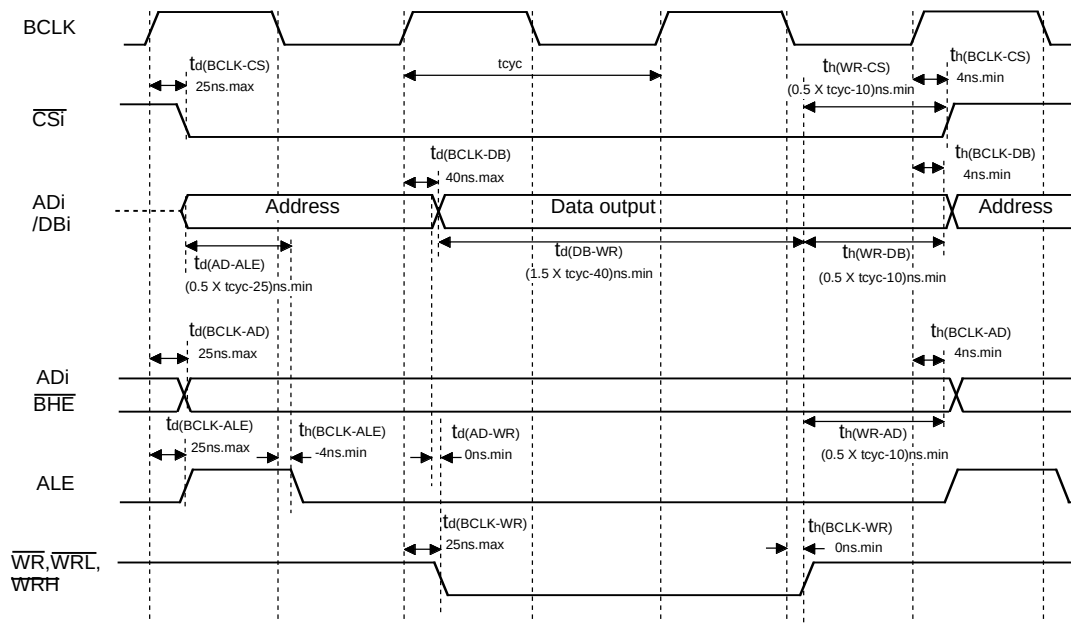
- V_{CC1}=V_{CC2}=5V
- Input timing voltage : V_{IL}=0.8V, V_{IH}=2.0V
- Output timing voltage : V_{OL}=0.4V, V_{OH}=2.4V

Figure 1.5.8. Timing Diagram (7)

VCC1 = VCC2 = 5V

Memory Expansion Mode, Microprocessor Mode

(For 1- or 2-wait setting, external area access and multiplex bus selection)

Read timing**Write timing**

$$t_{\text{cyc}} = \frac{1}{f(\text{BCLK})}$$

Measuring conditions

- Vcc1=Vcc2=5V
- Input timing voltage : $V_{\text{IL}}=0.8\text{V}$, $V_{\text{IH}}=2.0\text{V}$
- Output timing voltage : $V_{\text{OL}}=0.4\text{V}$, $V_{\text{OH}}=2.4\text{V}$

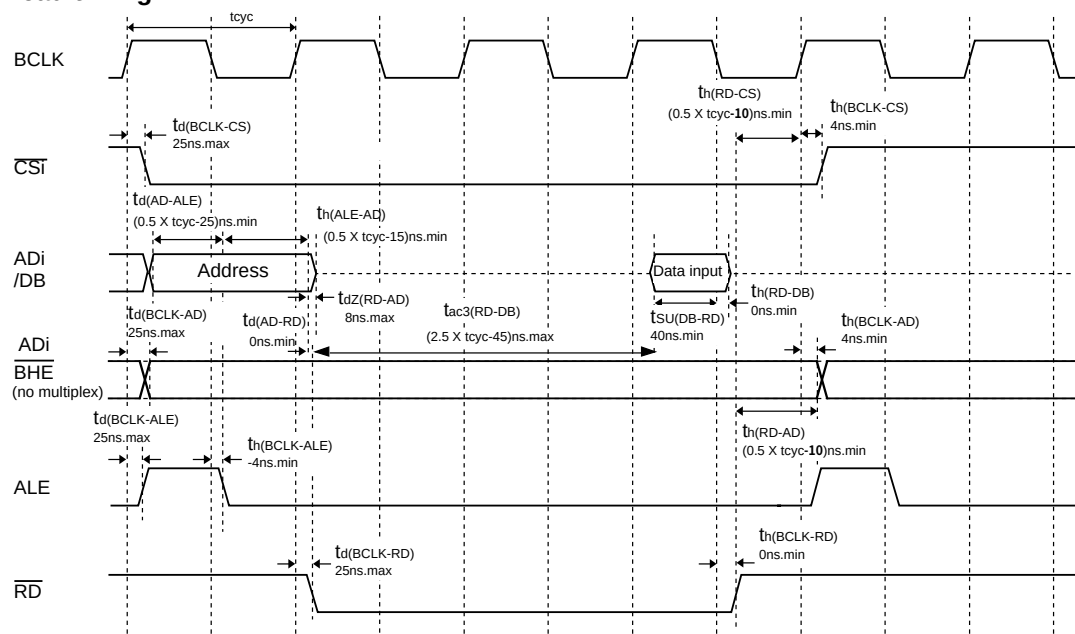
Figure 1.5.9. Timing Diagram (8)

$$V_{CC1} = V_{CC2} = 5V$$

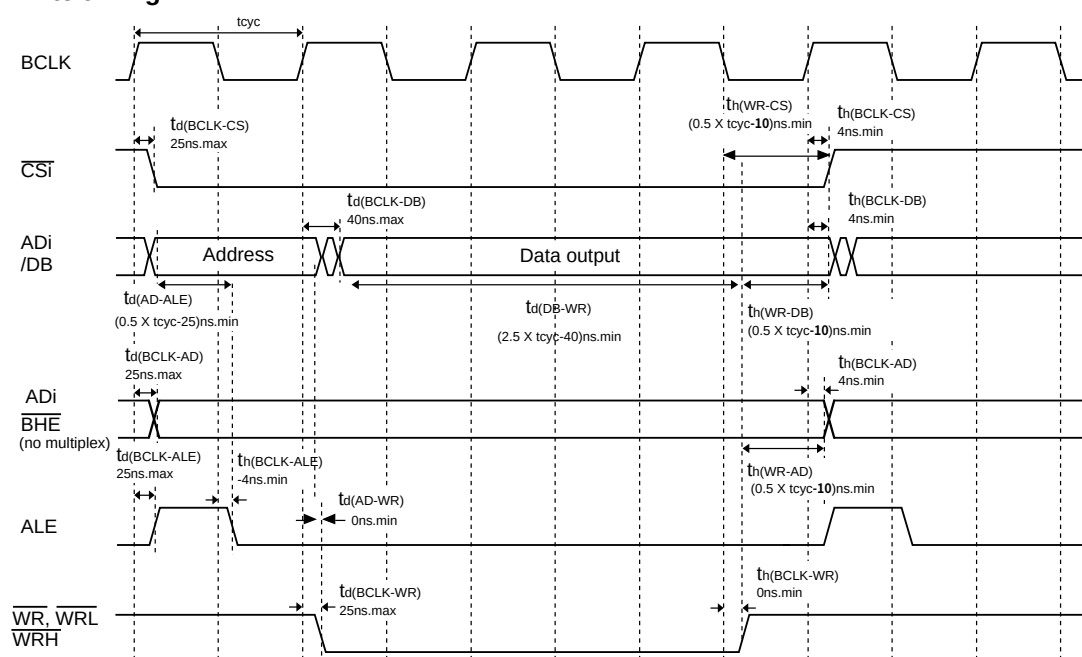
Memory Expansion Mode, Microprocessor Mode

(For 3-wait setting, external area access and multiplex bus selection)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1}=V_{CC2}=5V$
- Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
- Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 1.5.10. Timing Diagram (9)

$$V_{CC1} = V_{CC2} = 3V$$

Table 1.5.29. Electrical Characteristics (Note)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	HIGH output voltage	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P6 ₀ to P6 ₇ , P7 ₀ to P7 ₇ , P8 ₀ to P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇ , P14 ₀ , P14 ₁	I _{OH} = -1mA	V _{CC} -0.5		V _{CC}	V
V _{OH}	HIGH output voltage	XOUT	HIGHPOWER	V _{CC} -0.5		V _{CC}	V
			LOWPOWER	V _{CC} -0.5		V _{CC}	
	HIGH output voltage	XCOUT	HIGHPOWER		2.5		V
			LOWPOWER		1.6		
V _{OL}	LOW output voltage	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P6 ₀ to P6 ₇ , P7 ₀ to P7 ₇ , P8 ₀ to P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇ , P14 ₀ , P14 ₁	I _{OL} = 1mA			0.5	V
V _{OL}	LOW output voltage	XOUT	HIGHPOWER			0.5	V
			LOWPOWER			0.5	
	LOW output voltage	XCOUT	HIGHPOWER		0		V
			LOWPOWER		0		
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0 _{IN} to TA4 _{IN} , TB0 _{IN} to TB5 _{IN} , INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, SCL, SDA, CLK0 to CLK4, TA2 _{OUT} to TA4 _{OUT} , K10 to K13, Rx0 to Rx2, SIN3, SIN4		0.2		0.8	V
V _{T+} -V _{T-}	Hysteresis	RESET		0.2	(0.7)	1.8	V
I _{IH}	HIGH input current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P6 ₀ to P6 ₇ , P7 ₀ to P7 ₇ , P8 ₀ to P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇ , P14 ₀ , P14 ₁ , XIN, RESET, CNVss, BYTE	V _I = 3V			4.0	μA
I _{IL}	LOW input current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P6 ₀ to P6 ₇ , P7 ₀ to P7 ₇ , P8 ₀ to P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇ , P14 ₀ , P14 ₁ , XIN, RESET, CNVss, BYTE	V _I = 0V			-4.0	μA
R _{PULLUP}	Pull-up resistance	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₇ , P6 ₀ to P6 ₇ , P7 ₀ to P7 ₇ , P8 ₀ to P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ to P9 ₇ , P10 ₀ to P10 ₇ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₇ , P13 ₀ to P13 ₇ , P14 ₀ , P14 ₁	V _I = 0V	50	100	500	kΩ
R _{XIN}	Feedback resistance	XIN			3.0		MΩ
R _{XCIN}	Feedback resistance	XCIN			25		MΩ
V _{RAM}	RAM retention voltage		At stop mode	2.0			V

Note 1 : Referenced to V_{CC}=V_{CC1}=V_{CC2}=2.7 to 3.3V, V_{SS}=0V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

Note 2 : V_{CC1} for the port P6 to P11 and P14, and V_{CC2} for the port P0 to P5 and P12 to P13.

$$V_{CC1} = V_{CC2} = 3V$$

Table 1.5.30. Electrical Characteristics (2) (Note 1)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
Icc	Power supply current (Vcc1=2.7 to 3.6V)	In single-chip mode, the output pins are open and other pins are Vss	Mask ROM	f(BCLK)=10MHz, No division		8	11	mA
				No division, Ring oscillation		1		mA
			Flash memory	f(BCLK)=10MHz, No division		8	13	mA
				No division, Ring oscillation		1.8		mA
			Flash memory Program	f(BCLK)=10MHz, Vcc1=3.0V		12		mA
			Flash memory Erase	f(BCLK)=10MHz, Vcc1=3.0V		22		mA
			Mask ROM	f(Xcin)=32kHz, Low power dissipation mode, ROM(Note 3)		25		μA
			Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM(Note 3)		25		μA
				f(BCLK)=32kHz, Low power dissipation mode, Flash memory(Note 3)		420		μA
				Ring oscillation, Wait mode		45		μA
			Mask ROM Flash memory	f(BCLK)=32kHz, Wait mode (Note 2), Oscillation capacity High		6.0		μA
				f(BCLK)=32kHz, Wait mode (Note 2), Oscillation capacity Low		1.8		μA
				Stop mode, Topr=25°C		0.7	3.0	μA
Idet4	Voltage down detection dissipation current (Note 4)				0.6	4	μA	
Idet3	Reset level detection dissipation current (Note 4)				0.4	2	μA	
Idet2	RAM retention limit detection dissipation current (Note 4)				0.9	4	μA	

Note 1: Referenced to Vcc=Vcc1=Vcc2=2.7 to 3.3V, Vss=0V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

Note 2: With one timer operated using fc32.

Note 3: This indicates the memory in which the program to be executed exists.

Note 4: I_{det} is dissipation current when the following bit is set to "1" (detection circuit enabled).

I_{det4}: VC27 bit of VCR2 register

I_{det3}: VC26 bit of VCR2 register

I_{det2}: VC25 bit of VCR2 register

$$V_{CC1} = V_{CC2} = 3V$$

Timing Requirements

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.31. External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c	External clock input cycle time	100		ns
t _{w(H)}	External clock input HIGH pulse width	40		ns
t _{w(L)}	External clock input LOW pulse width	40		ns
t _r	External clock rise time		18	ns
t _f	External clock fall time		18	ns

Table 1.5.32. Memory Expansion and Microprocessor Modes

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{ac1} (RD-DB)	Data input access time (for setting with no wait)		(Note 1)	ns
t _{ac2} (RD-DB)	Data input access time (for setting with wait)		(Note 2)	ns
t _{ac3} (RD-DB)	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
t _{su} (DB-RD)	Data input setup time	50		ns
t _{su} (RDY-BCLK)	RDY input setup time	40		ns
t _{su} (HOLD-BCLK)	HOLD input setup time	50		ns
t _h (RD-DB)	Data input hold time	0		ns
t _h (BCLK-RDY)	RDY input hold time	0		ns
t _h (BCLK-HOLD)	HOLD input hold time	0		ns
t _d (BCLK-HLDA)	HLDA output delay time		40	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 60 \quad [\text{ns}]$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 60 \quad [\text{ns}] \quad \text{n is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.}$$

Note 3: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 60 \quad [\text{ns}] \quad \text{n is "2" for 2-wait setting, "3" for 3-wait setting.}$$

$$V_{CC1} = V_{CC2} = 3V$$

Timing Requirements(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = – 20 to 85°C / – 40 to 85°C unless otherwise specified)**Table 1.5.33. Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiN input cycle time	150		ns
t _w (TAH)	TAiN input HIGH pulse width	60		ns
t _w (TAL)	TAiN input LOW pulse width	60		ns

Table 1.5.34. Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiN input cycle time	600		ns
t _w (TAH)	TAiN input HIGH pulse width	300		ns
t _w (TAL)	TAiN input LOW pulse width	300		ns

Table 1.5.35. Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiN input cycle time	300		ns
t _w (TAH)	TAiN input HIGH pulse width	150		ns
t _w (TAL)	TAiN input LOW pulse width	150		ns

Table 1.5.36. Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _w (TAH)	TAiN input HIGH pulse width	150		ns
t _w (TAL)	TAiN input LOW pulse width	150		ns

Table 1.5.37. Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (UP)	TAiOUT input cycle time	3000		ns
t _w (UPH)	TAiOUT input HIGH pulse width	1500		ns
t _w (UPL)	TAiOUT input LOW pulse width	1500		ns
t _{su} (UP-TiN)	TAiOUT input setup time	600		ns
t _h (TiN-UP)	TAiOUT input hold time	600		ns

Table 1.5.38. Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiN input cycle time	2		μs
t _{su} (TAiN-TAOUT)	TAiOUT input setup time	500		ns
t _{su} (TAOUT-TAiN)	TAiN input setup time	500		ns

$$V_{CC1} = V_{CC2} = 3V$$

Timing Requirements(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = – 20 to 85°C / – 40 to 85°C unless otherwise specified)**Table 1.5.39. Timer B Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiN input cycle time (counted on one edge)	150		ns
t _w (TBH)	TBiN input HIGH pulse width (counted on one edge)	60		ns
t _w (TBL)	TBiN input LOW pulse width (counted on one edge)	60		ns
t _c (TB)	TBiN input cycle time (counted on both edges)	300		ns
t _w (TBH)	TBiN input HIGH pulse width (counted on both edges)	120		ns
t _w (TBL)	TBiN input LOW pulse width (counted on both edges)	120		ns

Table 1.5.40. Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiN input cycle time	600		ns
t _w (TBH)	TBiN input HIGH pulse width	300		ns
t _w (TBL)	TBiN input LOW pulse width	300		ns

Table 1.5.41. Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiN input cycle time	600		ns
t _w (TBH)	TBiN input HIGH pulse width	300		ns
t _w (TBL)	TBiN input LOW pulse width	300		ns

Table 1.5.42. A-D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (AD)	ADTRG input cycle time (trigger able minimum)	1500		ns
t _w (ADL)	ADTRG input LOW pulse width	200		ns

Table 1.5.43. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (CK)	CLKi input cycle time	300		ns
t _w (CKH)	CLKi input HIGH pulse width	150		ns
t _w (CKL)	CLKi input LOW pulse width	150		ns
t _d (C-Q)	TxDi output delay time		160	ns
t _h (C-Q)	TxDi hold time	0		ns
t _{su} (D-C)	RxDi input setup time	50		ns
t _h (C-D)	RxDi input hold time	90		ns

Table 1.5.44. External Interrupt INTi Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _w (INH)	INTi input HIGH pulse width	380		ns
t _w (INL)	INTi input LOW pulse width	380		ns

$$V_{CC1} \geq V_{CC2} = 3V$$

Switching Characteristics(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = – 20 to 85°C / – 40 to 85°C unless otherwise specified)**Table 1.5.45. Memory Expansion, Microprocessor Modes (for setting with no wait)**

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address output delay time	Figure 1.5.11		30	ns
t _h (BCLK-AD)	Address output hold time (refers to BCLK)		4		ns
t _h (RD-AD)	Address output hold time (refers to RD)		0		ns
t _h (WR-AD)	Address output hold time (refers to WR)		(Note 2)		ns
t _d (BCLK-CS)	Chip select output delay time			30	ns
t _h (BCLK-CS)	Chip select output hold time (refers to BCLK)		4		ns
t _d (BCLK-ALE)	ALE signal output delay time			30	ns
t _h (BCLK-ALE)	ALE signal output hold time		–4		ns
t _d (BCLK-RD)	RD signal output delay time			30	ns
t _h (BCLK-RD)	RD signal output hold time		0		ns
t _d (BCLK-WR)	WR signal output delay time			30	ns
t _h (BCLK-WR)	WR signal output hold time		0		ns
t _d (BCLK-DB)	Data output delay time (refers to BCLK)			40	ns
t _h (BCLK-DB)	Data output hold time (refers to BCLK)(Note 3)		4		ns
t _d (DB-WR)	Data output delay time (refers to WR)		(Note 1)		ns
t _h (WR-DB)	Data output hold time (refers to WR)(Note 3)		(Note 2)		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40 \quad [\text{ns}] \quad f(\text{BCLK}) \text{ is } 12.5\text{MHz or less.}$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \quad [\text{ns}]$$

Note 3: This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

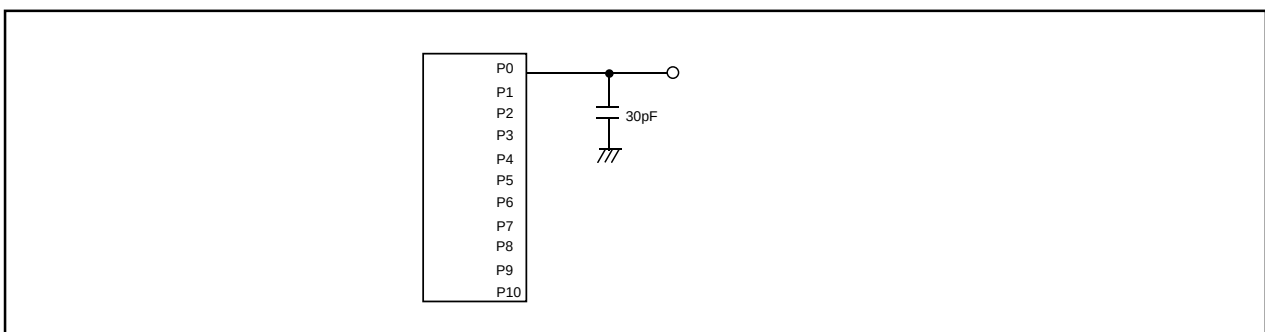
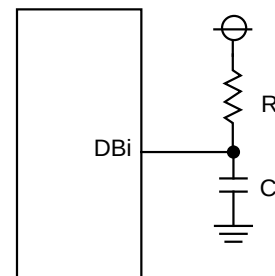
Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$$

by a circuit of the right figure.

For example, when V_{OL} = 0.2V_{CC2}, C = 30pF, R = 1kΩ, hold time of output “L” level is

$$t = -30\text{pF} \times 1\text{k}\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2}) \\ = 6.7\text{ns.}$$

**Figure 1.5.11. Ports P0 to P10 Measurement Circuit**

$$V_{CC1} \geq V_{CC2} = 3V$$

Switching Characteristics

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.46. Memory expansion and Microprocessor Modes
(for 1- to 3-wait setting and external area access)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address output delay time	Figure 1.5.11		30	ns
t _h (BCLK-AD)	Address output hold time (refers to BCLK)		4		ns
t _h (RD-AD)	Address output hold time (refers to RD)		0		ns
t _h (WR-AD)	Address output hold time (refers to WR)		(Note 2)		ns
t _d (BCLK-CS)	Chip select output delay time			30	ns
t _h (BCLK-CS)	Chip select output hold time (refers to BCLK)		4		ns
t _d (BCLK-ALE)	ALE signal output delay time			30	ns
t _h (BCLK-ALE)	ALE signal output hold time		–4		ns
t _d (BCLK-RD)	RD signal output delay time			30	ns
t _h (BCLK-RD)	RD signal output hold time		0		ns
t _d (BCLK-WR)	WR signal output delay time			30	ns
t _h (BCLK-WR)	WR signal output hold time		0		ns
t _d (BCLK-DB)	Data output delay time (refers to BCLK)			40	ns
t _h (BCLK-DB)	Data output hold time (refers to BCLK)(Note 3)		4		ns
t _d (DB-WR)	Data output delay time (refers to WR)		(Note 1)		ns
t _h (WR-DB)	Data output hold time (refers to WR)(Note 3)		(Note 2)		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 40 \quad [\text{ns}]$$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting.
When n=1, f(BCLK) is 12.5MHz or less.

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \quad [\text{ns}]$$

Note 3: This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

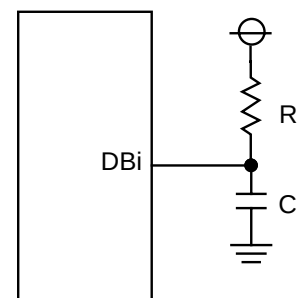
Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$$

by a circuit of the right figure.

For example, when V_{OL} = 0.2V_{CC2}, C = 30pF, R = 1kΩ, hold time of output "L" level is

$$t = -30\text{pF} \times 1\text{k}\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2}) = 6.7\text{ns}.$$



$$V_{CC1} \geq V_{CC2} = 3V$$

Switching Characteristics(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = – 20 to 85°C / – 40 to 85°C, unless otherwise specified)**Table 1.5.47. Memory expansion and Microprocessor Modes**
(for 2- to 3-wait setting, external area access and multiplex bus selection)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address output delay time	Figure 1.5.11		50	ns
t _h (BCLK-AD)	Address output hold time (refers to BCLK)		4		ns
t _h (RD-AD)	Address output hold time (refers to RD)		(Note 1)		ns
t _h (WR-AD)	Address output hold time (refers to WR)		(Note 1)		ns
t _d (BCLK-CS)	Chip select output delay time			50	ns
t _h (BCLK-CS)	Chip select output hold time (refers to BCLK)		4		ns
t _h (RD-CS)	Chip select output hold time (refers to RD)		(Note 1)		ns
t _h (WR-CS)	Chip select output hold time (refers to WR)		(Note 1)		ns
t _d (BCLK-RD)	RD signal output delay time			40	ns
t _h (BCLK-RD)	RD signal output hold time		0		ns
t _d (BCLK-WR)	WR signal output delay time			40	ns
t _h (BCLK-WR)	WR signal output hold time		0		ns
t _d (BCLK-DB)	Data output delay time (refers to BCLK)			50	ns
t _h (BCLK-DB)	Data output hold time (refers to BCLK)		4		ns
t _d (DB-WR)	Data output delay time (refers to WR)		(Note 2)		ns
t _h (WR-DB)	Data output hold time (refers to WR)		(Note 1)		ns
t _d (BCLK-ALE)	ALE signal output delay time (refers to BCLK)			40	ns
t _h (BCLK-ALE)	ALE signal output hold time (refers to BCLK)		– 4		ns
t _d (AD-ALE)	ALE signal output delay time (refers to Address)		(Note 3)		ns
t _h (ALE-AD)	ALE signal output hold time (refers to Address)		(Note 4)		ns
t _d (AD-RD)	RD signal output delay from the end of Address		0		ns
t _d (AD-WR)	WR signal output delay from the end of Address		0		ns
t _d (RD-AD)	Address output floating start time			8	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \quad [\text{ns}]$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 50 \quad [\text{ns}] \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

Note 3: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40 \quad [\text{ns}]$$

Note 4: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 15 \quad [\text{ns}]$$

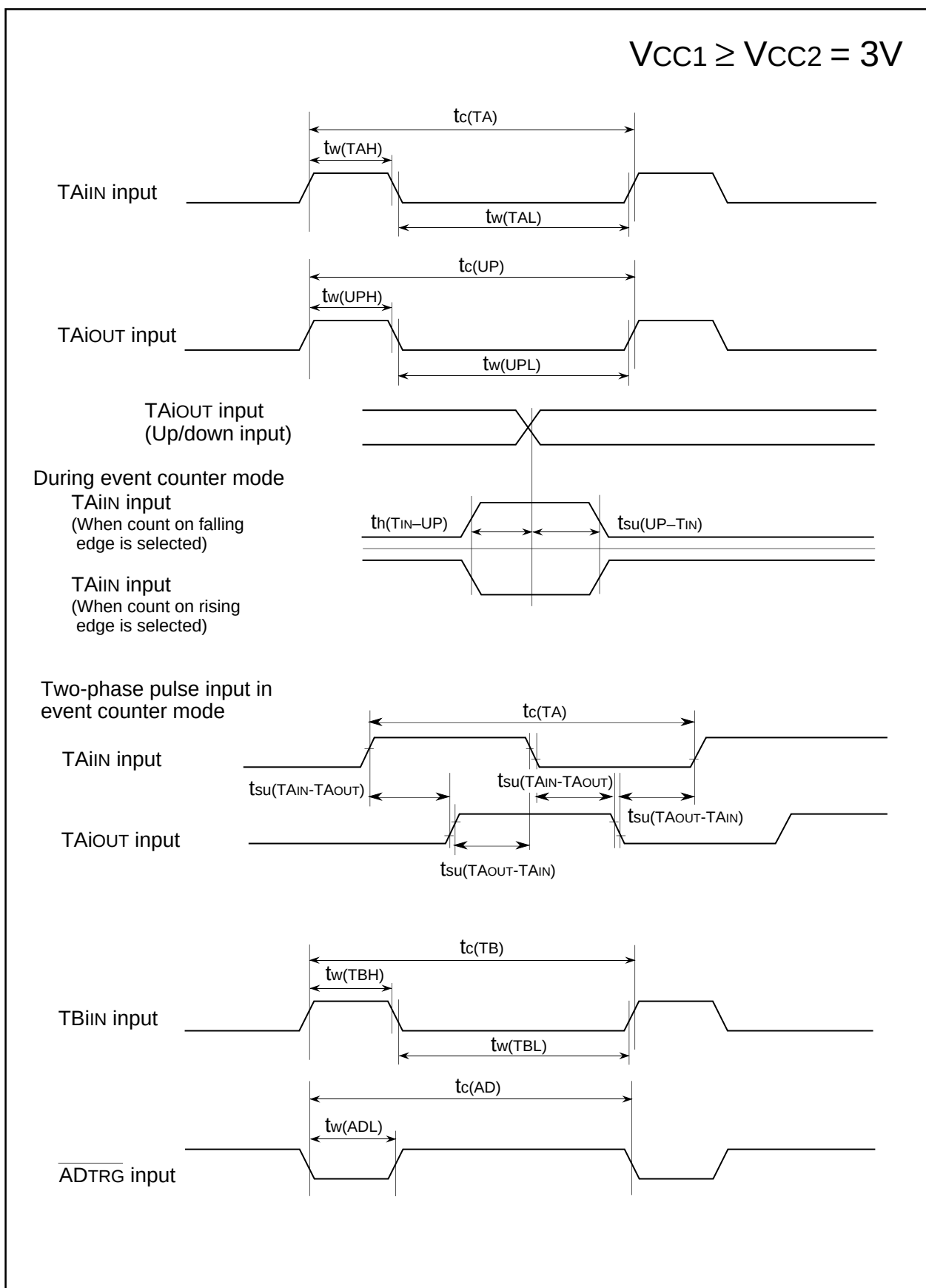


Figure 1.5.12. Timing Diagram (1)

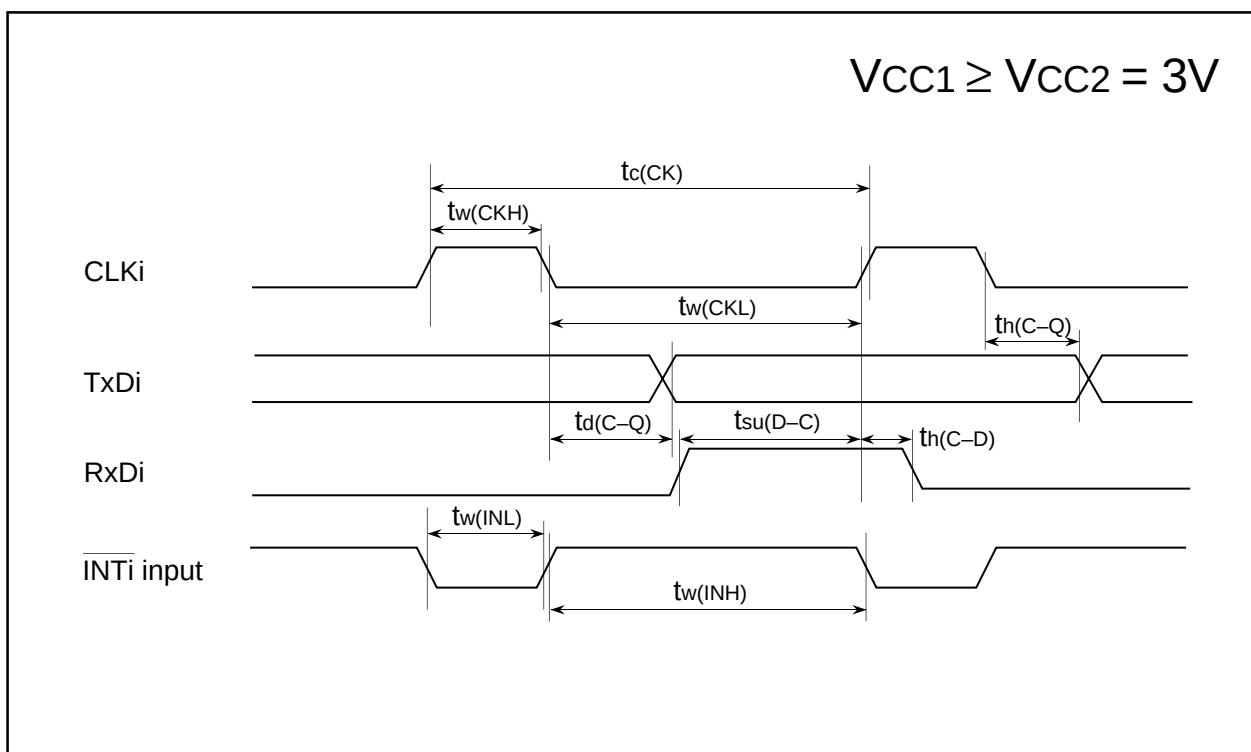
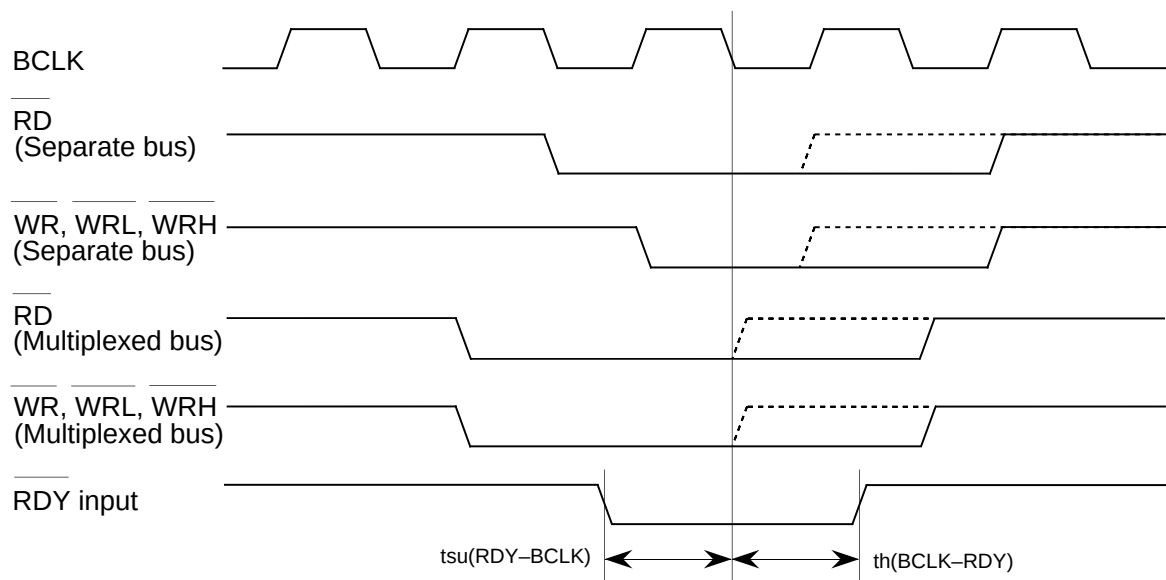


Figure 1.5.13. Timing Diagram (2)

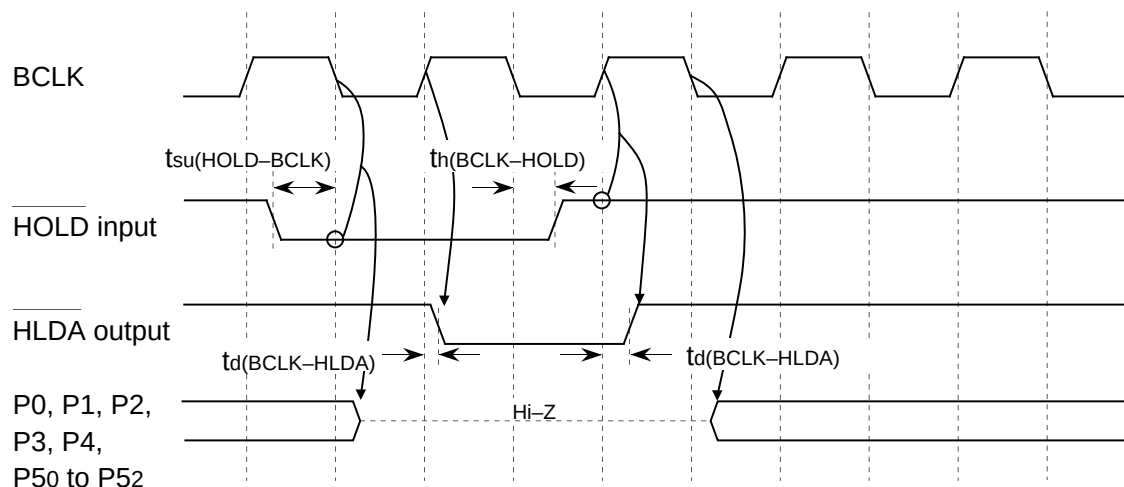
$$V_{CC1} \geq V_{CC2} = 3V$$

Memory Expansion Mode, Microprocessor Mode

(Effective for setting with wait)



(Common to setting with wait and setting without wait)



Note: The above pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit of PM0 register and PM11 bit of PM1 register.

Measuring conditions :

- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

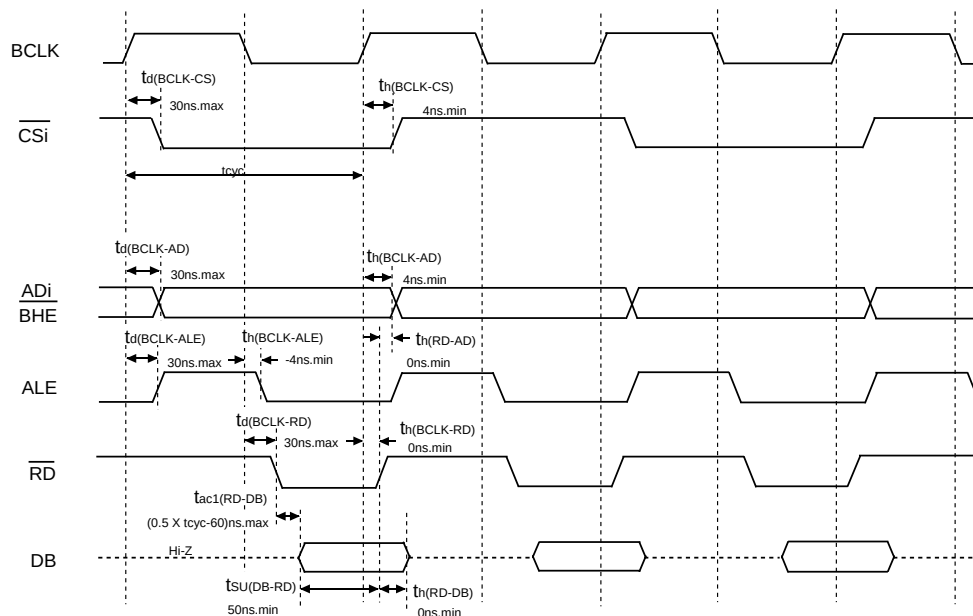
Figure 1.5.14. Timing Diagram (3)

$$V_{CC1} \geq V_{CC2} = 3V$$

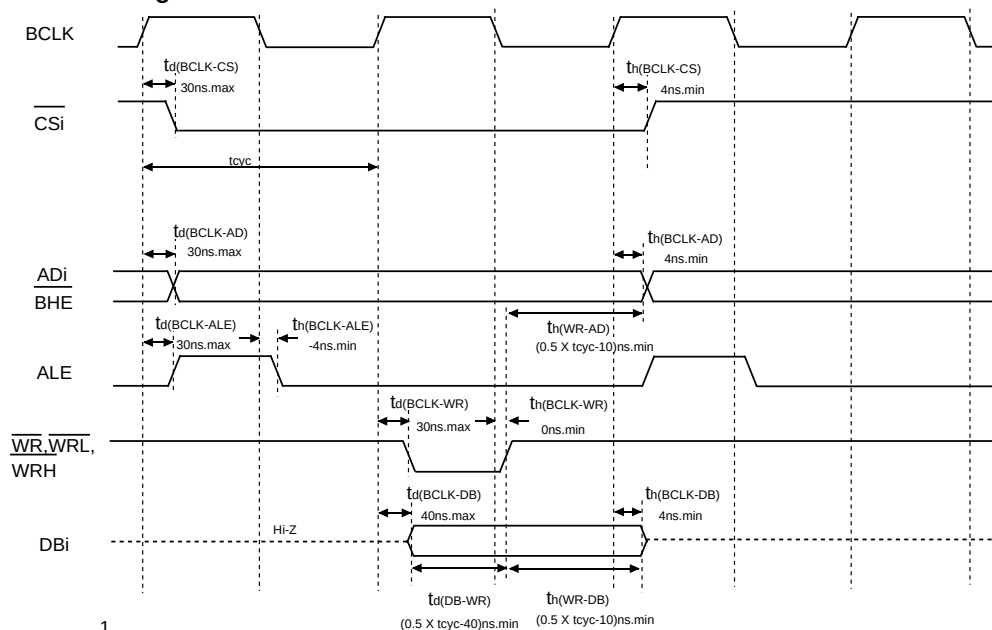
Memory Expansion Mode, Microprocessor Mode

(For setting with no wait)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions

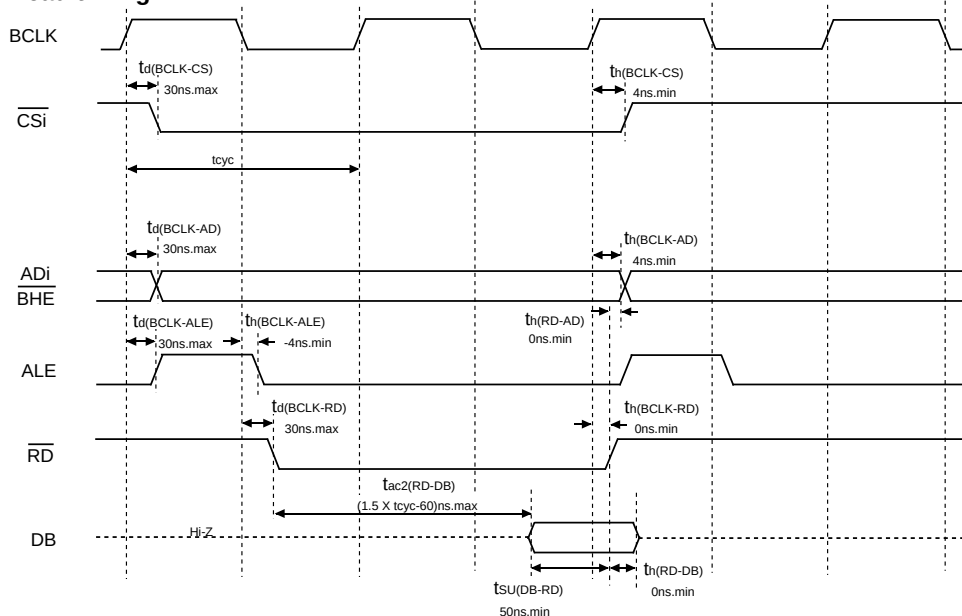
- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage : $V_{IL} = 0.6V$, $V_{IH} = 2.4V$
- Output timing voltage : $V_{OL} = 1.5V$, $V_{OH} = 1.5V$

Figure 1.5.15. Timing Diagram (4)

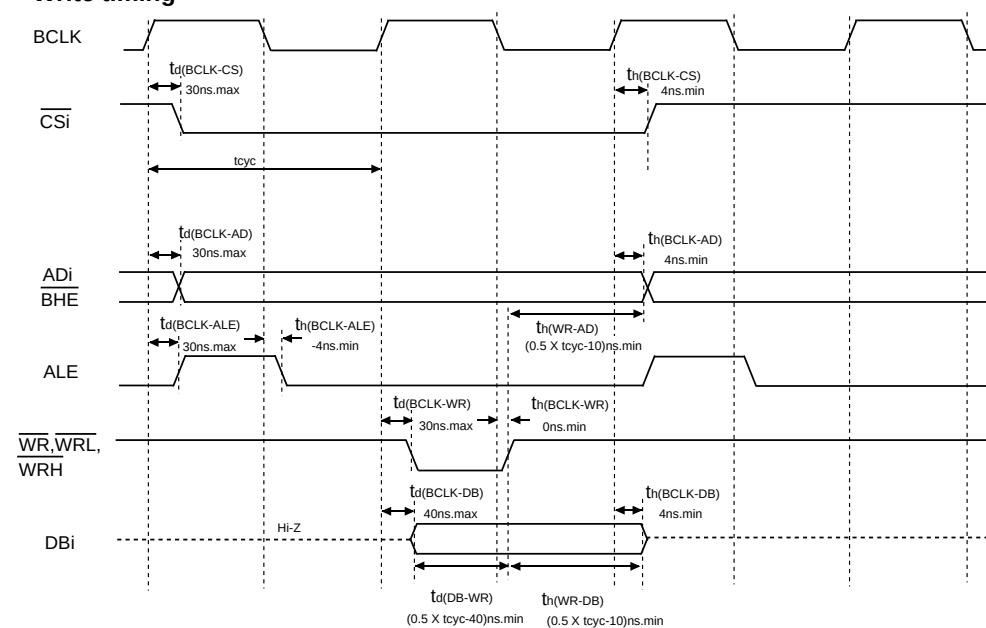
$$V_{CC1} \geq V_{CC2} = 3V$$

Memory Expansion Mode, Microprocessor Mode (for 1-wait setting and external area access)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(\text{BCLK})}$$

Measuring conditions

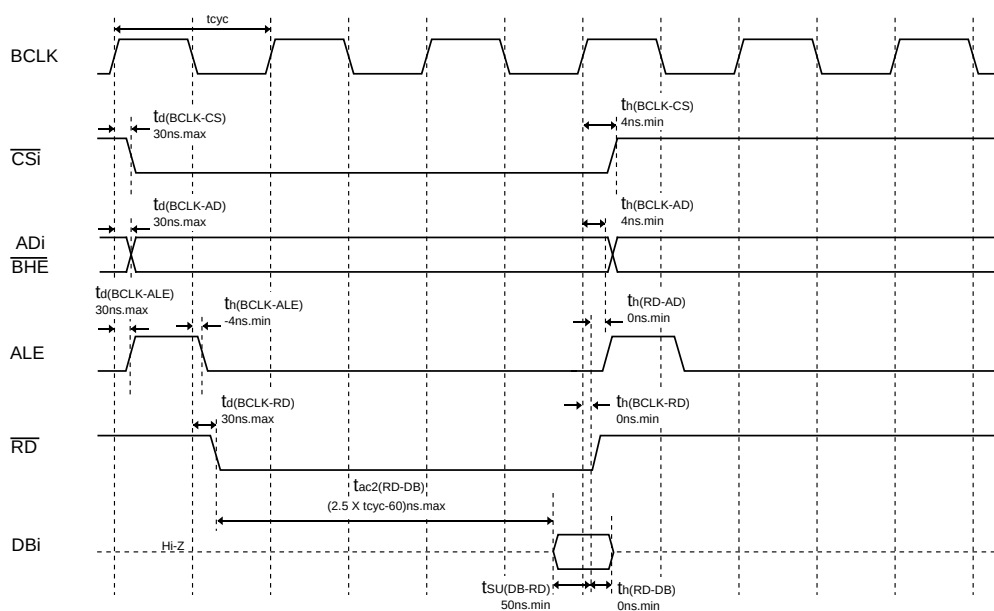
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 1.5.16. Timing Diagram (5)

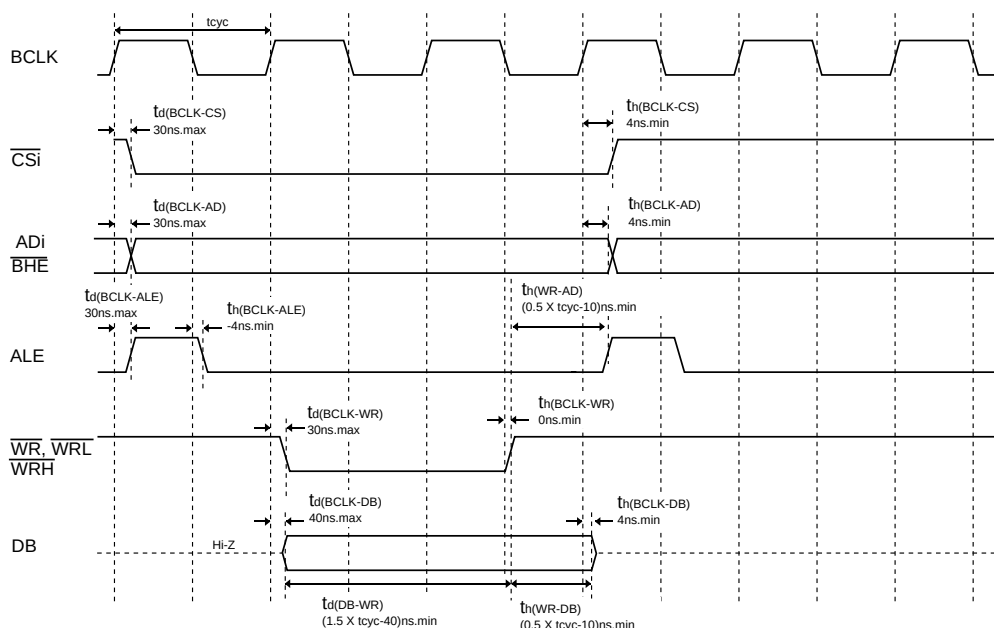
$$V_{CC1} \geq V_{CC2} = 3V$$

Memory Expansion Mode, Microprocessor Mode (for 2-wait setting and external area access)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

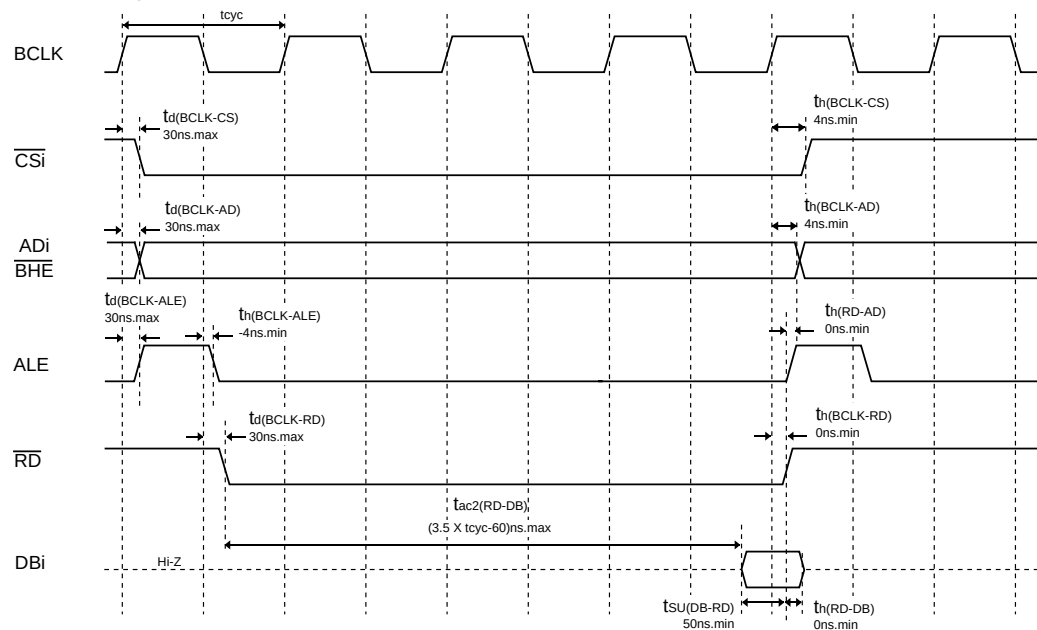
- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

Figure 1.5.17. Timing Diagram (6)

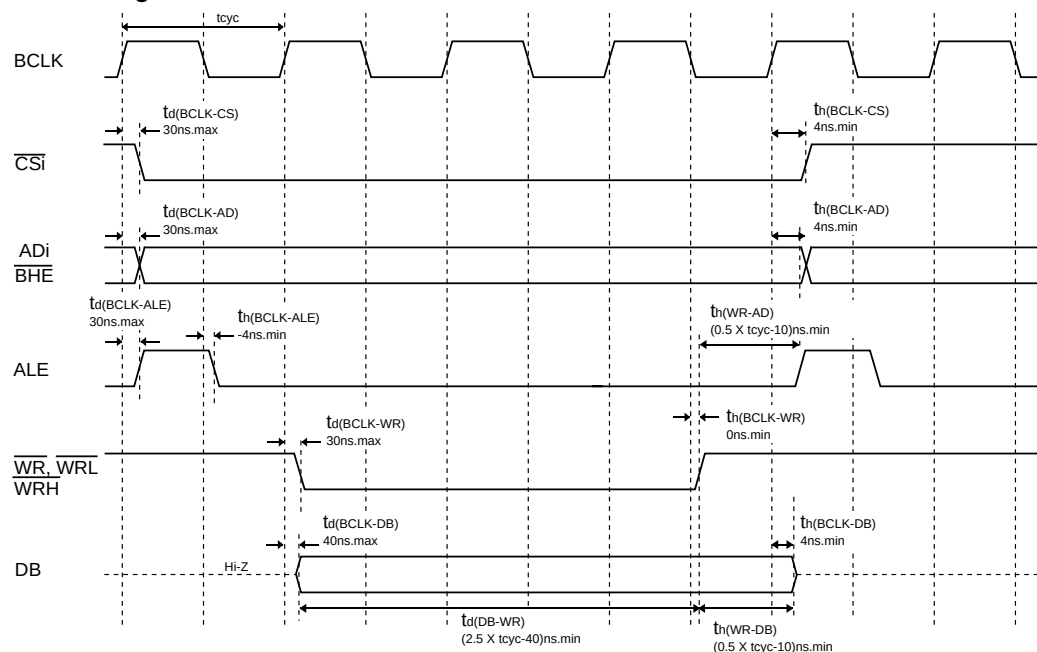
$$V_{CC1} \geq V_{CC2} = 3V$$

Memory Expansion Mode, Microprocessor Mode (for 3-wait setting and external area access)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- Vcc1=Vcc2=3V
- Input timing voltage : VIL=0.6V, VIH=2.4V
- Output timing voltage : VOL=1.5V, VOH=1.5V

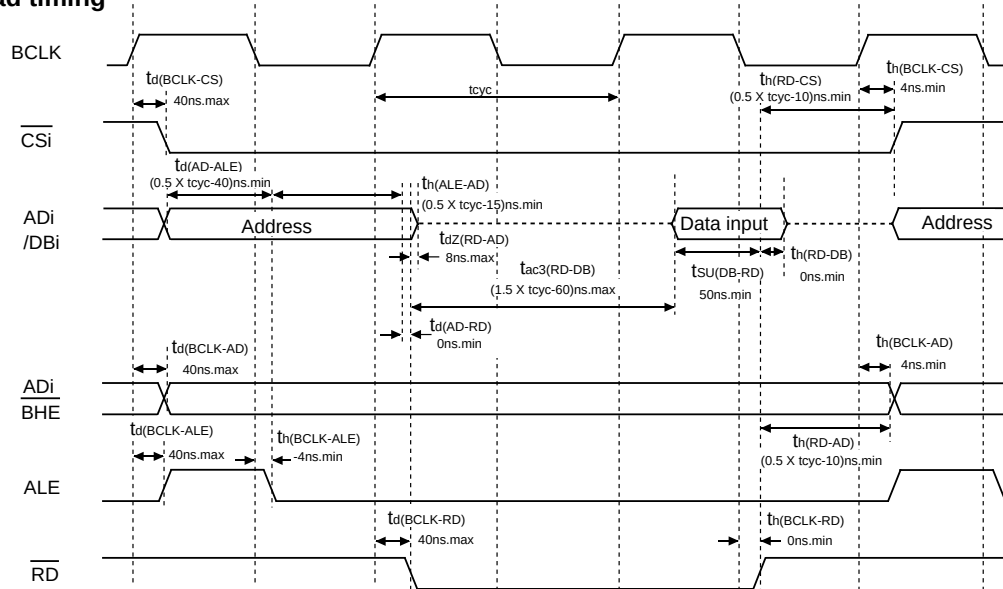
Figure 1.5.18. Timing Diagram (7)

$$V_{CC1} \geq V_{CC2} = 3V$$

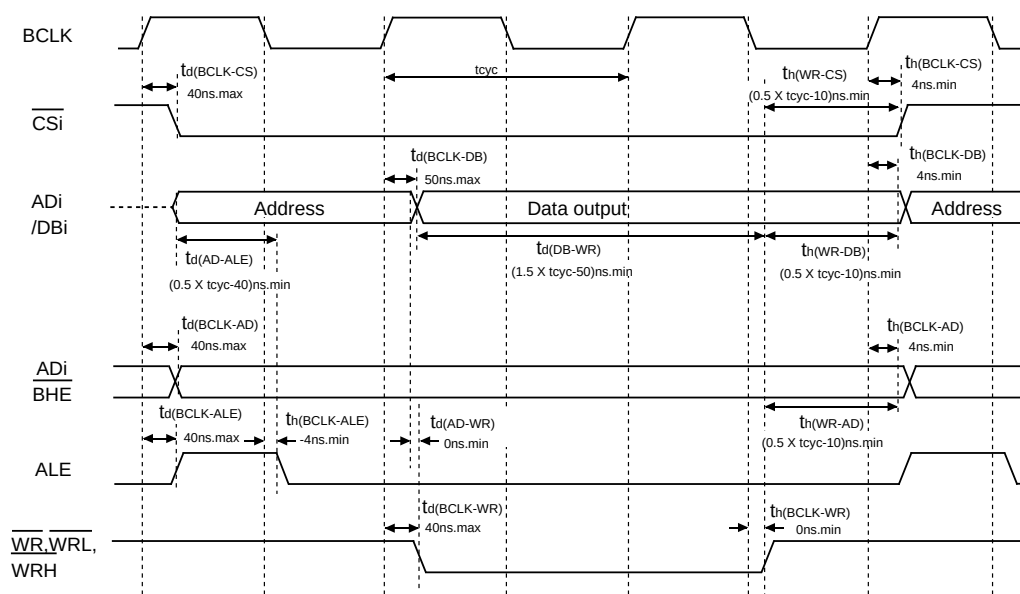
Memory Expansion Mode, Microprocessor Mode

(For 2-wait setting, external area access and multiplex bus selection)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

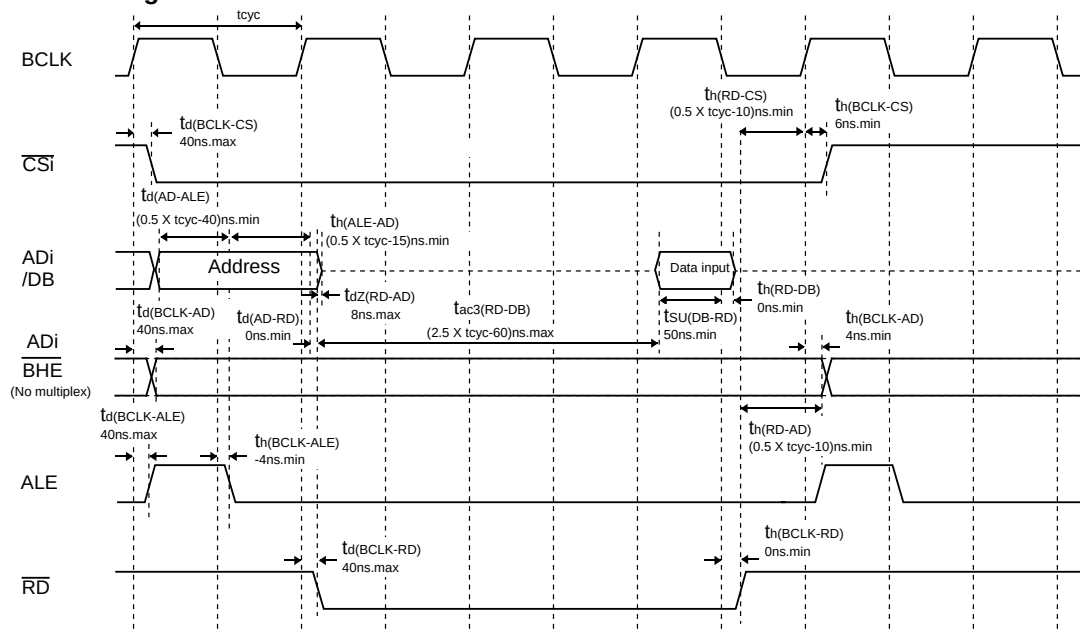
Figure 1.5.19. Timing Diagram (8)

$$V_{CC1} \geq V_{CC2} = 3V$$

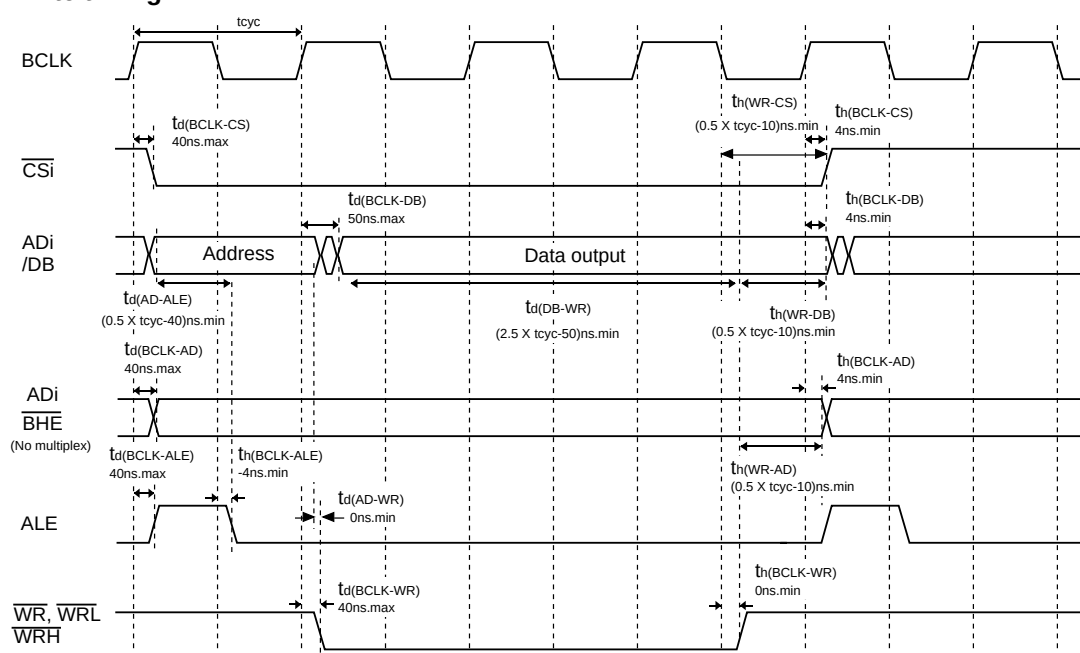
Memory Expansion Mode, Microprocessor Mode

(For 3-wait setting, external area access and multiplex bus selection)

Read timing



Write timing



$$t_{cyd} = \frac{1}{f(BCLK)}$$

Measuring conditions

- Vcc1=Vcc2=3V
- Input timing voltage : VIL=0.6V, VIH=2.4V
- Output timing voltage : VOL=1.5V, VOH=1.5V

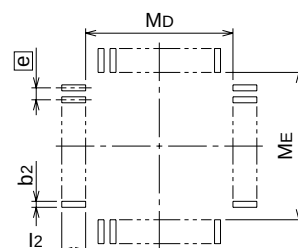
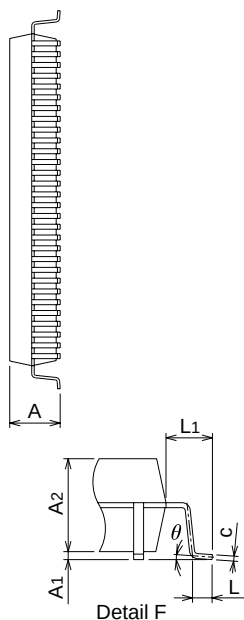
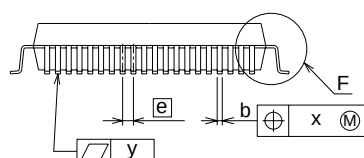
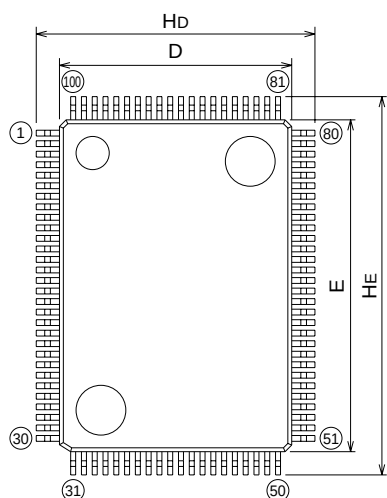
Figure 1.5.20. Timing Diagram (9)

Package Dimensions

100P6S-A (MMP)

Plastic 100pin 14X20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	—	1.58	Alloy 42



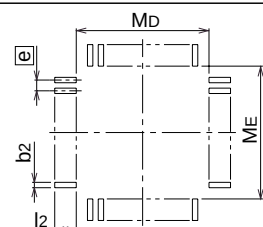
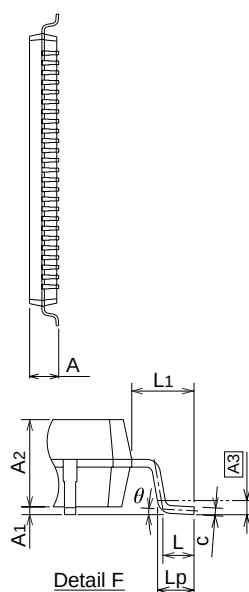
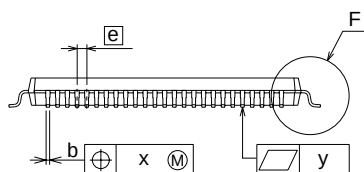
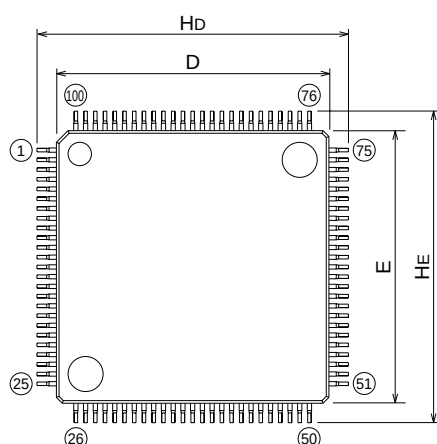
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A1	0	0.1	0.2
A2	—	2.8	—
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	—	0.65	—
Hd	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	—	1.4	—
x	—	—	0.13
y	—	—	0.1
θ	0°	—	10°
b2	—	0.35	—
l2	1.3	—	—
Md	—	14.6	—
ME	—	20.6	—

100P6Q-A (MMP)

Plastic 100pin 14X14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	—	0.63	Cu Alloy



Recommended Mount Pad

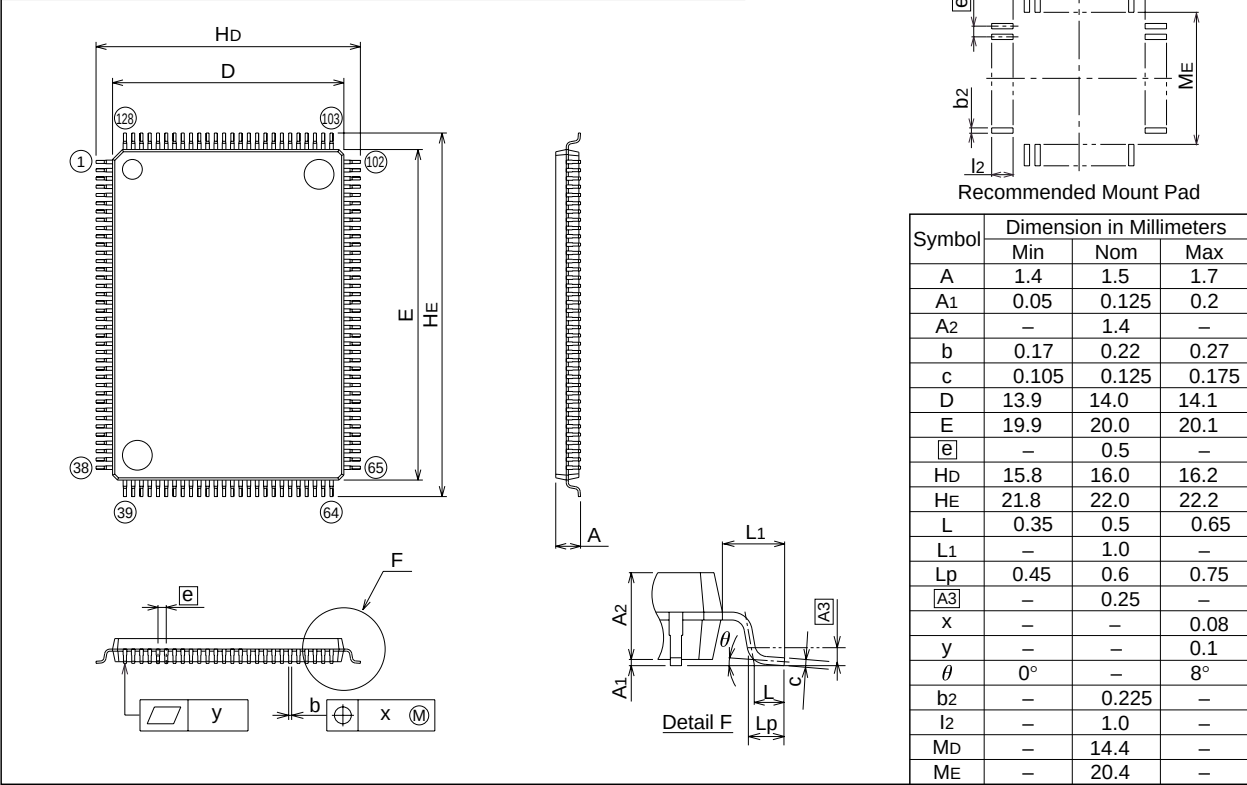
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	—	0.5	—
Hd	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.08
y	—	—	0.1
θ	0°	—	10°
b2	—	0.225	—
l2	0.9	—	—
Md	—	14.4	—
ME	—	14.4	—

128P6Q-A

(MMP)

Plastic 128pin 14X20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP128-P-1420-0.50	—	—	Cu Alloy



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REVISION HISTORY

M16C/62 Group (M16C/62P) Short Sheet / Data Sheet

Rev.	Date	Description	
		Page	Summary
1.10	Apr/XX/Y03 (Continued)	2	Table 1.1.1 is partly revised.
		4-5	Table 1.1.2 and 1.1.3 is partly revised.
		14-19	SFR is partly revised.
			"Note 1" is partly revised.
		22	Table 1.5.3 is partly revised.
		23	Table 1.5.5 is partly revised.
			Table 1.5.6 is added.
		24	Table 1.5.9 is partly revised.
		30	Notes 1 and 2 in Table 1.5.26 is partly revised.
		31	Notes 1 in Table 1.5.27 is partly revised.
		30-31	Note 3 is added to "Data output hold time(refers to BCLK)" in Table 1.5.26 and 1.5.27.
		32	Note 4 is added to "th(ALE-AD)" in Table 1.5.28.
		30-32	Switching Characteristics is partly revised.
		36-39	th(WR-AD) and th(WR-DB) in Figure 1.5.5 to 1.5.8 is partly revised.
		40-41	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.9 to 1.5.10 is partly revised.
		42	Note 2 is added to Table 1.5.29.
		47	Notes 1 and 2 in Table 1.5.45 is partly revised.
		48	Notes 1 in Table 1.5.46 is partly revised.
		47-48	Note 3 is added to "Data output hold time(refers to BCLK)" in Table 1.5.45 and 1.5.46.
		49	Note 4 is added to "th(ALE-AD)" in Table 1.5.47.
		47-49	Switching Characteristics is partly revised.
		53-56	th(WR-AD) and th(WR-DB) in Figure 1.5.15 to 1.5.18 is partly revised.
		57-58	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.19 to 1.5.20 is partly revised.