

54AC11109, 74AC11109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

TI0066—D2957, MARCH 1987—REVISED MARCH 1990

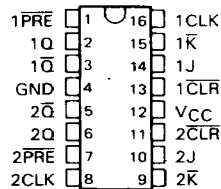
- Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- ESD Protection Exceeds 2000 V, MIL STD-883C Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

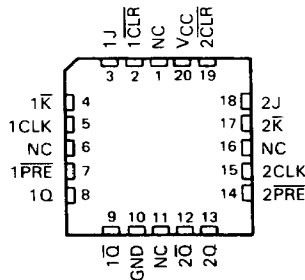
These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and $\bar{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\bar{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\bar{K}$ and tying J high. They also can perform as D-type flip-flops by tying the J and $\bar{K}$ inputs together.

The 54AC11109 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11109 is characterized for operation from -40°C to 85°C.

54AC11109 ... J PACKAGE
74AC11109 ... D OR N PACKAGE
(TOP VIEW)

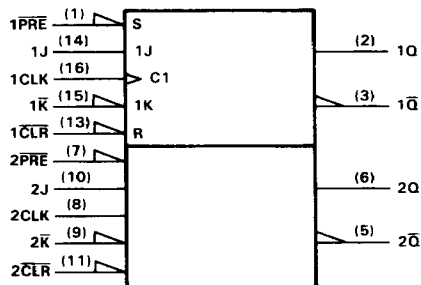


54AC11109 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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FUNCTION TABLE (each gate)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q ₀	$\bar{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q ₀	$\bar{Q}_0$

† This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to the inactive (high) level.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11109			74AC11109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1			2.1			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 5.5$ V	3.85			3.85			
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V			0.9			0.9	V
		$V_{CC} = 4.5$ V			1.35			1.35	
		$V_{CC} = 5.5$ V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3$ V			−4			−4	mA
		$V_{CC} = 4.5$ V			−24			−24	
		$V_{CC} = 5.5$ V			−24			−24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V			12			12	mA
		$V_{CC} = 4.5$ V			24			24	
		$V_{CC} = 5.5$ V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11109		74AC11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
		5.5 V				3.85				
V _{OL}	I _{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
	I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
		5.5 V					1.65			
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	µA
		5.5 V			4		80		40	µA
C _i	V _I = V _{CC} or GND	5 V			3.5					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

PARAMETER			T _A = 25°C		54AC11109		74AC11109		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	70	0	70	0	70	MHz
t _w	Pulse duration	PRE or CLR low	5		5		5		ns
		CLK high or low	7.2		7.2		7.2		
t _{su}	Setup time before CLK ↑	Data high or low	5.5		5.5		5.5		ns
		PRE or CLR inactive	2.5		2.5		2.5		
t _h	Hold time, data after CLK ↑		0		0		0		ns

timing requirements, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER			T _A = 25°C		54AC11109		74AC11109		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	100	0	100	0	100	MHz
t _w	Pulse duration	PRE or CLR low	4		5		4		ns
		CLK high or low	5		5		5		
t _{su}	Setup time before CLK ↑	Data high or low	4.5		4.5		4.5		ns
		PRE or CLR inactive	2		2		2		
t _h	Hold time, data after CLK ↑		0		0		0		ns

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11109		74AC11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			70	100		70		70		MHz
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	1.5	6.5	9	1.5	10.5	1.5	9.9	ns
t_{PHL}			1.5	8	12.6	1.5	14.4	1.5	13.7	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	1.5	8	11.4	1.5	13.5	1.5	12.7	ns
t_{PHL}			1.5	7.5	10.5	1.5	12.7	1.5	11.8	

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11109		74AC11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		100		100		MHz
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	1.5	4.5	6.5	1.5	7.6	1.5	7.1	ns
t_{PHL}			1.5	5	8.6	1.5	10.2	1.5	9.6	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	1.5	5.5	7.9	1.5	9.4	1.5	8.8	ns
t_{PHL}			1.5	5	7.3	1.5	8.6	1.5	8.1	

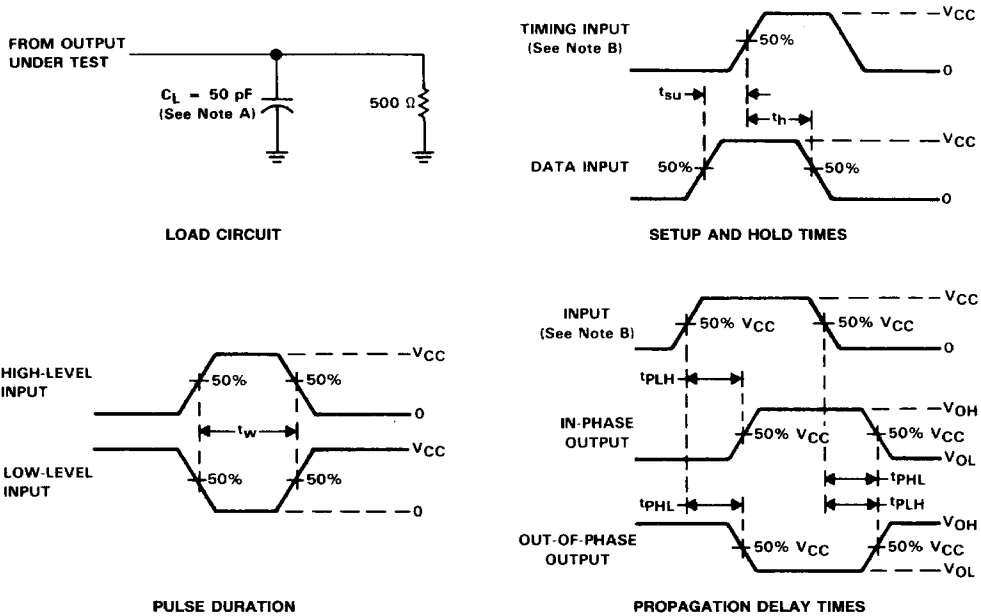
operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	32	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
 For testing pulse duration: $t_r = 1$ to 3 ns, $t_f = 1$ to 3 ns.
 C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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