

FEATURES

- 2:1 PECL/ECL multiplexer
- Guaranteed AC-performance over temperature/voltage
 - >3GHz f_{MAX} (toggle)
 - <200ps rise/fall time
 - <420ps propagation delay (D-to-Q)
- Low jitter performance
 - Random jitter: <1ps_{rms}
 - Deterministic jitter: <15ps_{pp}
 - Total jitter (clock): <1ps_{pp}
- Flexible supply voltage: +3V to +5.5V
- Wide operating temperature range: -40°C to +85°C
- Available in 8-pin MSOP and SOIC packages

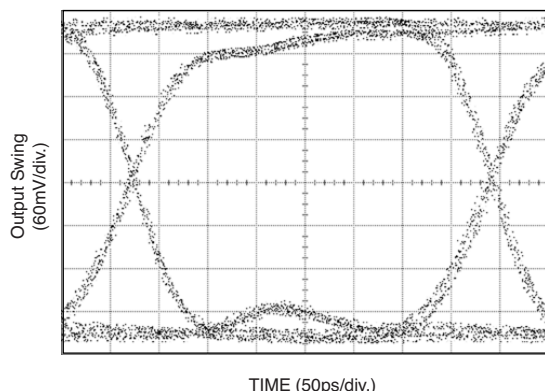
APPLICATIONS

- SONET
- Gig Ethernet
- Fibre Channel
- Transponders

MUX SELECT TRUTH TABLE

SEL1	DATA OUT
L	Db
H	Da

TYPICAL PERFORMANCE



2.7Gbps, $2^{23} - 1$ PRBS



ECL Pro™

DESCRIPTION

The SY10/100EP58V are 3.3V/5V, precision, high-speed, 2:1 multiplexers. Both devices are pin-for-pin, plug-in replacements for the MC10/100EP58D/DT in 8-pin SOIC and 6-pin TSSOP (MSOP) packages. The signal-path inputs (Da and Db) are single-ended PECL/ECL compatible, and can accept a signal swing as low as 150mV. All I/O pins are 10K/100K EP ECL/PECL compatible.

AC-performance is guaranteed over the industrial -40°C to +85°C temperature range and 3.0V to 5.5V supply voltage range. Maximum throughput (f_{MAX}) is guaranteed to be 3GHz with a differential output swing ≥ 400 mV. In addition, these multiplexers are optimized for low-jitter applications. The SY10EP58V and SY100EP58V are designed to operate in either ECL/PECL or PECL/LVPECL mode. The SY100EP58V is internally temperature compensated, thus is 100K EP ECL/PECL compatible—I/O logic levels remain constant over temperature.

The SY10/100EP58V is part of Micrel's high-speed, Precision Edge™ timing and distribution family. For applications that require a differential I/O combination, consult the Micrel website at www.micrel.com, and choose from a comprehensive product line of high-speed, low skew fanout buffers, translators, and clock dividers.

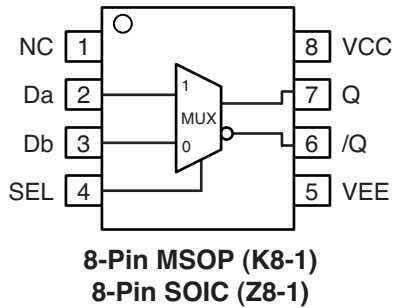
CROSS REFERENCE TABLE

Micrel Semiconductor	On Semiconductor	Package
SY10EP58VZI	MC10EP58D	8-pin SOIC
SY10EP58VZITR	MC10EP58DR2	8-pin SOIC TR ⁽¹⁾
SY10EP58VKI	MC10EP58DT	8-pin MSOP/TSSOP
SY10EP58VKITR	MC10EP58DTR2	8-pin MSOP/TSSOP TR ⁽¹⁾
SY100EP58VZI	MC100EP58D	8-pin SOIC
SY100EP58VZITR	MC100EP58DR2	8-pin SOIC TR ⁽¹⁾
SY100EP58VKI	MC100EP58DT	8-pin MSOP/TSSOP
SY100EP58VKITR	MC100EP58DTR2	8-pin MSOP/TSSOP TR ⁽¹⁾

Note:

1. Tape and Reel.

PACKAGE/ORDERING INFORMATION

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10EP58VZI	Z8-1	Industrial	HEP58V	Sn-Pb
SY10EP58VZITR ⁽²⁾	Z8-1	Industrial	HEP58V	Sn-Pb
SY100EP58VZI	Z8-1	Industrial	EP58V	Sn-Pb
SY100EP58VZITR ⁽²⁾	Z8-1	Industrial	EP58V	Sn-Pb
SY10EP58VKI	K8-1	Industrial	HP58	Sn-Pb
SY10EP58VKITR ⁽²⁾	K8-1	Industrial	HP58	Sn-Pb
SY100EP58VKI	K8-1	Industrial	XP58	Sn-Pb
SY100EP58VKITR ⁽²⁾	K8-1	Industrial	XP58	Sn-Pb
SY10EP58VZG ⁽³⁾	Z8-1	Industrial	HEP58V with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY10EP58VZGTR ^(2, 3)	Z8-1	Industrial	HEP58V with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EP58VZG ⁽³⁾	Z8-1	Industrial	XEP58V with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EP58VZGTR ^(2, 3)	Z8-1	Industrial	XEP58V with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY10EP58VKG ⁽³⁾	K8-1	Industrial	HP58 with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY10EP58VKGTR ^(2, 3)	K8-1	Industrial	HP58 with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EP58VKG ⁽³⁾	K8-1	Industrial	XP58 with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EP58VKGTR ^(2, 3)	K8-1	Industrial	XP58 with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1	NC	No connect.
2, 3	Da, Db ⁽¹⁾	100KEP PECL/ECL single-ended input channels a and b. Multiplexing of these inputs are controlled by SEL. The signal inputs include internal 75k Ω pull-down resistors. Default condition is LOW when left floating. The input signal should be terminated externally. See "Termination Recommendations" section.
4	SEL	100KEP PECL/ECL compatible 2:1 mux select control. See "Mux Select Truth Table." Enable pin includes an internal 75k Ω pull-down resistor. Default condition is LOW.
5	VEE	Negative Power Supply: For PECL/LVPECL connect to ground. Both V_{EE} pins must be connected together, externally on the PCB, for proper operation.
6, 7	/Q, Q	100KEP PECL/ECL compatible differential output. PECL/ECL termination is with a 50 Ω resistor to $V_{CC} - 2V$. Unused single-ended outputs must have a balanced load. For AC-coupled applications, the output stage emitter follower must have a DC current path to ground. See "Termination Recommendations" section.
8	VCC	Positive Power Supply. All V_{CC} pins must be connected to the same power supply externally. Bypass with 0.1 μF /0.01 μF low ESR capacitors.

Note:

1. If the inputs are AC-coupled, the outputs Q, and /Q will experience duty cycle distortion because the input levels do not track the internal reference voltage.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{IN})	–6.0V to 0V
Output Current (I_{OUT})	
Continuous	50mA
Surge	100mA
Lead Temperature (Soldering, 20sec.)	+260°C
Storage Temperature (T_S)	–65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage $ V_{CC}-V_{EE} $	+3.0V to +5.5V
Ambient Temperature (T_A)	–40°C to +85°C
Package Thermal Resistance	
MSOP (θ_{JA})	
Still-air	206°C/W
500lfpm	155°C/W
SOIC (θ_{JA})	
Still-air	160°C/W
500lfpm	109°C/W
MSOP (θ_{JC})	39°C/W
SOIC (θ_{JC})	39°C/W

DC ELECTRICAL CHARACTERISTICS⁽³⁾

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Power Supply Voltage										V	
	(PECL)	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5		
	(LVPECL)	3.0	—	3.8	3.0	—	3.8	3.0	—	3.8		
	(ECL)	–5.5	–5.0	–4.5	–5.5	–5.0	–4.5	–5.5	–5.0	–4.5		
	(LVECL)	–3.8	–3.3	–3.0	–3.8	–3.3	–3.0	–3.8	–3.3	–3.0		
I_{EE}	Supply Current	—	35	50	—	35	50	—	35	50	mA	No Load
I_{IH}	Input HIGH Current	—	—	75	—	—	75	—	—	80	μA	$V_{IN} = V_{IH}$
I_{IL}	Input LOW Current											
	All Inputs	0.5	—	—	0.5	—	—	0.5	—	—	μA	$V_{IN} = V_{IL}$
C_{IN}	Input Capacitance (MSOP)	—	—	—	—	1.0	—	—	—	—	pF	
	(SOIC)	—	—	—	—	1.0	—	—	—	—	pF	

10K DC ELECTRICAL CHARACTERISTICS⁽³⁾

$V_{CC} = 3.0\text{V to } 5.5\text{V}$; $V_{EE} = 0\text{V}^{(4)}$ $V_{CC} = 0\text{V or } V_{EE} = -5.5\text{V to } -3.0\text{V}$.

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current ⁽⁵⁾	—	—	40	—	30	40	—	—	40	mA
V_{OH}	Output HIGH Voltage ⁽⁶⁾	–1135	—	–0885	–1070	–0945	–0820	–1010	—	–0760	mV
V_{OL}	Output LOW Voltage ⁽⁶⁾	–1935	—	–1685	–1870	–1745	–1620	–1810	—	–1560	mV
V_{IH}	Input HIGH Voltage	–1210	—	–0885	–1145	—	–0820	–1085	—	–0760	mV
V_{IL}	Input LOW Voltage	–1935	—	–1610	–1870	—	–1545	–1810	—	–1485	mV
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA
I_{IL}	Input LOW Current	D	0.5	—	0.5	—	—	0.5	—	—	μA

Notes:

- Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
- The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- 10KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
- Input and output parameters vary 1:1 with V_{CC} .
- $V_{CC} = 0\text{V}$, $V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$, all other pins floating.
- All loading with 50Ω to $V_{CC} - 2.0\text{V}$.

(100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS⁽⁷⁾ $V_{CC} = +3.3V \pm 10\%$, $V_{EE} = 0V$.

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	1355	—	1675	1355	—	1675	1355	—	1675	mV	
V_{IH}	Input HIGH Voltage (Single-Ended)	2075	—	2420	2075	—	2420	2075	—	2420	mV	
V_{OL}	Output LOW Voltage	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV	50Ω to $V_{CC}-2V$
V_{OH}	Output HIGH Voltage	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV	50Ω to $V_{CC}-2V$
V_{BB}	Output Reference Voltage	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV	
V_{IHCMR}	Input HIGH Voltage ⁽⁸⁾ Common Mode Range	2.0	—	V_{CC}	2.0	—	V_{CC}	2.0	—	V_{CC}	V	

(100KEP) PECL DC ELECTRICAL CHARACTERISTICS⁽⁷⁾ $V_{CC} = +5.0V \pm 10\%$, $V_{EE} = 0V$.

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	3055	—	3375	3055	—	3375	3055	—	3375	mV	
V_{IH}	Input HIGH Voltage (Single-Ended)	3775	—	4120	3775	—	4120	3775	—	4120	mV	
V_{OL}	Output LOW Voltage	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV	50Ω to $V_{CC}-2V$
V_{OH}	Output HIGH Voltage	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV	50Ω to $V_{CC}-2V$
V_{BB}	Output Reference Voltage	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV	
V_{IHCMR}	Input HIGH Voltage ⁽⁸⁾ Common Mode Range	2.0	—	V_{CC}	2.0	—	V_{CC}	2.0	—	V_{CC}	V	

(100KEP) ECL/LVECL DC ELECTRICAL CHARACTERISTICS⁽⁷⁾ $V_{CC} = 0V$, $V_{EE} = -5.5V$ to $-3.0V$.

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage	-1945	—	-1625	-1945	—	-1625	-1945	—	-1625	mV	
V_{IH}	Input HIGH Voltage	-1225	—	-880	-1225	—	-880	-1225	—	-880	mV	
V_{OL}	Output LOW Voltage	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV	50Ω to $V_{CC}-2V$
V_{OH}	Output HIGH Voltage	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV	50Ω to $V_{CC}-2V$
V_{BB}	Output Reference Voltage	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV	
V_{IHCMR}	Input HIGH Voltage ⁽⁸⁾ Common Mode Range	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	V	

Notes:

- 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
- The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC ELECTRICAL CHARACTERISTICS

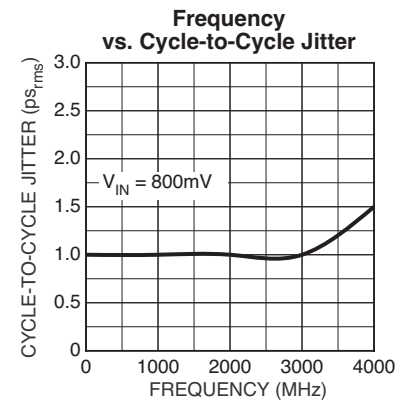
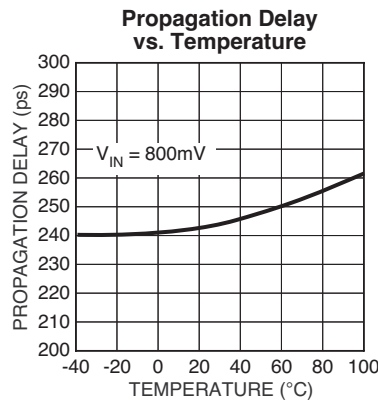
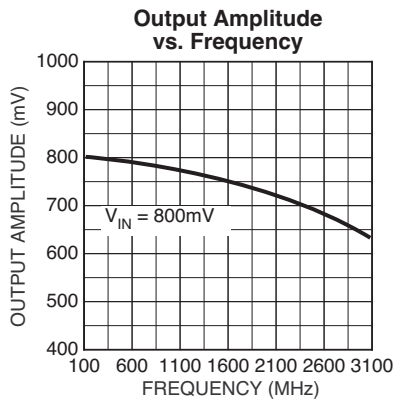
$V_{CC} = 3.0V$ to $5.5V$, $V_{EE} = 0V$ or $V_{CC} = 0V$; $V_{EE} = -3.0V$ to $-5.5V$.

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Toggle Frequency ⁽¹⁾	3	—	—	3	—	—	3	—	—	GHz	
t_{PLH} t_{PHL}	Propagation Delay (Differential) SEL to Q, /Q; D to Q, /Q	170	—	380	190	230	410	210	—	420	ps	
t_{SKEW}	Part-to-Part Skew ⁽²⁾	—	—	200	—	—	200	—	—	200	ps	
t_{JITTER}	Cycle-to-Cycle Jitter (rms) ⁽³⁾	—	0.2	<1	—	0.2	<1	—	0.2	<1	ps _{pp}	
	Random Jitter ⁽⁴⁾	—	—	—	—	—	<1	—	—	—	ps _{pp}	Note 3
	Deterministic Jitter ⁽⁵⁾	—	—	—	—	7	<15	—	—	—	ps _{pp}	Note 4
	@ 1.25Gbps	—	—	—	—	10	<25	—	—	—	ps _{pp}	Note 4
	@ 2.5Gbps	—	—	—	—	10	<25	—	—	—	ps _{pp}	Note 4
	Total Jitter ⁽⁶⁾	—	<1	—	—	<1	—	—	<1	—	ps _{pp}	
V_{IN}	Differential Input Voltage Range	150	800	1200	150	800	1200	150	800	1200	mV	
t_r, t_f	Output Rise/Fall Time Q, /Q (20% to 80%)	—	—	170	—	140	180	—	—	200	ps	

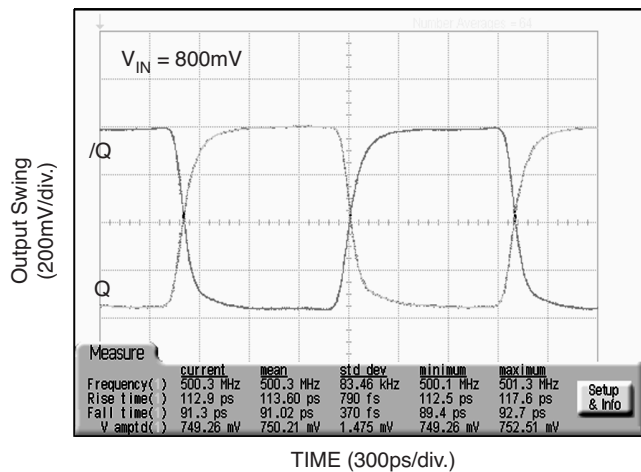
Notes:

1. Measured with 750mV input signal, 50% duty cycle. Output swing $\geq 400mV$. All loading with a 50Ω to $V_{CC} - 2.0V$.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
3. The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER_CC} = t_n - t_{n-1} + 1$, where t is the time between rising edges of the output signal.
4. Random jitter is measured with a K28.7 comma detect character pattern, measured at 1.25Gbps and 2.5Gbps.
5. Deterministic jitter is measured at 1.25Gbps and 2.5Gbps, with both K28.5 and $2^{23}-1$ PRBS pattern.
6. Total Jitter is defined as an ideal clock input, no more than 1 output edge in 10^{12} output edges will deviate by more than specified peak-to-peak jitter value.

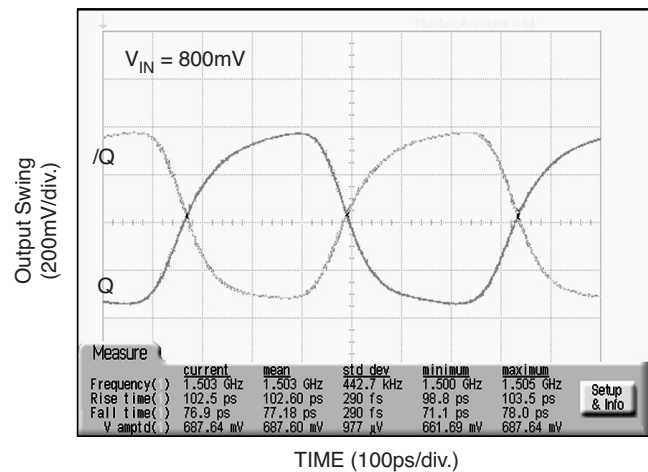
TYPICAL OPERATING CHARACTERISTICS

Conditions: $V_{CC} = 3.3V$, $V_{EE} = GND$, $T_A = 25^\circ C$, unless otherwise stated.

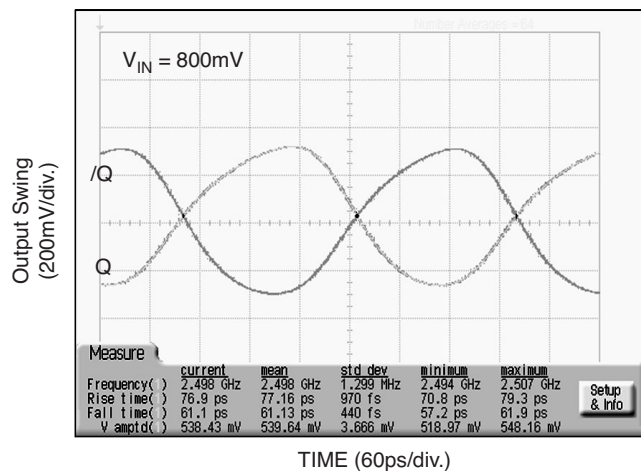
500MHz Output



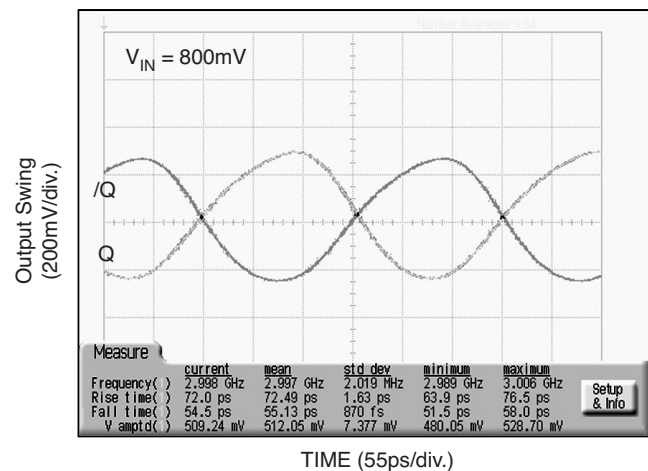
1.5GHz Output



2.5GHz Output



3.0GHz Output



TERMINATION RECOMMENDATIONS

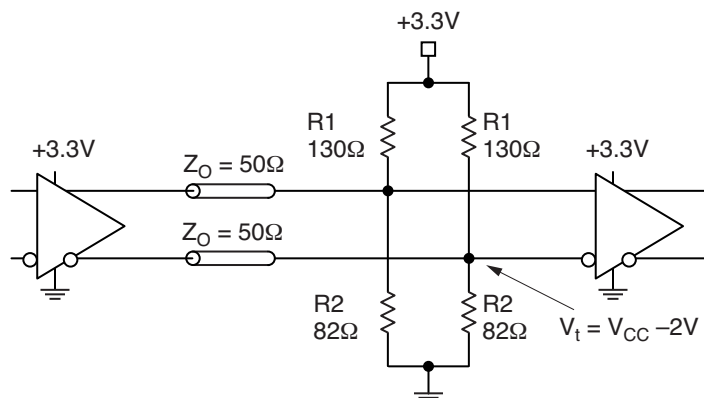


Figure 1. Parallel Termination-Thevenin Equivalent

Note:

1. For +5.0V systems: $R_1 = 82\Omega$, $R_2 = 130\Omega$.

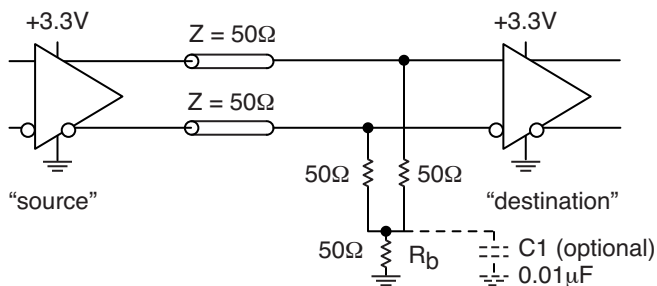
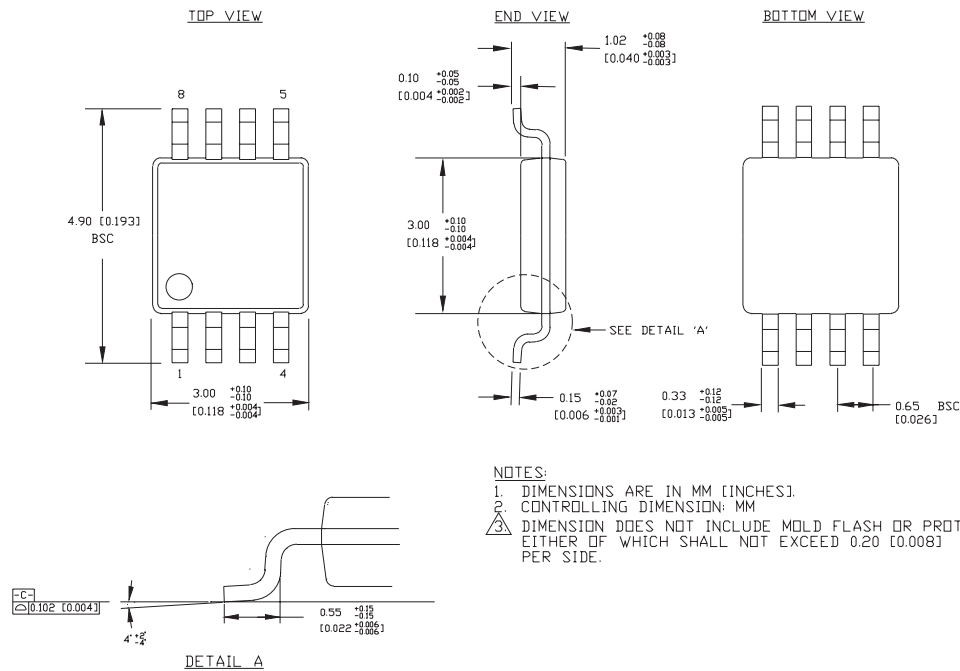


Figure 2. Three-Resistor "Y-Termination"

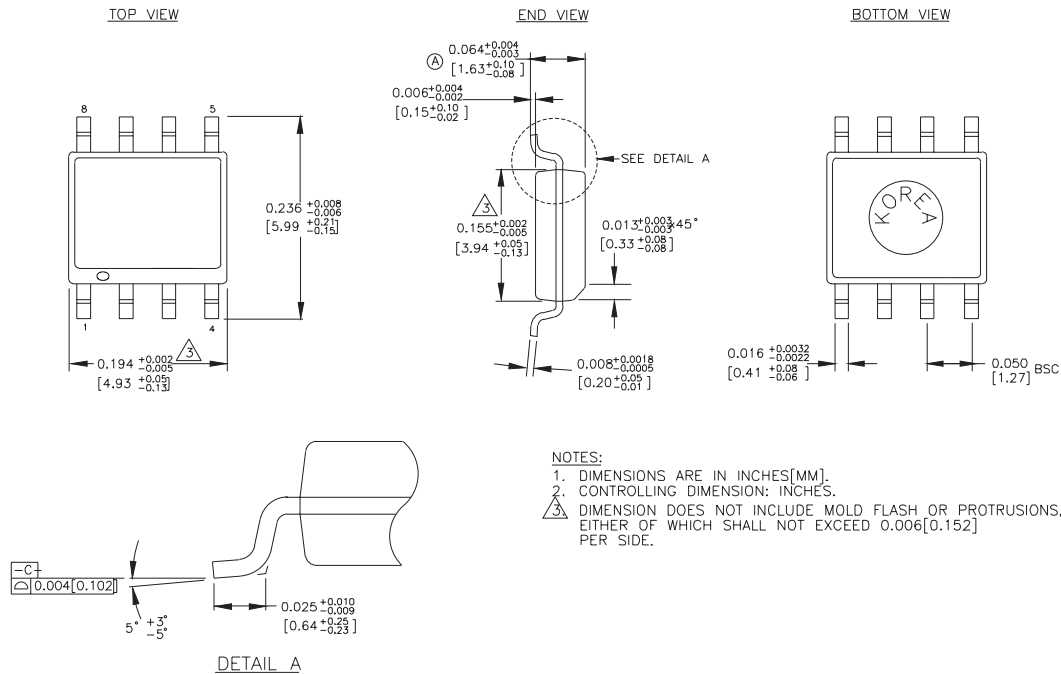
Notes:

1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_T . For +3.3V systems $R_b = 46\Omega$ to 50Ω . For +5V systems, $R_b = 110\Omega$.

8 LEAD MSOP (K8-1)



Rev. 01

8 LEAD SOIC (Z8-1)

Rev. 03

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