

### PROTECTION PRODUCTS

#### Description

The SMDAxxC-8 series of transient voltage suppressors are designed to protect components which are connected to data and transmission lines from voltage surges caused by ESD (electrostatic discharge), EFT (electrical fast transients), and lightning.

TVS diodes are characterized by their high surge capability, low operating and clamping voltages, and fast response time. This makes them ideal for use as board level protection of sensitive semiconductor components. The SMDAxxC-8 is designed to provide transient suppression on multiple data lines and I/O ports. The low profile SO-14 design allows the user to protect up to eight data and I/O lines with one package. They are bidirectional device and may be used on lines where the normal operating voltage is above and below ground (i.e. -12V to +12V).

The SMDAxxC-8 TVS diode array will meet the surge requirements of IEC 61000-4-2 (Formerly IEC 801-2), Level 4, "Human Body Model" for air and contact discharge.

#### Features

- ◆ Transient protection for data lines to  
**IEC 61000-4-2 (ESD) 15kV (air), 8kV (contact)**  
**IEC 61000-4-4 (EFT) 40A (5/50ns)**  
**IEC 61000-4-5 (Lightning) 12A (8/20μs)**
- ◆ Small SO-14 surface mount package
- ◆ Protects eight I/O lines
- ◆ Working voltages: 5V, 12V, 15V and 24V
- ◆ Low leakage current
- ◆ Low operating and clamping voltages
- ◆ Solid-state silicon avalanche technology

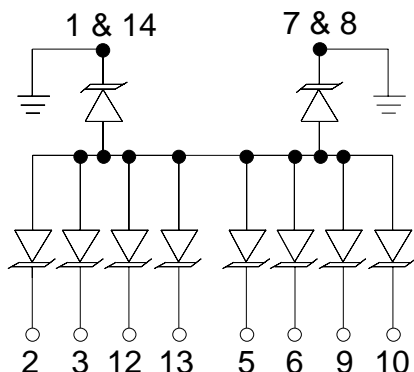
#### Mechanical Characteristics

- ◆ JEDEC SO-14 package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Part Number, Logo, Date Code
- ◆ Packaging : Tape and Reel per EIA 481

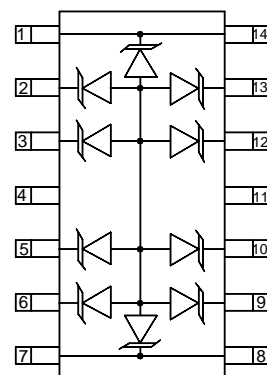
#### Applications

- ◆ RS-232 & RS-422 Data Lines
- ◆ Microprocessor Based Equipment
- ◆ LAN/WAN Equipment
- ◆ Set-Top Box
- ◆ Notebooks, Desktops, & Servers
- ◆ Portable Instrumentation
- ◆ Peripherals
- ◆ Serial and Parallel Ports

#### Circuit Diagram



#### Schematic & PIN Configuration



**SO-14 (Top View)**

**PROTECTION PRODUCTS**
**Absolute Maximum Rating**

Rating	Symbol	Value	Units
Peak Pulse Power ( $t_p = 8/20\mu s$ )	$P_{pk}$	300	Watts
Lead Soldering Temperature	$T_L$	260 (10 sec.)	°C
Operating Temperature	$T_J$	-55 to +125	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

**Electrical Characteristics**

<b>SMDA05C-8</b>						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	$V_{RWM}$				5	V
Reverse Breakdown Voltage	$V_{BR}$	$I_t = 1mA$	6			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 5V, T=25^\circ C$			20	$\mu A$
Clamping Voltage	$V_C$	$I_{PP} = 1A, t_p = 8/20\mu s$			9.8	V
Maximum Peak Pulse Current	$I_{PP}$	$t_p = 8/20\mu s$			17	A
Junction Capacitance	$C_J$	Between I/O Pins and Gnd $V_R = 0V, f = 1MHz$			350	pF

<b>SMDA12C-8</b>						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	$V_{RWM}$				12	V
Reverse Breakdown Voltage	$V_{BR}$	$I_t = 1mA$	13.3			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 12V, T=25^\circ C$			1	$\mu A$
Clamping Voltage	$V_C$	$I_{PP} = 1A, t_p = 8/20\mu s$			19	V
Maximum Peak Pulse Current	$I_{PP}$	$t_p = 8/20\mu s$			12	A
Junction Capacitance	$C_J$	Between I/O Pins and Gnd $V_R = 0V, f = 1MHz$			120	pF

**PROTECTION PRODUCTS**
**Electrical Characteristics (Continued)**

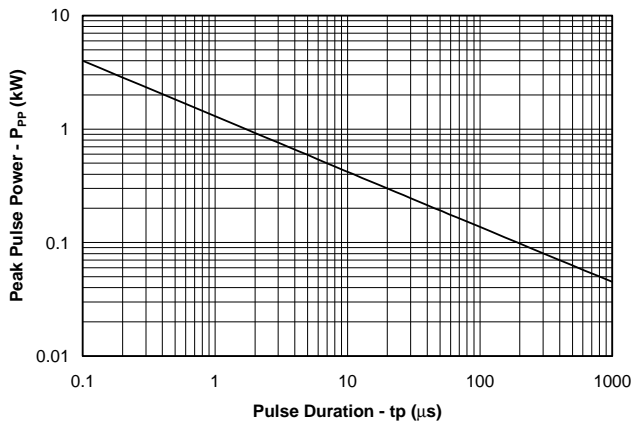
<b>SMDA15C-8</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Conditions</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Units</b>
Reverse Stand-Off Voltage	$V_{RWM}$				15	V
Reverse Breakdown Voltage	$V_{BR}$	$I_t = 1mA$	16.7			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 15V, T=25^{\circ}C$			1	$\mu A$
Clamping Voltage	$V_C$	$I_{PP} = 1A, t_p = 8/20\mu s$			24	V
Maximum Peak Pulse Current	$I_{PP}$	$t_p = 8/20\mu s$			10	A
Junction Capacitance	$C_j$	Between I/O Pins and Gnd $V_R = 0V, f = 1MHz$			75	pF

<b>SMDA24C-8</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Conditions</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Units</b>
Reverse Stand-Off Voltage	$V_{RWM}$				24	V
Reverse Breakdown Voltage	$V_{BR}$	$I_t = 1mA$	26.7			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 24V, T=25^{\circ}C$			1	$\mu A$
Clamping Voltage	$V_C$	$I_{PP} = 1A, t_p = 8/20\mu s$			43	V
Maximum Peak Pulse Current	$I_{PP}$	$t_p = 8/20\mu s$			5	A
Junction Capacitance	$C_j$	Between I/O Pins and Gnd $V_R = 0V, f = 1MHz$			50	pF

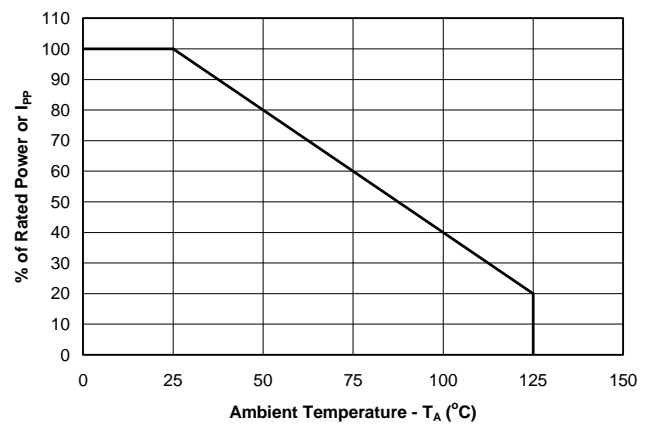
## PROTECTION PRODUCTS

### Typical Characteristics

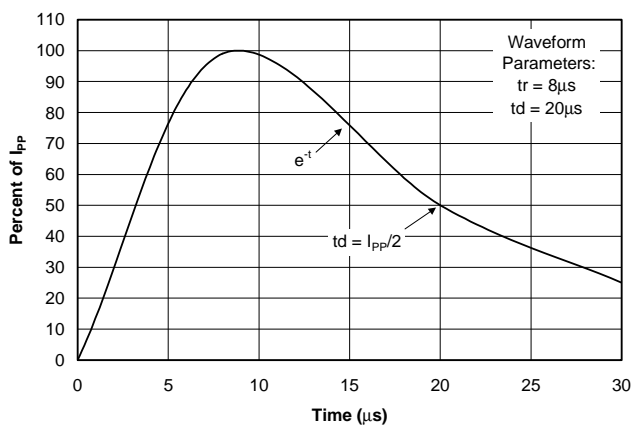
**Non-Repetitive Peak Pulse Power vs. Pulse Time**



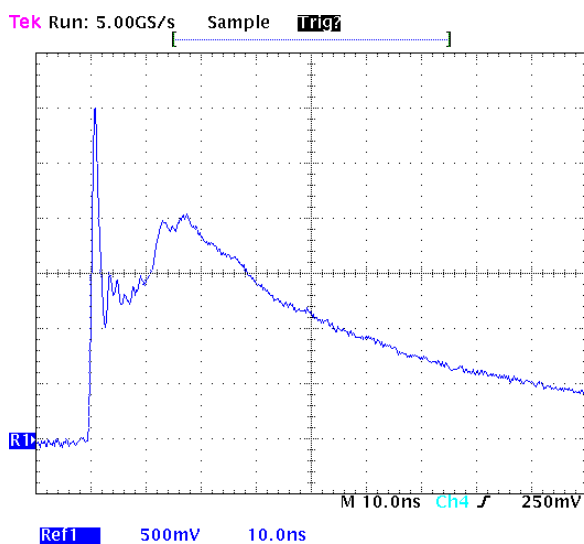
**Power Derating Curve**



**Pulse Waveform**



**ESD Pulse Waveform (IEC 61000-4-2)**



**IEC 61000-4-2 Discharge Parameters**

Level	First Peak Current (A)	Peak Current at 30 ns (A)	Peak Current at 60 ns (A)	Test Voltage (Contact Discharge) (kV)	Test Voltage (Air Discharge) (kV)
1	7.5	4	8	2	2
2	15	8	4	4	4
3	22.5	12	6	6	8
4	30	16	8	8	15

## PROTECTION PRODUCTS

### Applications Information

#### Device Connection for Protection of Eight Data Lines

The SMDAxxC-8 is designed to protect up to 8 data or I/O lines. They are bidirectional devices and may be used on lines where the signal polarities are above and below ground.

The SMDAxxC-8 TVS arrays employ a monolithic structure. Therefore, the working voltage ( $V_{RWM}$ ) and breakdown voltage ( $V_{BR}$ ) specifications apply to the differential voltage between any two data line pins. For example, the SMDA24C-8 is designed for a maximum voltage excursion of +/-12V between any two data lines.

The device is connected as follows:

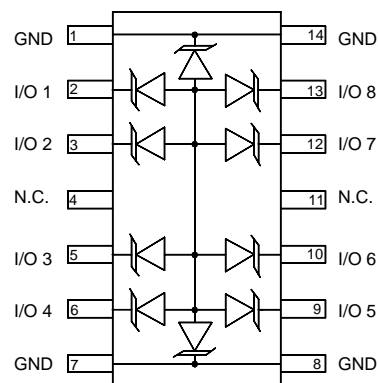
- Pins 2, 3, 5, 6, 9, 10, 12 and 13 are connected to the lines that are to be protected. Pins 1, 7, 8, and 14 are connected to ground. The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces. Pins 4 and 11 are not connected.

#### Circuit Board Layout Recommendations for Suppression of ESD.

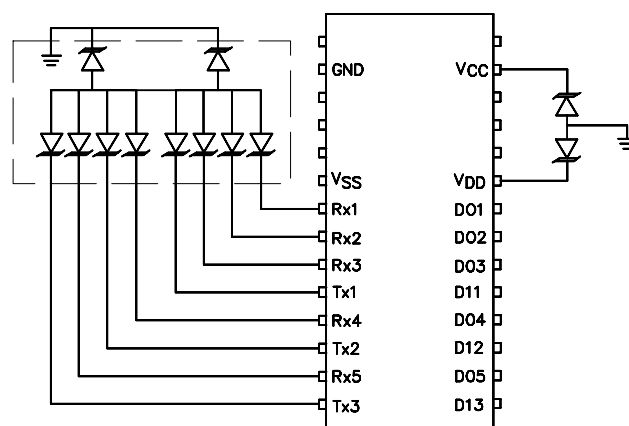
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

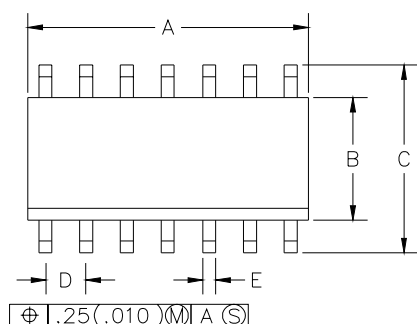
- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

**Circuit Diagram**

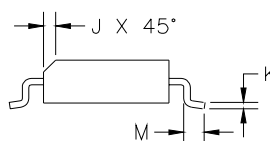
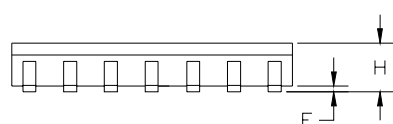


**Connection Diagram**

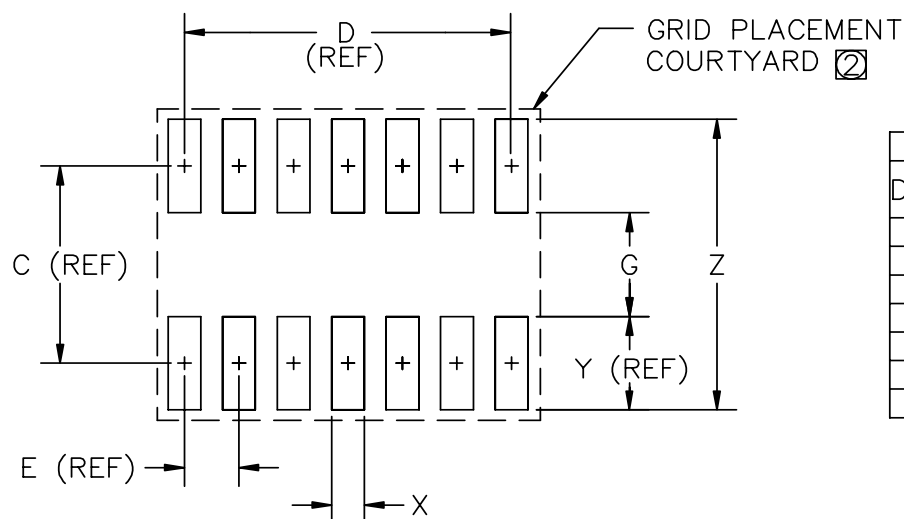


**PROTECTION PRODUCTS**
**Outline Drawing - SO-14**


DIM <sup>N</sup>	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.337	.344	8.55	8.75	2
B	.150	.158	3.80	4.00	3
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.010	.020	0.25	0.50	
K	.007	.010	.19	.25	
M	.016	.050	0.40	1.27	



- ③ DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25 mm (.010") PER SIDE.
- ② DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15 mm (.010") PER SIDE.
- ① CONTROLLING DIMENSION : MILLIMETER

**Land Pattern - SO-14**


DIM <sup>N</sup>	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.19	—	5.00	—
D	—	.30	—	7.62	—
E	—	.05	—	1.27	—
G	.10	.11	2.60	2.80	—
X	.02	.03	.60	.80	—
Y	—	.09	—	2.40	—
Z	—	.29	7.20	7.40	—

- ② GRID PLACEMENT COURTYARD IS 20x16 ELEMENTS (10mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

- ① CONTROLLING DIMENSION: MILLIMETERS

**PROTECTION PRODUCTS****Ordering Information**

<b>Part Number</b>	<b>Working Voltage</b>	<b>Qty per Reel</b>	<b>Reel Size</b>
SMDA05C-8.TE	5V	2,500	13 Inch
SMDA12C-8.TE	12V	2,500	13 Inch
SMDA15C-8.TE	15V	2,500	13 Inch
SMDA24C-8.TE	24V	2,500	13 Inch

Note:

(1) No suffix indicates tube pack.

**Contact Information**

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