W81C280

USB Keyboard/ Device Controller

W81C280 Data Sheet Correction Table

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Winbond Electronics Corp.

USB Keyboard/ Device Controller

1. GENERAL DESCRIPTION

W81C280 is a single-chip microcontroller with Universal Serial Bus (USB) interface for keyboard application, it includes the core of Winbond's 8-bit microprocessor W78C52. It implements a standard PC keyboard and enables connection to host system through low- speed (1.5Mhz) or high speed(12Mhz) . It complies with USB Specification Revision 1.0 and HID Class Definition Revision 1.0.

W81C280 supports an 18 X 8 keyboard scan matrix wihich allows suspend wakeup, and also provides a port for PS/2 mouse. It consists of an 8051 compatible CPU core, a 6K-byte ROM, a 256-byte SRAM, and three 16-bit programmable timers.

W81C280 supports one device address and five endpoints, one for Control transfer and four for Interrupt transfer. Through modification of firmware of W78C52, it can be used for multi-function device design, such as USB-IR receiver and any High-Speed(12Mhz)/Slow-Speed(1.5Mhz) USB peripheral device controller.

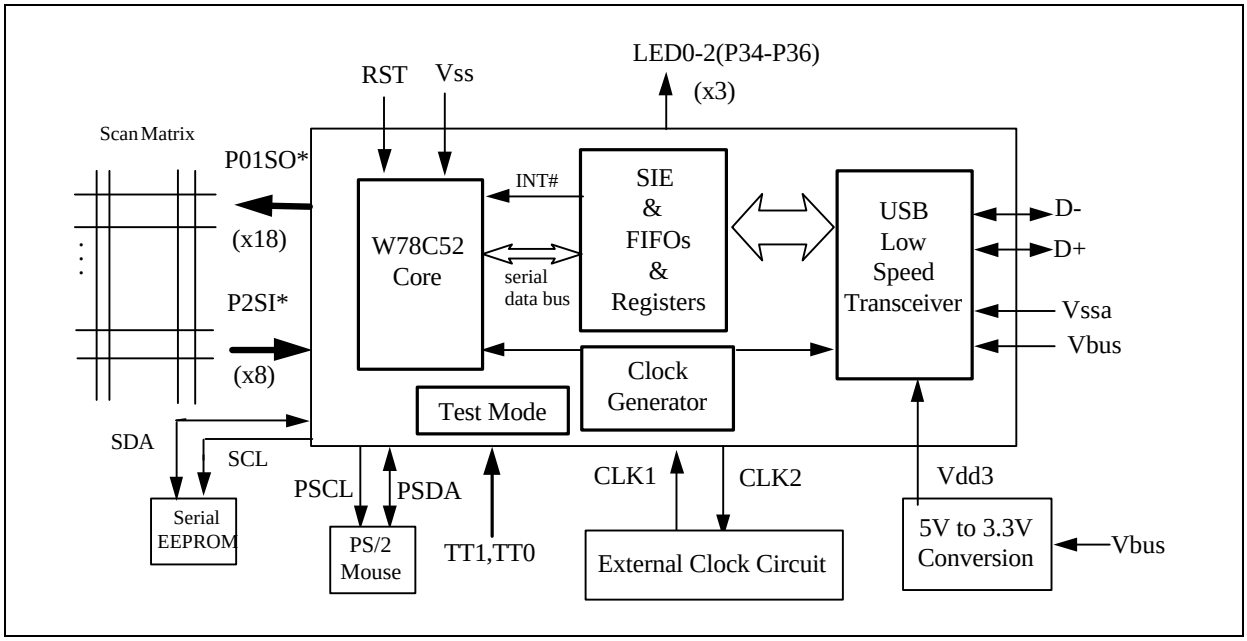
2. FEATURES

- Complying with USB spec. Rev.1.0 and HID Class Rev. 1.0
- Supporting one device address and five endpoints (one Control transfer, four Interrupt transfer)
- Implementing USB keyboard with PS/2 mouse connection

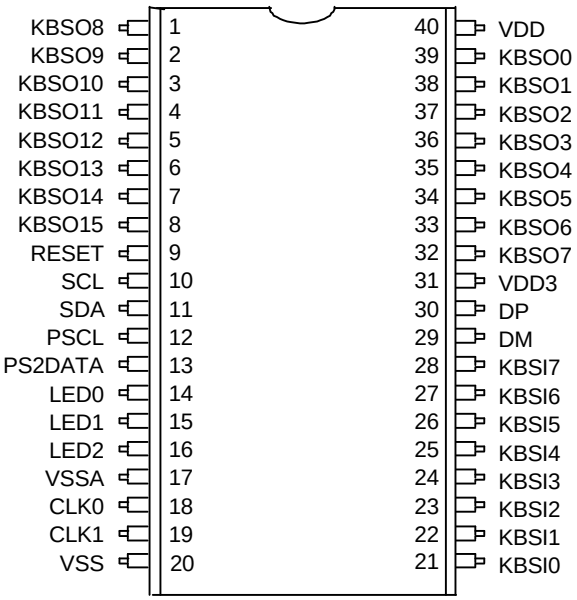
  Supporting 8-bit sense (row) input with wakeup interrupt on falling eage, internal pull-ups
- Supporting 18-bit drive (column) output, open drain with pull-ups
- 8-bit 8051 compatible CPU core
- 6K-byte ROM
- 256-byte SRAM
- 3 direct drive LED outputs with internal series resisters, Isink= 20 mA
- Supporting warm reset
- Supporting external serial EEPROM access
- 40/42-pin DIP
- 5V CMOS Device

3. BLOCK DIAGRAM

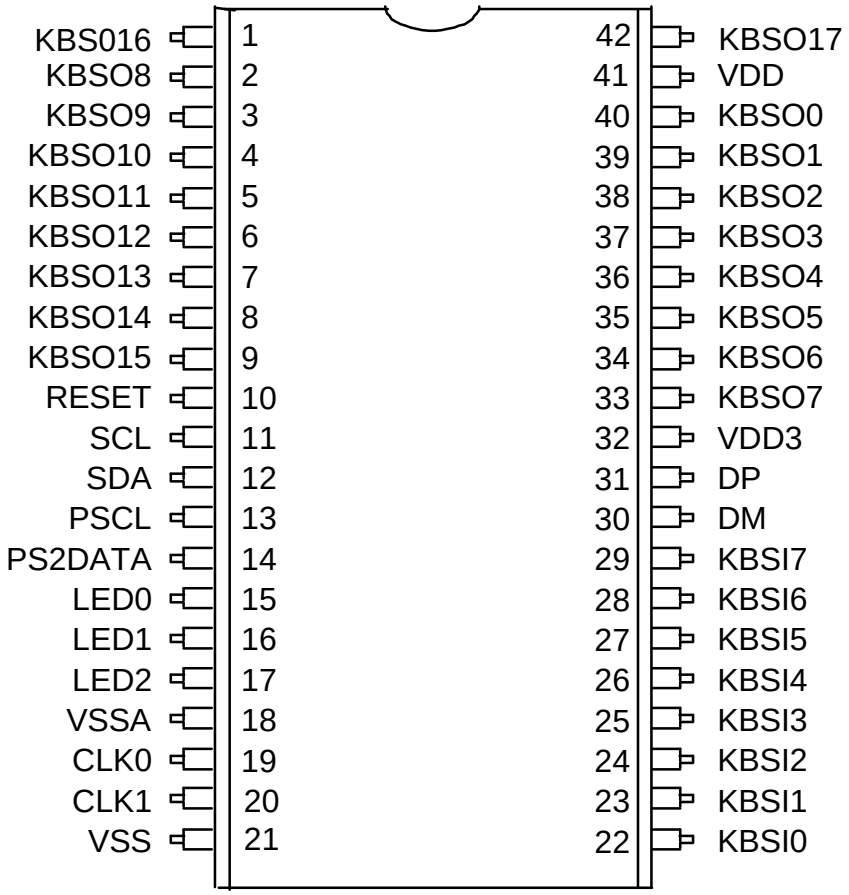
Winbond USB Keyboard Controller



4. PIN CONFIGURATION



40-pin DIP



42-pin DIP

5. PIN DESCRIPTION

5.1 40 DIP PIN

PIN NO.	NAME	TYPE	DESCRIPTION
1	P10 / KBSO8	OUTPUT	Keyboard scan output
2	P11 / KBSO9	OUTPUT	Keyboard scan output
3	P12 / KBSO10	OUTPUT	Keyboard scan output
4	P13 / KBSO11	OUTPUT	Keyboard scan output
5	P14 / KBSO12	OUTPUT	Keyboard scan output
6	P15 / KBSO13	OUTPUT	Keyboard scan output
7	P16 / KBSO14	OUTPUT	Keyboard scan output

8	P17 / KBSO15	OUTPUT	Keyboard scan output
9	RESET	INPUT	Reset signal
10	P30(TT0) / SCL	I/O	P30 / EEPROM CLK (IE.6=1, IP.3=1,see 5.3) Pull high when RESET falling
11	P31(TT1) / SDA	I/O	P31 / EEPROM DATA (IE.6=1, IP.3=1,see 5.3) Pull high when RESET falling

5.1 40 DIP PIN, continued

PIN NO.	NAME	TYPE	DESCRIPTION
12	PSCL	I/O	PS2 clock line
13	PSDA	I/O	PS2 data line
14*	P34/ KBSO16/ LED0	I/O	Keyboard scan output (Direct LED Drive)
15*	P35/ KBSO17/ LED1	I/O	Keyboard scan output (Direct LED Drive)
16	P36/ LED2	OUTPUT	Direct LED drive, Port36
17	VSSA	POWER	Analog ground
18	CLK0	OUTPUT	Crystal output
19	CLK1	INPUT	Crystal input
20	VSS	POWER	GND
21	P20/ KBSI0	INPUT	Keyboard scan intput
22	P21/ KBSI1	INPUT	Keyboard scan intput
23	P22/ KBSI2	INPUT	Keyboard scan intput
24	P23/ KBSI3	INPUT	Keyboard scan intput
25	P24/ KBSI4	INPUT	Keyboard scan intput
26	P25/ KBSI5	INPUT	Keyboard scan intput
27	P26/ KBSI6	INPUT	Keyboard scan intput
28	P27/ KBSI7	INPUT	Keyboard scan intput
29	DM	I/O	USB upstreampoint negative drive
30	DP	I/O	USB upstreampoint positive drive
31	VDD3	OUTPUT	3.3V input for USB bus drive
32	P07/ KBSO7	OUTPUT	Keyscan output
33	P06/ KBSO6	OUTPUT	Keyscan output
34	P05/ KBSO5	OUTPUT	Keyscan output
35	P04/ KBSO4	OUTPUT	Keyscan output
36	P03/ KBSO3	OUTPUT	Keyscan output
37	P02/ KBSO2	OUTPUT	Keyscan output
38	P01/ KBSO1	OUTPUT	Keyscan output
39	P00/ KBSO0	OUTPUT	Keyscan output
40	VDD	POWER	5V supply

* In 40 pin configuration,P34,P35 are shared by LED drive and Scanout function.

5.2 42 DIP PIN

PIN NO.	NAME	TYPE	DESCRIPTION
1	KBSO16	OUTPUT	Keyboard scan output line 16
2	P10 / KBSO8	OUTPUT	Keyboard scan output line 8
3	P11 / KBSO9	OUTPUT	Keyboard scan output line 9
4	P12 / KBSO10	OUTPUT	Keyboard scan output line 10
5	P13 / KBSO11	OUTPUT	Keyboard scan output line 11
6	P14 / KBSO12	OUTPUT	Keyboard scan output line 12
7	P15 / KBSO13	OUTPUT	Keyboard scan output line 13
8	P16 / KBSO14	OUTPUT	Keyboard scan output line 14
9	P17 / KBSO15	OUTPUT	Keyboard scan output line 15
10	RESET	INPUT	Reset signal
11	P30(TT0) / SCL	I/O	P30 / EEPROM CLK (IE.6=1, IP.3=1,see 5.3) Pull high when RESET falling
12	P31(TT1) / SDA	I/O	P31 / EEPROM DATA (IE.6=1, IP.3=1,see 5.3) Pull high when RESET falling
13	PSCL	I/O	PS2 clock line
14*	PSDA	I/O	PS2 data line
15*	P34/ KBSO16/ LED0	I/O	Keyboard scan output line 16(Direct LED0 Drive)
16	P35/ KBSO17/ LED1	I/O	Keyboard scan output line 17(Direct LED1 Drive)
17	P36/ LED2	OUTPUT	Direct LED2 drive, Port36
18	VSSA	POWER	Analog ground
19	CLK0	OUTPUT	Crystal output
20	CLK1	INPUT	Crystal input
21	VSS	POWER	GND
22	P20/ KBSI0	INPUT	Keyboard scan intput line 0
23	P21/ KBSI1	INPUT	Keyboard scan intput line 1
24	P22/ KBSI2	INPUT	Keyboard scan intput line 2
25	P23/ KBSI3	INPUT	Keyboard scan intput line 3
26	P24/ KBSI4	INPUT	Keyboard scan intput line 4
27	P25/ KBSI5	INPUT	Keyboard scan intput line 5

4.1 Pin Description, continued

40 DIP PIN#	NAME	TYPE	DESCRIPTION
28	P26/ KBSI6	INPUT	Keyboard scan intput line 6
29	P27/ KBSI7	INPUT	Keyboard scan intput line 7
30	DM	I/O	USB upstreampoint negative drive
31	DP	I/O	USB upstreampoint positive drive
32	VDD3	OUTPUT	3.3V input for USB bus drive
33	P07/ KBSO7	OUTPUT	Keyboard scan output line 7
34	P06/ KBSO6	OUTPUT	Keyboard scan output line 6
35	P05/ KBSO5	OUTPUT	Keyboard scan output line 5
36	P04/ KBSO4	OUTPUT	Keyboard scan output line 4
37	P03/ KBSO3	OUTPUT	Keyboard scan output line 3
38	P02/ KBSO2	OUTPUT	Keyboard scan output line 2
39	P01/ KBSO1	OUTPUT	Keyboard scan output line 1
40	P00/ KBSO0	OUTPUT	Keyboard scan output line 0
41	VDD	POWER	Power supply
42	KBSO17	OUTPUT	Keyboard scan output line 17

* In 40 pin configuration,P34,P35 are shared by LED drive and Scanout function.

6. FUNCTIONAL DESCRIPTION

6.1 First In First Out Storage (FIFO'S) Organization

The W81C280 has six FIFO's, one for receiving and five for transmitting.

FIFO or SRAM	SIZE (Byte)	NOTES
Endpt 0 Receiving	16	Data received on upstream port which contains the correct address and pids will be stored here for the CPU core to read.
Endpt 0 Transmitting	16	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 1 Transmitting	16	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 2 Transmitting	16	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 3 Transmitting	16	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 4 Transmitting	16	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.

6.1.1 INTERFACE TO THE MICROCONTROLLER:

The FIFOs communicate with the CPU core via a 2-wire serial bus. One signal is the data (P30/MDA) and the other is the clock (P31/MCL). The clock is always generated by the CPU core. The data is bi-directional. After each byte of data (MSB first) an acknowledge bit (MDA=0) is sent by the receiver. The CPU core always initiates the communication with a start condition (MDA from 1 change to 0 while MCL=1) and the FIFO's address. The CPU core ends the transmission with a stop condition (MDA from 0 change to 1 while MCL=1). Data is always changed while MCL=0 and clocked in on the rising edge of MCL. The FIFO acts as a slave memory device at address E8h.

the serial BUS'S ADDRESS	READ FROM FIFO	WRITE TO FIFO
1110 100S	S=1	S=0

The format for describing the interface to the FIFO is as follows:

ST = Start (MDA from 1 change to 0 while MCL=1)

AW = An acknowledge given by the FIFO Interface (the FIFO Interface brings MDA=0 during the 9th MCL pulse.)

AU = An acknowledge given by the CPU core (the CPU core brings MDA=0 during the 9th MCL pulse.)

NA = No acknowledge (this signifies the end of data being read from the FIFO Interface.)

SP = Stop (MDA from 0 change to 1 while MCL=1)

For example, for the CPU core to read the USB Interface's Status Register0 only and the value is E9h″:

ST	11101001	AW	SR0 (8)	NA	SP

ST= Start AW= FIFO Interface Acknowledge

AU= CPU core Acknowledge

NA= No Acknowledge

SP= Stop

11101001= the serial bus's Read Address

SR0 (8) = Status Register 0 (8 bits) (MSB 1st)

6.2 Register Descritpion

6.2.1 Status Registers

Status Register 0:

BIT	SYMBOL	DESCRIPTION
7	BADRECV	Set when received either a bad CRC or stuffing error from the host.
6	NINT	Cleared when an interrupt is pending. (See INTERRUPTS)
5	DAVEP0	Set when USB endpoint 0 FIFO has data to be read. Cleared after data is read.
4	EP1_ACK	Set when USB endpoint 1 has received the ACK. Cleared after Status Registers are read.
3	(RESERVED)	
2	NRST_RECD	Cleared when a RESET command is received from the host. Set after Status Registers are read.
1	NSUSPEND	Cleared when no activity is on the USB bus for > 3ms. Set when activity is resumed.
0	NREC_RES	Cleared by a global wake up sent from USB bus. Set after Status Registers are read.

Status Register 1: (RESERVED)

Status Register 2:

BIT	SYMBOL	DESCRIPTION
7	NTOUT4	Cleared when host not responds to handshake for endpoint 4 transmitted on the turnaround interval.
6	SPD_CHK	"1" for High speed device ; "0" for Low speed device
5	PWD_Mode	"1" for chip going into power down status
4-0	(RESERVED)	

Status Register 3:

BIT	SYMBOL	DESCRIPTION
7	VBUS	Shows the VBUS voltage from host (upstream port attached.)
6	NTOUT0	Cleared when host not responds to handshake for endpoint 0 transmitted on the turnaround interval.
5	NTOUT1	Cleared when host not responds to handshake for endpoint 1 transmitted on the turnaround interval.
4	NTOUT2	Cleared when host not responds to handshake for endpoint 2 transmitted on the turnaround interval.
3	NTOUT3	Cleared when host not responds to handshake for endpoint 3 transmitted on the turnaround interval.
2	EP2_ACK	Set when USB endpoint 2 has received the ACK. Cleared after data is read.
1	EP3_ACK	Set when USB endpoint 3 has received the ACK. Cleared after data is read.
0	EP4_ACK	Set when USB endpoint 4 has received the ACK. Cleared after data is read.

6.2.2 Control Registers (All registers are set to 00h at power up.)

Control Register 0:

BIT	SYMBOL	DESCRIPTION
7	USB_SP	"1" for high speed device ; "0" for low speed device
6	WARM_RESET	"1" = Warm Reset for whole chip.
5	URESUME	Setting causes a resume (K state) to be sent to upstream port..
4-1	(RESERVED)	
0	CPU RSTP0	Setting causes a SE0 to be placed on upstream port. To take the SE0 off, Clear CPU core RSTP0.

Control Register 1: (RESERVED)

Control Register 2:

BIT	SYMBOL	DESCRIPTION
7	(RESERVED)	
6	CRC_OFF	Setting this bit disables the receiving CRC checking circuit.
5-0	(RESERVED)	

Control Register 3: (RESERVED)

Control Register 4: (RESERVED)

Control Register 5:

BIT	SYMBOL	DESCRIPTION
7	(RESERVED)	
6-0		USB Address code for device.

Control Register 6:

BIT	SYMBOL	DESCRIPTION
7	CLK_SEL	Internal clock select. "1" for low speed device.
6	SYSCLK_SEL	"0" for 6 MHZ ; "1" for 12 MHZ.
5	PWD_MODE	Power down Mode flag (set "1" When chip goes into suspend mode)
4-2	(RESERVED)	
1-0	(RESERVED BITs ; Should be set " 0")	

6.3 Reading Data From The USB FIFOs and Registers

When data has been received by the W81C280 from USB bus, theinternal interrupt will be enabled and the following flag in the Status Register will be set: DAVEP0.

To access this data just continue reading the FIFO by the serial bus. The data associated with the flag stated above will be read from the W81C280. In all cases the MSB will be read first since the W81C280 converts the USB's LSB protocol.

6.3.1 Reading from the USB's Endpoint0 FIFO

The endpoint0 FIFO is used for Control Transfers. After valid data (USB address match) is sent from the PC to the device via USB's endpoint 0, when the CPU core reads the Status Registers it sees that DAVEP0 is set. Therefore, when it continues to read from the W81C280 beyond Status Register 3, the ensuing data will be the USB's endpoint 0 FIFO. Consult the USB specification for transfer types, stages, and phases.

- Reading the Control transfer's Setup stage (always 8 bytes of data sent from the host):

ST	11101001	AW	SR0 (8)	AU	SR1 (8)	AU	SR2 (8)	AU	SR3 (8)	AU	
			SETUP PID	AU	ADDRESS	AU	CRC	AU	DATA0 PID	AU	
	DATA0	AU	DATA1	AU	DATA2	AU	DATA3	AU	DATA4	AU	
	DATA5	AU	DATA6	AU	DATA7	AU	CRC	AU	CRC	NA	SP

11101001= the serial bus's Read Address

- Reading the Control transfer's Data stage for a Write transfer (maximum 8 bytes of data sent from the host):

ST	11101001	AW	SR0 (8)	AU	SR1 (8)	AU	SR2 (8)	AU	SR3 (8)	AU	
			OUT PID	AU	ADDRESS	AU	CRC	AU	DATA1 PID	AU	
	DATA0	AU	DATA1	AU	DATA2	AU	DATA3	AU	DATA4	AU	
	DATA5	AU	DATA6	AU	DATA7	AU	CRC	AU	CRC	NA	SP

- Reading the Control transfer's Status stage for a Read / Write transfer:

ST	11101001	AW	SR0 (8)	AU	SR1 (8)	AU	SR2 (8)	AU	SR3 (8)	AU	
			IN PID	AU	ADDRESS	AU	CRC	AU	ACK or FFh	NA	SP

An ACK is read when the host successfully received the data packet sent from the W81C280.

Then the handshake was completed.

If the BAD_RECV bit in StatusRegister0 is set and CRC_OFF bit is cleared in ControlRegister 2, then ignore all data read.

6.3.2 Reading ACK Flag for the USB's Endpoint 1 - 4

The endpoint 1 - 4 are used for the Interrupt transfers. After valid datas ("IN" DATA stage) are sent to the host via USB's endpoint 1 - 4 FIFOs, and then ACK is sent by host, The interrupt flag is enabled and EP1_ACK/EP2_ACK/EP3_ACK/EP4_ACK is set in Status Registers. Therefore, the CPU core check the ACK handshake just from Status Registers.

- Checking the Interrupt transfer's Handshake from host:

ST	11101001	AW	SR0 (8)	AU	SR1 (8)	AU	SR2 (8)	AU	SR3 (8)	AU	SP

11101001= the serial bus Read Address

6.4 Writing Data To The USB FIFOs and Registers

There are 6 separate memory locations which the CPU core can write to: W81C280 Control Registers, USB endpoint 0-4 FIFOs. To access the desired memory location, the CPU core follows the address byte with a memory select byte:

Write to USB endpoint 0:	01h, 61h
Write to USB endpoint 1:	02h, 22h
Write to USB endpoint 2:	06h, 26h
Write to USB endpoint 3:	0ah, 2ah
Write to USB endpoint 4:	0eh, 2eh
Write to Control Registers:	X0h (X = 1~D)

6.4.1 Writing To The Control Registers

The W81C280 contains 7 write-only Control Registers.

ST	1110 1000	AW	xxx1 0000	AW	CR0 (8)	AW	CR1 (8)	AW	CR2 (8)	AW
	CR3 (8)	AW	CR4(8)	AW	CR5(8)	AW	CR6(8)	AW	SP	

CR0 (8) = Control Register 0 (8 bits) (MSB 1st) 11101000= the serial bus's Write Address

xxx : index of control register can be from 000 to 110

The writing to the Control Registers can be started any Control Register dependent on B[7:5] of sencond byte and discontinued with a 'Stop' after any byte.

6.4.2 Writing To The USB Endpoint 0

Endpoint 0 is used for USB Control transfer for the device. The FIFO is set for a maximum data packet size of 8 bytes. That is, it can store 8 bytes of data plus sync, PID, and the 2 CRC bytes (12 bytes). The data written to this FIFO will be sent to the host via the USB bus (DP,DM) after the writing is completed and when any of the following conditions occur:

- A token packet is received from the PC with the correct address/endpoint, and an IN PID.
- A token packet is received from the PC with the correct address/endpoint, and an OUT or SETUP PID, followed by data sent from the PC.

If no data is present in the FIFO, a NAK PID will be sent to the host when one of the above conditions occur. Except after a SETUP PID when an ACK PID will be sent by the W81C180 if no data is present.

The data sent to the W81C280 FIFO must contain all of the data required to send including the sync, PID, and CRC's (unless it is chosen that the W81C280 generates the CRC's by H/w generator.) The CRC's can be generated by the W81C280 by including the number of data bytes to be sent in the high nibble of the memory select byte.The data sent also requires one stop byte of FFh. The W81C280 will convert the data to the USB protocol of NRZI, bit stuffing, and LSB first. Once the data is sent, the FIFO is emptied until new data is written to it.

- Writing 2 bytes of data to the FIFO and letting the W81C280 generate the CRC's by H/W

ST	1110 1000	AW	0110 0001	AW	SYNC(80H)	AW	DATAx PID	AW	DATA		AW
					DATA	AW	1111 1111	AW	SP		

11101000= the serial bus's Write Address 1111 1111=Stop Byte

- Writing 2 bytes of data to the FIFO and having the W81C280 generate the CRC's by F/W

ST	1110 1000	AW	01h	AW	SYNC(80H)	AW	DATAx PID	AW	DATA		AW
	DATA	AW	CRC	AW	CRC	AW	1111 1111	AW	SP		

6.4.3 Writing To The USB Endpoint 1 - 4

Endpoint 1 - 4 are used for USB Interrupt transfers. The FIFOs are set for a maximum data packet size of 8 bytes. That is, it can store 8 bytes of data plus sync, PID, and the 2 CRC bytes (unless the it is chosen that the W81C280 generates the CRC's by H/W.) The CRC's can be generated by the W81C280 by including the number of data bytes to be sent in the high nibble of the memory select byte. The data sent also requires one stop byte of FFh. The data written to this FIFO will be sent to the host via the USB bus (DP,DM) after the writing is completed and when a token packet is received from the PC with the correct address/endpoint, and an IN PID. If no data is present in the FIFO, a NAK PID will be sent to the host when the above condition occurs.

The W81C280 will convert the data to the USB protocol of NRZI, bit stuffing, and LSB first. Once the data is sent, the FIFO is emptied until new data is written to it.

- Writing 8 bytes of data to the FIFO and having the W81C280 generate the CRC's BY F/W

ST	1110 1000	AW	0000 xx10	AW	SYNC(80H)	AW	DATA1 PID	AW	DATA0	AW		
	DATA1	AW	DATA2	AW	DATA3	AW	DATA4	AW	DATA5	AW		
	DATA6	AW	DATA7	AW	CRC	AW	CRC	AW	1111 1111	AW	SP	

- Writing 8 bytes of data to the FIFO and letting the W81C280 generate the CRC's by H/W

ST	1110 1000	AW	0010 xx10	AW	SYNC(80H)	AW	DATA1 PID	AW	DATA0	AW
	DATA1	AW	DATA2	AW	DATA3	AW	DATA4	AW	DATA5	AW
	DATA6	AW	DATA7	AW	1111 1111	AW	SP			

XX = 00(EP1); 01(EP2); 10(EP3); 11(EP4)

6.5 Internal interrupts

The interrupt (P3.7 in CPU core) will be enabled and disabled under the following actions:

ENABLE INTERRUPT	DISABLE INTERRUPT
Resume	After the CPU core reads the Status Registers.
Endpoint 1 - 4 Handshake ACK received	After Status Registers are read.
Endpoint 0 data received	After the CPU core reads the Status Registers.
Turnaround time-out	After the CPU core reads the Status Registers.
Suspend (no activity) on the USB bus	After the CPU core reads the Status Registers.
Reset sent from upstream	After the CPU core reads the Status Registers.

6.5.1 Reacting To The Internal interrupts

Since there is no condition which requires immediate attention by the CPU core, the NINT pin does not necessarily have to be used. The CPU core can access the W81C280 in following alternative way:

- Have the P3.7 to be an interrupt pin in the CPU core and read the W81C280 Status registers when it is enabled.

6.6 Reset

The W81C280 supports three types of reset. During a reset, all registers of the CPU core and USB return to their default status, and USB device address is set to zero.

6.6.1 External Reset

As in 8051 series controller, the external RESET signal is sampled at S5P2. To take effect, it must be held high at least two machine cycles while the oscillator is running.

An internal trigger circuit in the reset line is used to deglitch the reset line. The reset logic also has a special glitch remocal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON(with exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

6.6.2 Warm Reset

W81C280 provides a warm reset by programming a 1 to bit 6 of control register 0.

6.6.3 USB Reset

The W81C280 handles the USB reset function independently from the CPU core. If a Single Ended Zero (SE0) is detected on the upstream port for greater then 2.5us, then the interrupt is enabled. The CPU core read flag from bit2 of status register 0 and t reset the device address to 0, and enter the active state.

6.7 USB SUSPEND

If there is no upstream activity for 3msec then the SUSPEND flag is set and the interrupt enabled. When SUSPEND flag is read by CPU core, The W81C280 go into suspend

6.8 USB RESUME:

The suspend mode can be disabled by a 'resume'. The resume can occur by four methods.

- The host can send a resume to all ports by placing a 0 (K state) on the bus. The W81C280 sees the resume, disables the SUSPEND flag, and enables the interrupt. In this case, the CPU core does not have to perform any functions.
- The host can reset the bus.
- When any key in Keyboard is press The CPU core can initiate a resume by setting URESUME in the Control Register which will cause a K state to be sent. To un-resume, the CPU core must clear the URESUME bit in the Control Register.

6.9 FULL/LOW SPEED DEVICE DETECTION:

The W81C280 detects if upstream port is full speed (FS) or low speed (LS) and sets the appropriate flag. the CPU core has to configure it as a FS or LS device

7. PROGRAMMING NOTES :

The W81C280 uses reserved bit of the Interrupt Enable Register IE.6 as a pre-docoding bit to implement

a alternative register which has the same address with IP, the Interrupt Priority register. That is, for E.6=0 (default), the IP acts normally and for IE.6=1 it cab be used for programming functions described as below:

7.1 SET IP(INTERRUPT PRIORITY) REGISTER IN CPU CORE :

step 1 : set IE.6 = 0 (Interrupt enable bit)

step 2 : access any IP bit

7.2 SET WAKEUP AND RESUME INTERRUPTS (for RESUME the chip)

step 1 : set IE.6 = 1

step 2 : set IP.2 = 1

7.3 THE SERIAL BUS ACCESS

P30 and P31 of the CPU core are used to access both internal serial bus and the external serial EEPROM.

7.3.1 Access external EEPROM

step 1 : set IE.6 = 1

step 2 : set IP.3 = 1

step 3 : use the serial bus to access serial EEPROM

7.3.2 Access internal serial bus

step 1 : set IE.6 = 1

step 2 : set IP.3 = 0

step 3 : access DATA by the serial bus

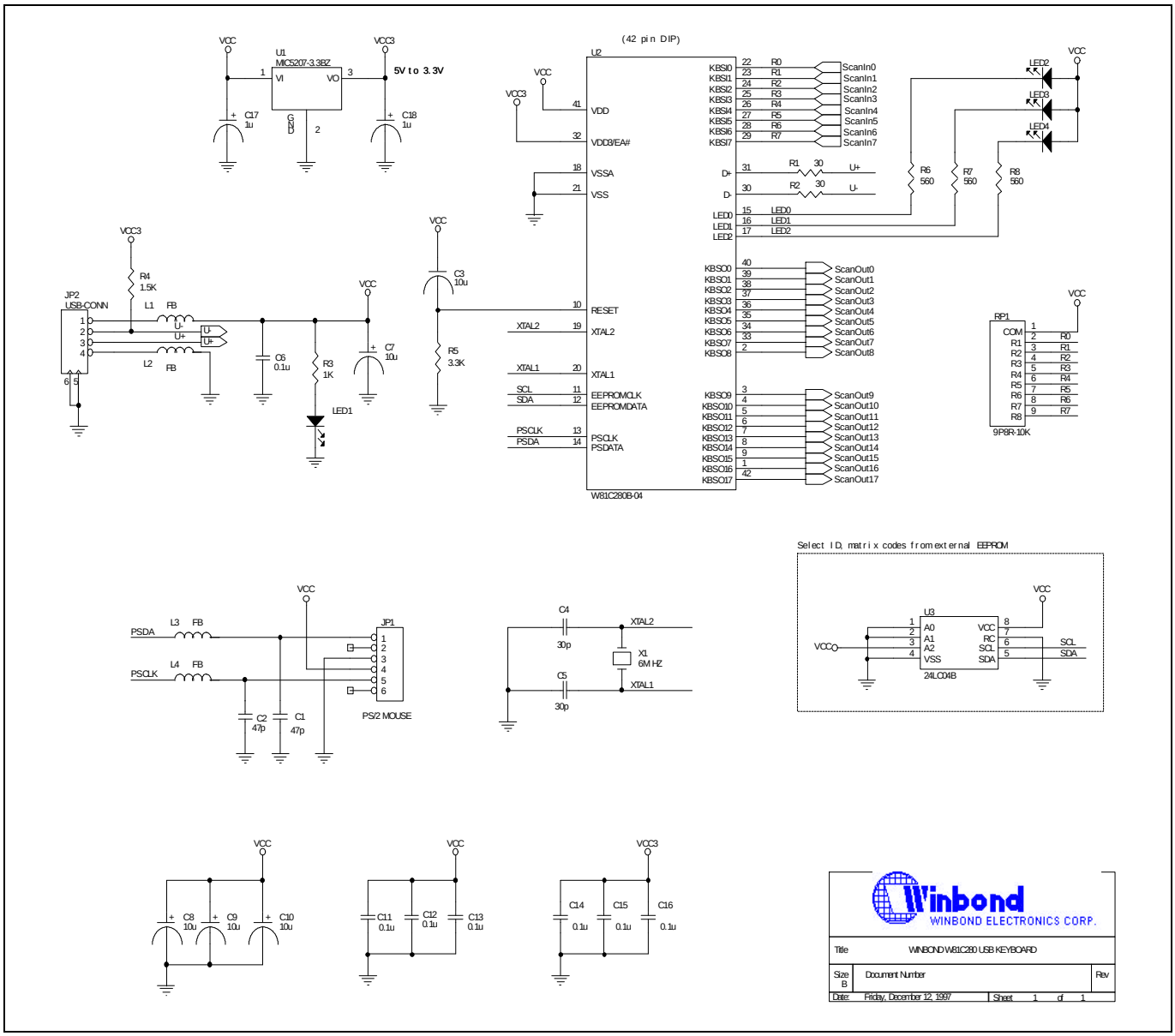
8. ELECTRICAL CHARACTERISTICS & CAPACITANCE

(Ta = 0¢Jto + 70¢J, VDD = +5V ± 5%)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTE
VDD	Power Support	4.75	5.0	5.25	V	
VIL	Input Low Voltage(except RESET)			0.8	V	
VIL1	Input Low Voltage(RESET)			0.6	V	
VIH1	Input High Voltage(except RESET)	2.0			V	
VIH2	Input High Voltage(RESET)	3.5			V	
VOH	Output High Voltage(D0 ~ D7)			2.4	V	IOH=-4mA
VOL	Output Low Voltage(D0 ~ D7)	0.4			V	IOL= 4mA
IOFL	Output Leakage Current(D0 ~D7), High-Z state)	-10		10	uA	
IIH	Input Leakage Current	-10		10	uA	VDD=5.5V VIN=VDD
IIL	Input Leakage Current	-10		10	uA	VDD=5.5V VIN=VSS

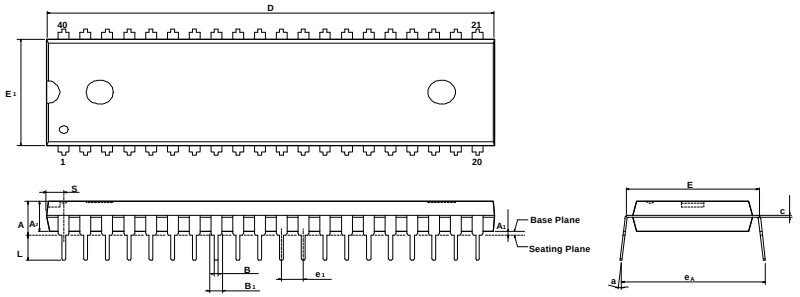
	Symbol	Conditions	Min	Max	Unit
Leakage Current:					
Hi-Z State Data Line Leakage	ILO	0 V < VIN < 3.3V	-10	+10	μA
Input Levels:					
Differential Input Sensitivity	VDI	|(D+)-(D-)|, and Figure 0-4	0.2		V
Differential Common Mode Range	VCM	Includes VDI range	0.8	2.5	V
Single Endge Receiver Threshold	VSE		0.8	2.0	V
Output Levels:					
Static Output Low	VOL	RL of 1.5kΩ to 3.6V		0.3	V
Static Output High	VOH	RL of 1.5kΩ to GND	2.8	3.6	V
Capacitance:					
Transceiver Capacitance	CIN	Pin to GND		20	pF
Driver Characteristics:					
Transition Time:					
Rise Time	TR	CL=50pF/350pF	75	300	ns
Fall Time	TF	CL=50pF/350pF	75	300	ns
Rise / Fall Time Matching	TRFM	(TR / TF)	80	120	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V
Data Source Timings:					
Low Speed Data Rate	TDRATE	Ave.Bit Rate(1.5Mb/s± 1.5%)	1.4775	1.5225	Mbs
Source Differential Driver Jitter					
To Next Transition	TDJ1		-95	95	ns
For Paired Transitions	TDJ2		-150	150	ns
Source EOP Width	TEOPT		1.25	1.50	μs
Differential to EOP transition Skew	TDEOP		-40	100	ns
Receiver Data Jitter Tolerance					
To Next Transition	TJR1		-75	75	ns
For Paired Transitions	TJR2		-45	45	ns
EOP Width at receiver					
Must reject as EOP	TEORP1		330		ns
Must accept as EOP	TEOPR2		675		ns

9. USB KEYBOARD SAMPLE APPLICATION



10. PACKAGE DIMENSIONS

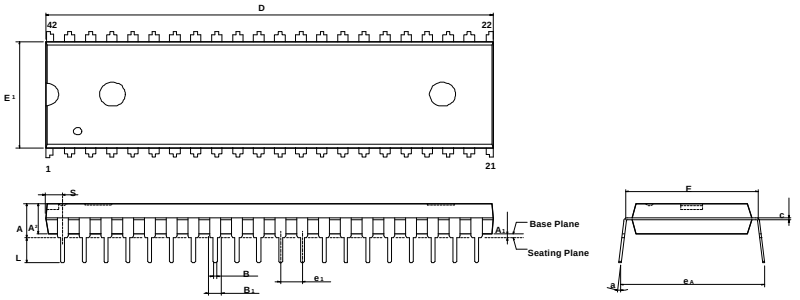
40-pin PDIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:
1. Dimensions D Max & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

42-pin PDIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.040	—	—	1.02

Notes:
1. Dimensions D Max & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

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