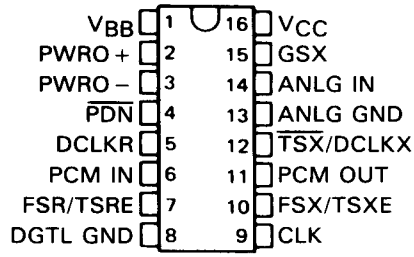
TCM29C18, TCM29C19
ANALOG INTERFACE FOR DSP

D3036, AUGUST 1987

- **Reliable Silicon-Gate CMOS Technology**
- **Low Power Consumption**
  Operating Mode . . . 80 mW
  Power-Down Mode . . . 5 mW
  μ-Law Coding
- **Excellent Power Supply Rejection Ratio over Frequency Range of 0 to 50 kHz**
- **No External Components Needed for Sample, Hold, and Auto-Zero Functions**
- **Precision Internal Voltage References**
- **Single Chip Contains A/D, D/A, and Associated Filters**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FEATURE TABLE

16 Pins
μ-Law Coding
Variable Mode:
64 kHz to 2.048 MHz
Fixed Mode:
2.048 MHz (TCM29C18),
1.536 MHz (TCM29C19)
8-Bit Resolution
12-Bit Dynamic Range

ADVANCE INFORMATION

description

The TCM29C18 and the TCM29C19 are low-cost single-chip pulse-code-modulated encoders and decoders (PCM codecs) and PCM line filters. These devices incorporate both the A/D and D/A functions, an anti-aliasing filter (A/D), and a smoothing filter (D/A). The TCM29C18 and the TCM29C19 are ideal for use with the TMS320 family members, particularly those featuring a serial port such as the TMS32020, TMS32011, and TMS320C25.

Primary applications of these devices include:

Digital Encryption Systems
Digital Voice-Band Data Storage Systems
Digital Signal Processing

These devices are designed to perform encoding of analog input signals (A/D conversion) and decoding of digital PCM signals (D/A conversion). They are useful for implementation in the analog interface of a digital-signal processing system. Both devices also provide band-pass filtering of the analog signals prior to encoding and smoothing after decoding.

The analog input is encoded into an 8-bit digital representation by use of the μ-law encoding scheme (CCITT G.711) which equates to 12 bits of resolution for low amplitude signals. Similarly, the decoding section converts 8-bit PCM data into an analog signal with 12 bits of dynamic range. The filter characteristics (bandpass) for the encoder and decoder are determined by a single clock input (CLK). The filter roll-off (-3 dB) is derived by:

$$f_{co} = k \cdot f_{CLK}/256 \text{ for the TCM29C18 or } f_{co} = k \cdot f_{CLK}/192 \text{ for the TCM29C19}$$

where k has a value of 0.44 for the high-frequency roll-off point, and a value of 0.019 for the low-frequency roll-off point.

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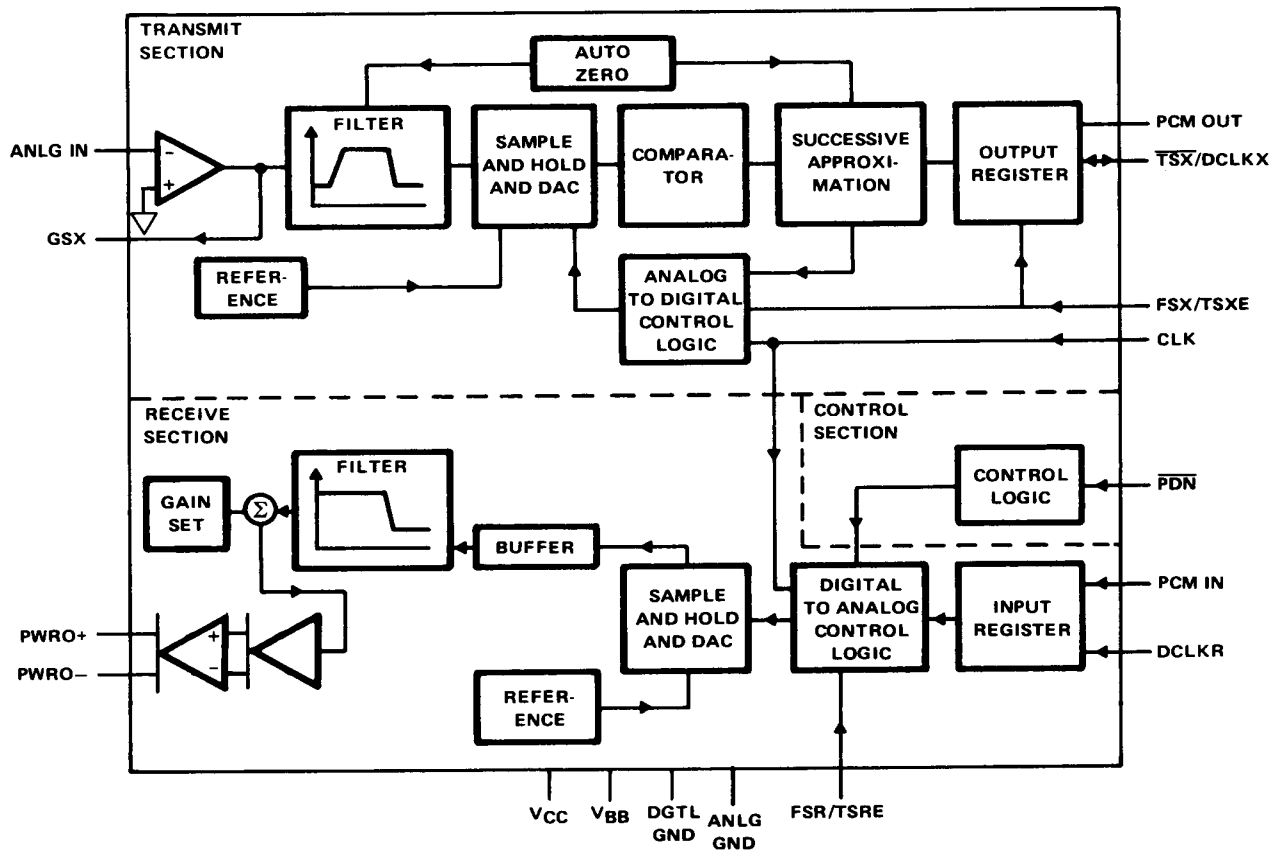
description (continued)

The sampling rate of the ADC is determined by the Frame Sync Clock, FSX; the sampling rate of the DAC is determined by the Frame Sync Clock, FSR. Once a conversion is initiated by FSX or FSR, data is clocked in or out on the next consecutive eight clock pulses in the fixed data rate mode. Likewise, data may also be transferred on the next eight consecutive clock pulses of the data clocks, DCLKX and DCLKR, in the variable data rate mode. In the variable data rate mode, DCLKX and DCLKR are independent, but must be in the range from $f_{CLK}/32$ to f_{CLK}.

The TCM29C18 and TCM29C19 are characterized for operation over the temperature range of 0 °C to 70 °C.

functional block diagram



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NAME	PIN	DESCRIPTION
ANLG IN	14	Inverting analog input to uncommitted transmit operational amplifier
ANLG GND	13	Analog ground return for all voice circuits. Not internally connected to digital ground.
CLK	9	Master clock and data clock for the fixed data rate mode. Master (filter) clock only for variable data-rate mode. This clock is used for both the transmit and receive sections.
DCLKR	5	When this pin is connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock, which operates at frequencies from 64 kHz to 2.048 MHz.
DGTL GND	8	Digital ground for all internal logic circuits. Not internally connected to analog ground.
FSR/TSRE	7	Frame sync clock input/time-slot enable for the receive channel. In the variable-data-rate-mode, this signal must remain high for the duration of the time-slot. The receive channel enters the standby state when FSR is TTL low for 30 ms.
FSX/TSXE	10	Frame synchronization clock input/time-slot enable for transmit channel. Operates independently of, but in an analogous manner to FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300 ms.
GSX	15	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
PCM IN	6	Receive PCM input. PCM data is clocked in on this pin on eight consecutive negative transitions of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
PCM OUT	11	Transmit PCM output. PCM data is clocked out of this output on eight consecutive positive transitions of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.
$\overline{\text{PDN}}$	4	Power-Down Select. On the TCM29C18, the device is inactive with a TTL low-level input and active with a TTL high-level input to the pin. On the TCM29C19, this pin must be connected to a TTL high level.
PWRO +	2	Noninverting output of power amplifier can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
PWRO −	3	Inverting output of power amplifier, functionally identical to PWRO +
$\overline{\text{TSX}}$/DCLKX	12	Transmit channel time slot strobe (output) or data clock (input). In the fixed-data-rate mode, this is an open-drain output to be used as an enable signal for a three-state-buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock, which operates at TTL levels from 64 kHz to 2.048 MHz.
V_{BB}	1	Negative supply voltage, −5 V ±5%.
V_{CC}	16	Positive supply voltage, 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 to 15 V
Output voltage, V_O . . . . . −0.3 to 15 V
Input voltage — digital inputs, V_I . . . . . −0.3 to 15 V
Digital ground voltage . . . . . −0.3 to 15 V
Operating free-air temperature range (under bias) . . . . . −10°C to 80°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTE 1: Voltage values for maximum ratings are with respect to V_{BB}.

ADVANCE INFORMATION

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{BB}		−4.75	−5	−5.25	V
DGTL GND voltage with respect to ANLG GND			0		V
High-level input voltage, V_{IH}, all inputs except ANLG IN		2.2			V
Low-level input voltage, V_{IL}, all inputs except ANLG IN				0.8	V
Peak-to-peak analog input voltage, V_{IPP}				4.2	V
Load resistance, R_L	GSX	10			kΩ
	PWRO+ and/or PWRO−	300			Ω
Load capacitance, C_L	GSX			50	pF
	PWRO+ and/or PWRO−			100	
Operating free-air temperature, T_A		0		70	°C

NOTES: 2. Voltages at analog inputs and outputs, V_{CC} and V_{BB} terminals are with respect to the ANLG GND terminal. All other voltages are referenced to the DGTL GND terminal unless otherwise noted.
3. Analog input signals that exceed 4.2 V peak-to-peak may contribute to clipping and preclude correct A/D conversion. The digital code representing values higher than 4.200 V is 10000000. For values more negative than 4.200 V, the code is 0000000.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

supply current, fdclk = 2.048 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	operating			10	mA
		standby	FSX or FSR at V_{IL} after 300 ms		1.2	
		power down	$\overline{PDN}$ at V_{IL} after 10 μs		1	
I_{BB}	Supply current from V_{BB}	operating			−10	mA
		standby	FSX or FSR at V_{IL} after 300 ms		−1.2	
		power down	$\overline{PDN}$ at V_{IL} after 10 μs		−1	

digital interface

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage, PCM OUT	I_{OH} = −9.6 mA	2.4			V
		I_{OH} = −0.1 mA	3.5			
V_{OL}	Low-level output voltage, $\overline{TSX}$	I_{OL} = 3.2 mA			0.4	V
I_{IH}	High-level input current, any digital input	V_I = 2.2 V to V_{CC}			10	μA
I_{IL}	Low-level input current, any digital input	V_I = 0 to 0.8 V			10	μA
C_i	Input capacitance			5	10	pF
C_o	Output capacitance			5	10	pF

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

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transmit side (A/D) characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input offset current at ANLG IN	V_I = −2.17 V to 2.17 V		1		pA
Input offset voltage at ANLG IN	V_I = −2.17 V to 2.17 V			±25	mV
Input bias current	V_I = −2.17 V to 2.17 V			±100	nA
Open-loop voltage amplification at GSX		5000			
Unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN		10			Ω
Gain tracking error with sinusoidal input (see Notes 4, 5, and 6)	3 dBm0 to −40 dBm0, REF level = −10 dBm0			±0.5	dB
	−40 dBm0 to −50 dBm0, REF level = −10 dBm0			±2.5	
Transmit gain tolerance	V_i = 1.06 V, f = 1.02 kHz	0.95		1.19	Vrms
Supply voltage rejection ratio, V_{CC} or V_{BB}	f = 0 to 30 kHz, (measured at PCM OUT) idle channel, Supply signal = 200 mV P-P	−20			dB
Crosstalk attenuation, transmit-to-receive (single-ended)	ANLG IN = 0 dBm, f = 1 kHz unity gain, PCM IN = lowest decode level, measured at PWRO+	−62			dB
Signal-to-distortion ratio, with sinusoidal input (see Note 7)	ANLG IN = 0 to −30 dBm0	25			dB
	ANLG IN = −30 to −40 dBm0	20			
	ANLG IN = −40 to −45 dBm0	15			
Absolute delay time to PCM OUT	Fixed data rate, FCLKX = 2.048 MHz, input to ANLG IN = 1 kHz at 0 dB		245		μs

receive side (D/A) characteristics (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output offset voltage PWRO+ and PWRO− (single-ended)	Relative to ANLG GND			±200	mV
Output resistance at PWRO+ and PWRO−			1	2	Ω
Gain tracking error with sinusoidal input (see Notes 4, 5, and 6)	3 dBm0 to −40 dBm0, REF level = −10 dBm0			±0.5	dB
	−40 dBm0 to −50 dBm0, REF level = −10 dBm0			±2.5	
Receive gain tolerance	V_i = 1.06 V, f = 1.02 kHz	1.34		1.69	Vrms
Noise	Ref max output level: 200 Hz to 3 kHz	−60			dB
Supply voltage rejection ratio, V_{CC} or V_{BB} (single-ended)	f = 0 to 30 kHz, idle channel, Supply signal = 200 mV P-P, narrow band, frequency at PWRO+	−20			dB
Crosstalk attenuation, receive-to-transmit (single-ended)	PCM IN = 0 dB, Frequency = 1 kHz at PCM OUT	−60			dB
Signal-to-distortion ratio, sinusoidal input (see Note 7)	ANLG IN = 0 dBm0 to −30 dBm0	25			dB
	ANLG IN = −30 dBm0 to −40 dBm0	20			
	ANLG IN = −40 dBm0 to −45 dBm0	15			
Absolute delay time to PWRO+	Fixed data rate, FCLKX = 2.048 MHz		190		μs

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

NOTES: 4. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 V rms, or an output of 1.503 V rms.
5. The input amplifier is set for unity gain, noninverting. GSX is connected to ANLG IN−. Signal input is ANLG IN+. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
6. Receive output is measured single-ended in the maximum-gain configuration. To set the output amplifier for maximum gain, GSR is connected to PWRO− and the output is taken at PWRO+. All output levels are (sin x)/x corrected.
7. CCITT G.712 — Method 2.
8. The receive side (D/A) characteristics are referenced to a 600-Ω termination.

ADVANCE INFORMATION

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see timing diagrams)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to bit 1 data valid at PCM OUT (data enable time on time slot entry)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	From rising edge of transmit clock bit n to bit n + 1 data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	From falling edge of transmit clock bit 8 to bit 8 Hi-Z at PCM OUT (data float time on time slot exit)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock bit 1 to TSX active (low) (time slot enable time)	C_L = 0 to 100 pF	0	145	ns
t_{pd5}	From falling edge of transmit clock bit 8 to TSX inactive (high) (timeslot disable time)	C_L = 0	60	190	ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	From DCLKX	C_L = 0 to 100 pF	0	100	ns
t_{pd7}	From time slot enable to PCM OUT	C_L = 0 to 100 pF	0	50	ns
t_{pd8}	From time slot disable to PCM OUT	C_L = 0 to 100 pF	0	80	ns
t_{pd9}	From FSX	$t_{d(TSDX)}$ = 140 ns	0	140	ns

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see timing diagrams)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLK, (2.048-MHz systems)	488			ns
t_r, t_f	Rise and fall times for CLK	5		30	ns
$t_{w(CLK)}$	Pulse duration for CLK	220			ns
$t_{w(DCLK)}$	Pulse duration for DCLK (f_{DCLK} = 64 Hz to 2.048 MHz)	220			ns
	Clock duty cycle [$t_{w(CLK)}/t_{c(CLK)}$] for CLK	45	50	55	%

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSX)}$	Frame sync delay time	0	$t_{c(CLK)} - 100$	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame sync delay time	0	$t_{c(CLK)} - 100$	ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDX)}$	Delay time, timeslot from DCLKX (see Note 9)	140	$t_{w(DCLKX)}-140$	ns
$t_{d(FSX)}$	Delay time, frame sync	100	$t_{c(CLK)}-100$	ns
$t_{w(DCLKX)}$	Pulse duration, DCLKX	488	15620	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDR)}$	Delay time, timeslot from DCLKR (see Note 10)	140	$t_{w(DCLKR)}-140$	ns
$t_{d(FSR)}$	Delay time, frame sync $T_{C(CLK)}$	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Setup time, before bit 7 falling edge	10		ns
$t_{h(PCM\ IN)}$	Hold time after bit 8 falling edge	60		ns
$t_{w(DCLKR)}$	Pulse duration, DCLKR	488	15620	ns
	Time slot and receive time	0		ns

64-kbit operation timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{FSLX}	Transmit frame sync minimum down time	FSX = TTL high for remainder of frame	488		ns
t_{FSLR}	Receive frame sync minimum down time	FSR = TTL high for remainder of frame	1952		ns
t_{wCLK}	Pulse duration, data clock			10	μs

NOTES: 9. t_{FSLX} min requirement overrides the $t_{d(TSCDX)}$ max requirement for 64-kHz operation.
10. t_{FSLR} min requirement overrides the $t_{c(TSDR)}$ max requirement for 64-kHz operation.

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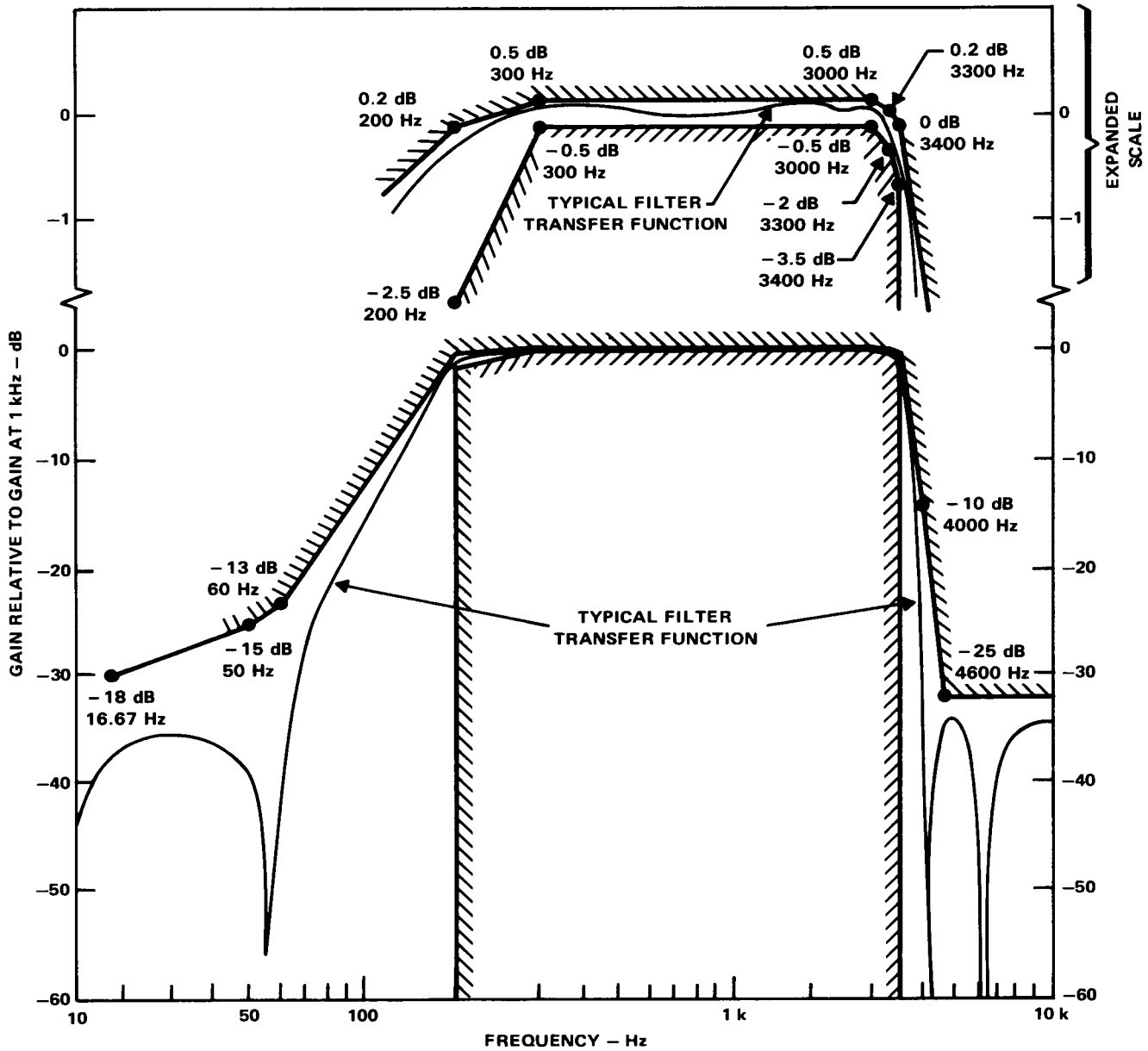

NOTE: This is a typical transfer function of the receiver filter component.

FIGURE 1. TRANSFER CHARACTERISTICS OF THE TRANSMIT FILTER

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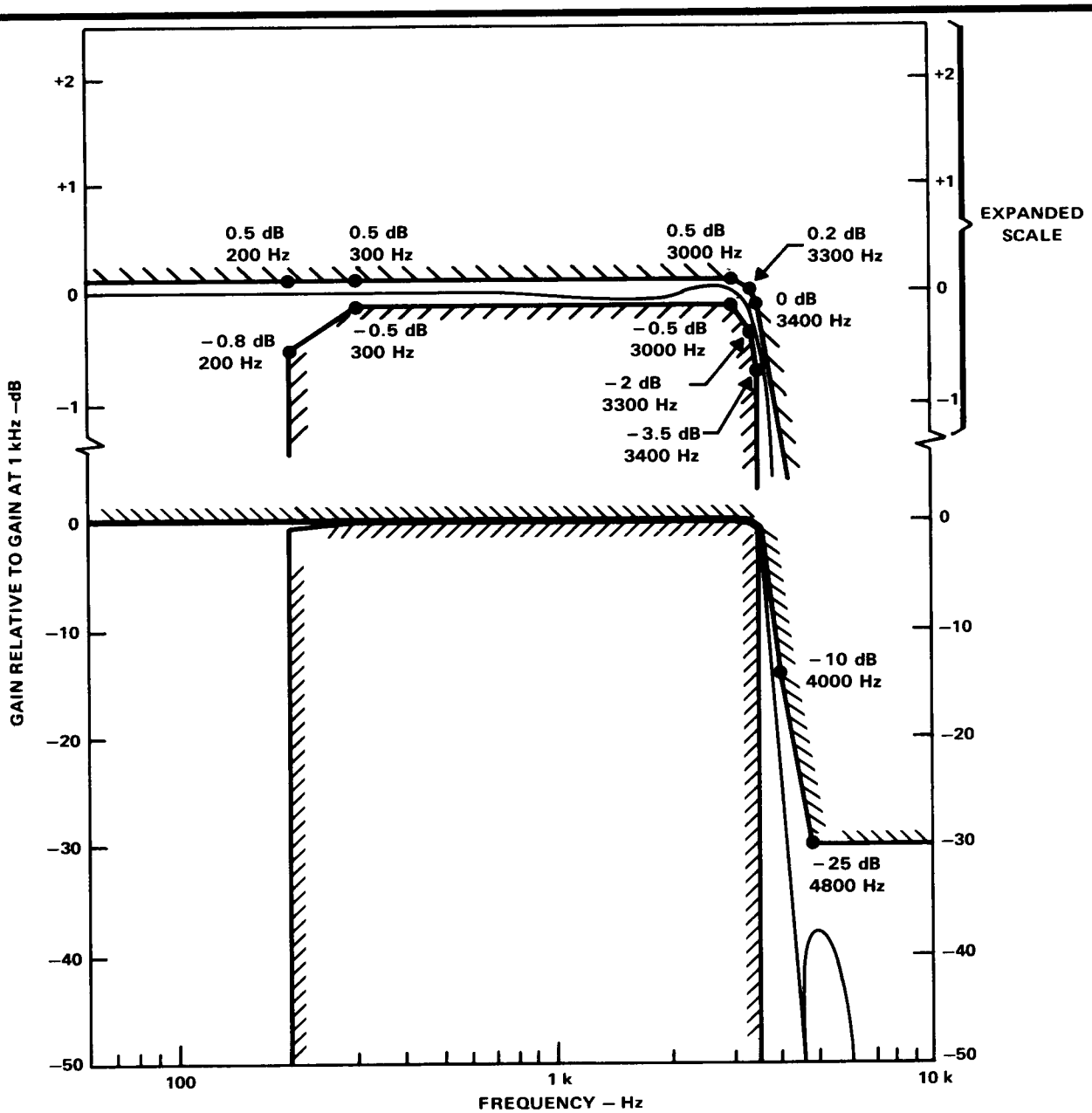


NOTE: This is a typical transfer function of the receiver filter component.

FIGURE 2. TRANSFER CHARACTERISTIC OF THE RECEIVE FILTER

ADVANCE INFORMATION

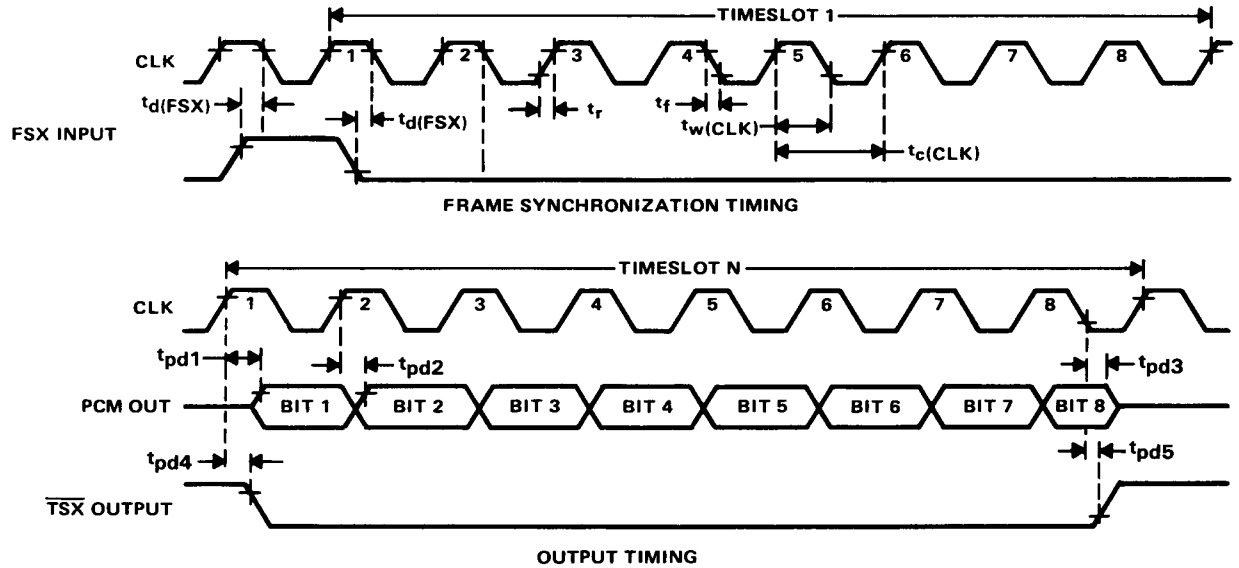


FIGURE 3. TRANSMIT TIMING (FIXED-DATA-RATE)

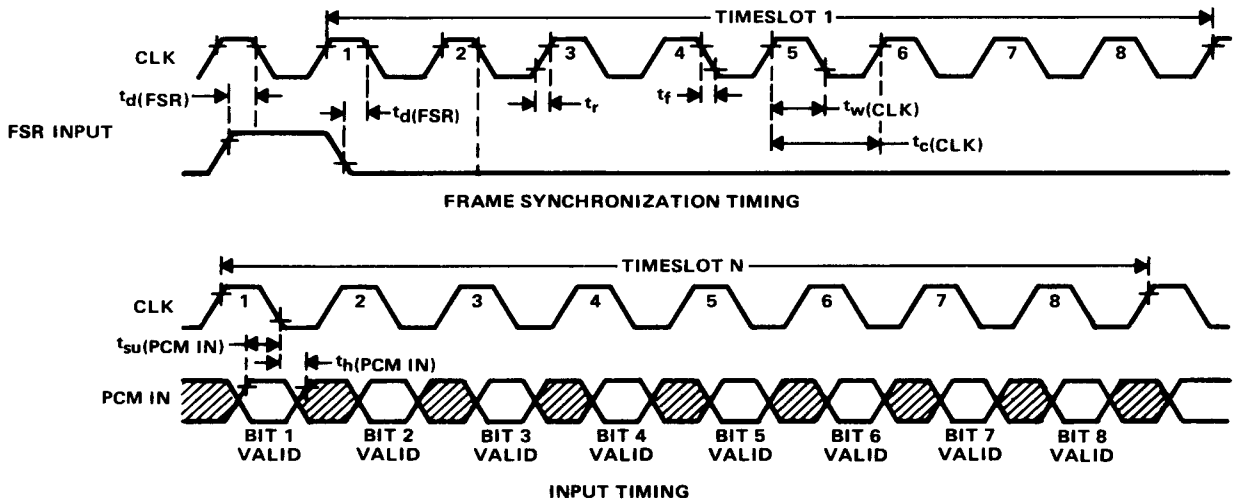


FIGURE 4. RECEIVE TIMING (FIXED-DATA-RATE)

NOTES: A. Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

B. Bit 1 is the most significant bit (MSB) and is clocked in first on the PCM IN input or is clocked out first on the PCM OUT output. Bit 8 is the least significant bit (LSB) and is clocked in last on the PCM IN input or is clocked out last on the PCM OUT output.

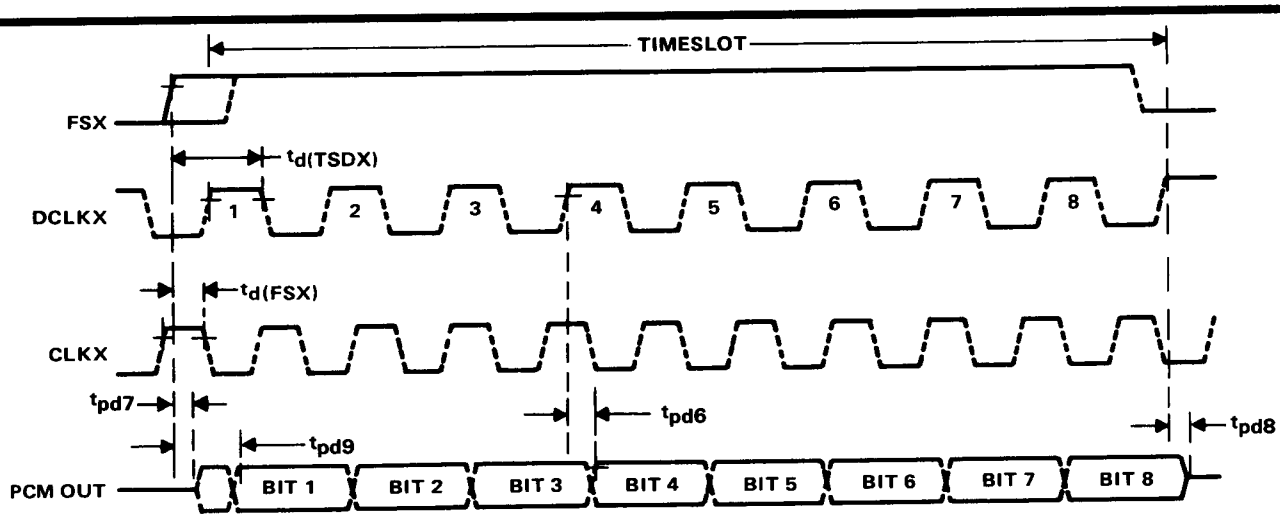
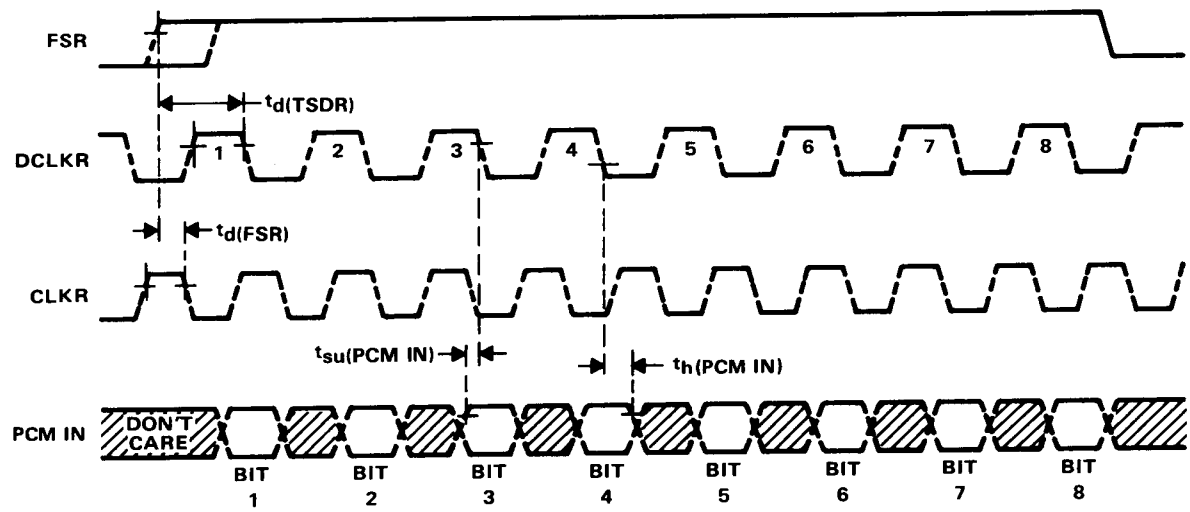


FIGURE 5. TRANSMIT TIMING (VARIABLE-DATA-RATE)



NOTE: All timing parameters referenced to V_{IH} and V_{IL} except t_{pd7} and t_{pd8}, which reference a high-impedance state.

FIGURE 6. RECEIVE TIMING (VARIABLE-DATA-RATE)

ADVANCE INFORMATION

GENERAL OPERATION

system reliability features

The TCM29C18 and TCM29C19 are powered up in four steps:
V_{CC} and V_{BB} supply voltages are applied.
All clocks are connected.
TTL high is applied to $\overline{PDN}$.
FSX and/or FSR synchronization pulses are applied.

On the transmit channel, digital outputs PCM OUT and $\overline{TSX}$ are held in high-impedance state for approximately four frames (500 μs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Thus valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

To further enhance system reliability, PCM OUT and $\overline{TSX}$ will be placed in a high-impedance state approximately 20 μs after an interruption of CLKX. These interruptions could possibly occur with some kind of fault condition.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external TTL low signal is applied to the $\overline{PDN}$ pin. It is not sufficient to remove the TTL high voltage to $\overline{PDN}$. In the absence of a signal, the $\overline{PDN}$ pin floats to TTL high and the device remains active. In the power-down mode, the average power consumption is reduced to an average of 5 mW.

The standby modes give the user the option of putting the entire device on standby, putting only the transmit channel on standby, or putting only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held at TTL low. For transmit-only operation, FSX is high and FSR is held low. For receive-only operation, FSR is high and FSX is held low. See Table 1 for power down and standby procedures.

TABLE 1. POWER DOWN AND STANDBY PROCEDURES

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ = TTL low	5 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state
Entire device on standby	FSX and FSR are TTL low	12 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state
Only transmit on standby	FSX is TTL low FSR is TTL high	70 mW	$\overline{TSX}$ and PCM OUT are placed in a high-impedance state within 300 ms.
Only receive on standby	FSR is TTL low FSX is TTL high	110 mW	

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fixed-data-rate timing (see Figure 7)

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB}. It uses master clock CLK, frame synchronizer clocks FSX and FSR, and output $\overline{TSX}$. FSX and FSR are 8-kHz inputs that set the sampling frequency. Data is transmitted on the PCM OUT pin on the first eight positive transitions of CLK following the rising edge of FSX. Data is received on the PCM IN pin on the first eight falling edges of CLK following FSX. A digital-to-analog (D/A) conversion is performed on the received digital word and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The TCM29C18 operates at 2.048 MHz only. The TCM29C19 operates at 1.536 MHz only.

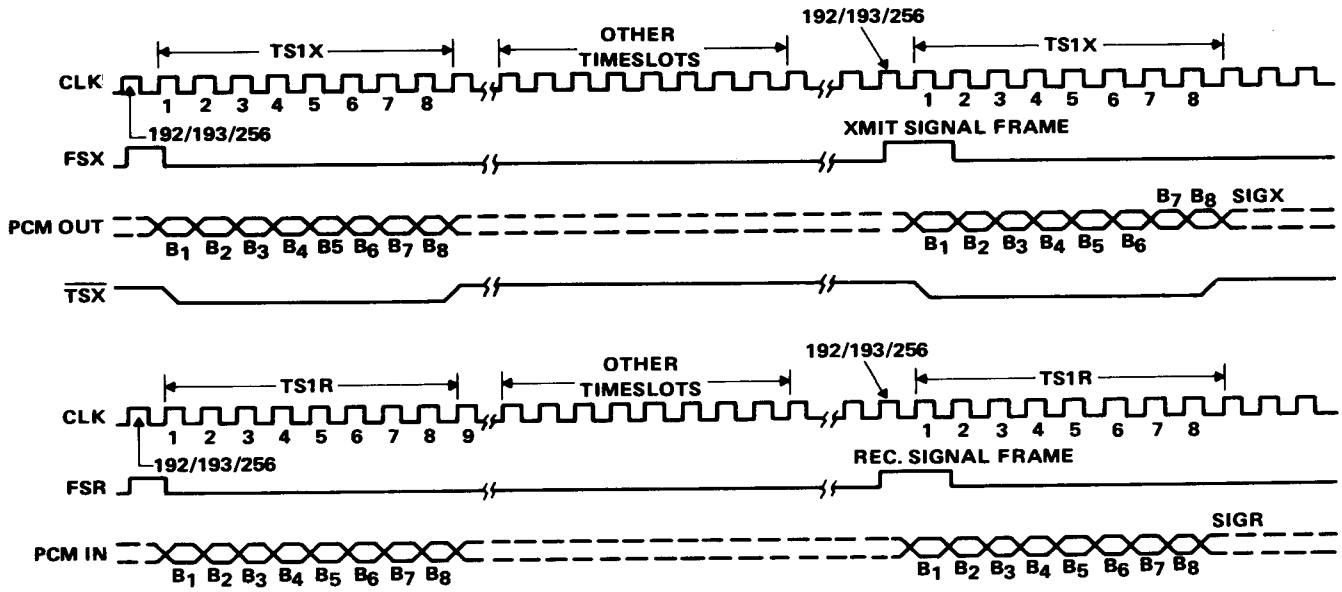

FIGURE 7. SIGNALING TIMING (FIXED-DATA-RATE ONLY)

variable data rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clock CLK, bit clocks DCLKX and DCLKR, and frame synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 2.048 MHz. The bit clocks must be synchronous in the TCM29C18 and TCM29C19. The master clock for the TCM29C18 and TCM29C19 is restricted to 2.048 MHz.

While FSX/TSXE input is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word will be repeated in all remaining timeslots in the 125 μs frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, is available only with variable-data-rate timing.

asynchronous operation

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. Specifically, in the variable-data-rate mode the rising edge of CLK must occur within $t_{d(FSX)}$ ns before the rise of FSX, while the leading edge of DCLKX must occur within t_{TSDX} ns of the rise of FSX. CLK and DCLKX are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (see variable data rate timing diagrams). This approach requires the provision of two separate master clocks but avoids the use of a synchronizer, which can cause intermittent data conversion errors.

transmit operation

transmit filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. The load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on the ANLG IN pin can be either ac or dc coupled. The input operational amplifier can also be used in the inverting mode or differential amplifier mode.

A low-pass antialiasing section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The TCM29C18 and TCM29C19 specifications meet or exceed digital class 5 central office switching systems requirements.

A high-pass section configuration was chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder performs an analog-to-digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder. The autozero circuit uses the sign bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

receive operation

decoding

The serial PCM word is received at the PCM IN pin on the first eight data clock bits of the frame. Digital-to-analog conversion is performed and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides passband flatness and stopband rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive output power amplifiers

A balanced output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single-ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output will directly drive a bridged load. The output stage is capable of driving loads as low as 300 ohms single-ended to a level of 12 dBm or 600 ohms differentially to a level of 15 dBm.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

output gain

The TCM29C18 and TCM29C19 are internally connected to set the PWRO+ and PWRO− to 0 dBm.