

HM6207H Series

256 k High Speed SRAM (256-kword × 1-bit)

HITACHI

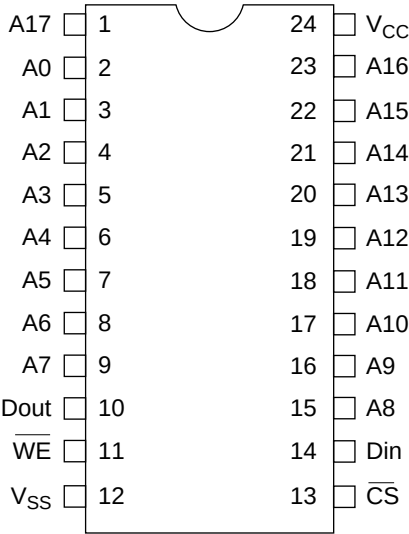
Features

- Single 5 V supply and high density 24-pin package
- High speed
Access time: 25/35/45 ns (max)
- Low power
 - Operation: 300 mW (typ)
 - Standby: 100 μ W (typ)
30 μ W (typ) (L-version)
- Completely static memory required, no clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible, all inputs and outputs
- Battery backup operation capability (L-version)

Ordering Information

Type No.	Access Time	Package
HM6207HP-25	25 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6207HP-35	35 ns	
HM6207HP-45	45 ns	
HM6207HLP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6207HLP-35	35 ns	
HM6207HLP-45	45 ns	
HM6207HJP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6207HJP-35	35 ns	
HM6207HJP-45	45 ns	
HM6207HLJP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6207HLJP-35	35 ns	
HM6207HLJP-45	45 ns	

Pin Arrangement

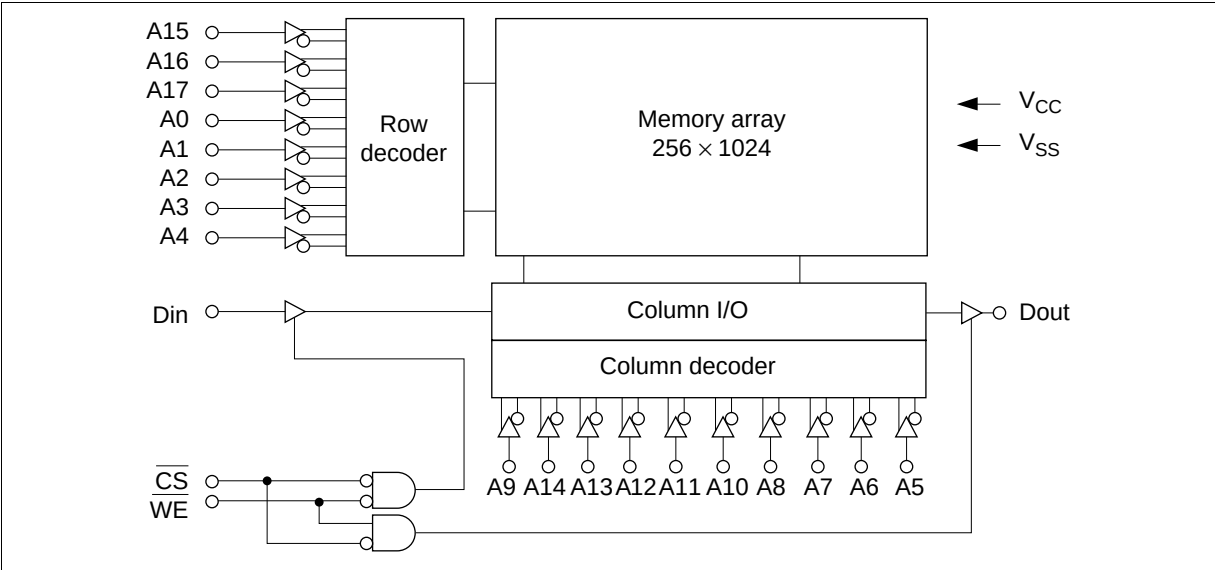


(Top view)

Pin Description

Pin Name	Function
A0–A17	Address
Din	Data input
Dout	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{\text{CS}}$	$\overline{\text{WE}}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not selected	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
L	H	Read	I_{CC}	Dout	Read cycle
L	L	Write	I_{CC}	High-Z	Write cycle

Note: × = Don't care.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{in}	-0.5^1 to +7.0	V
Power dissipation	P_{T}	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	-55 to +125	°C
Storage temperature range under bias	T_{bias}	-10 to +85	°C

Note: 1. $V_{\text{in min}} = -2.5$ V for pulse width < 10 ns.

HM6207H Series

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input high (logic 1) voltage	V _{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V _{IL}	−0.5 ^{*1}	—	0.8	V

Note: 1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	HM6207H-25			HM6207H-35/45			Unit	Test Conditions
		Min	Typ ^{*1}	Max	Min	Typ ^{*1}	Max		
Input leakage current	I _{LI}	—	—	2.0	—	—	2.0	μA	V _{CC} = Max, Vin = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	—	10.0	—	—	10.0	μA	$\overline{CS} = V_{IH}$, V _{I/O} = V _{SS} to V _{CC}
Operating power supply current	I _{CC}	—	60	120	—	50	100	mA	CS = V _{IL} , I _{I/O} = 0 mA, min cycle, duty = 100%
	I _{CC1}	—	40	80	—	40	80	mA	$\overline{CS} = V_{IL}$, I _{I/O} = 0 mA, t cycle = 50 ns, duty = 100%
Standby power supply current	I _{SB}	—	20	40	—	15	30	mA	$\overline{CS} = V_{IH}$, min cycle
Standby power supply current (1)	I _{SB1}	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS} \geq V_{CC} - 0.2$ V, 0 V ≤ Vin < 0.2, or Vin ≥ V _{CC} − 0.2 V
	L- Version	—	0.006	0.1	—	0.006	0.1		
Output low voltage	V _{OL}	—	—	0.4	—	—	0.4	V	I _{OL} = 8 mA
Output high voltage	V _{OH}	2.4	—	—	2.4	—	—	V	I _{OH} = −4.0 mA

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.

Capacitance (Ta = 25°C, f = 1 MHz)^{*1}

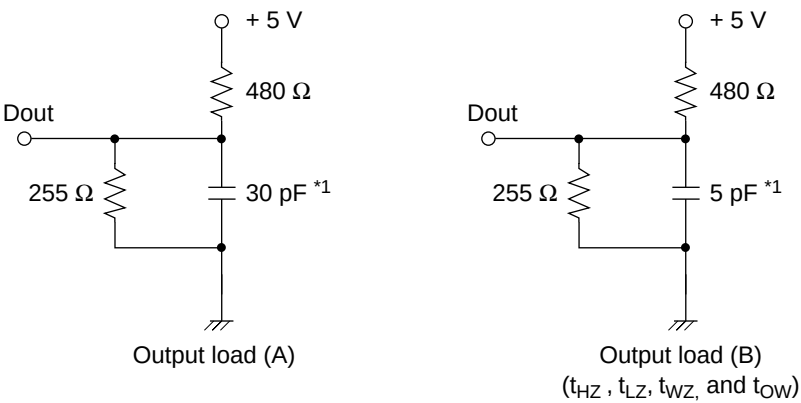
Parameter	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	10	pF	Vout = 0 V

Note: 1. This parameter is sampled and is not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10% unless otherwise noted)

Test Conditions

- Input pulse levels: V_{ss} to 3.0 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall time: 5 ns
- Output load: See figures



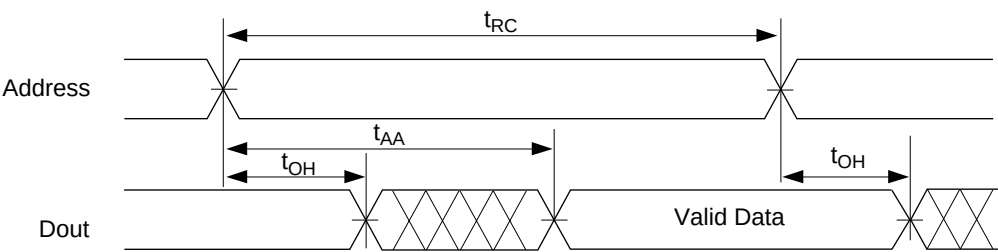
Note: 1. Including scope and jig

Read Cycle

Parameter	Symbol	HM6207H-25		HM6207H-35		HM6207H-45		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	35	—	45	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}^{*1}	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}^{*1}	0	15	0	20	0	20	ns

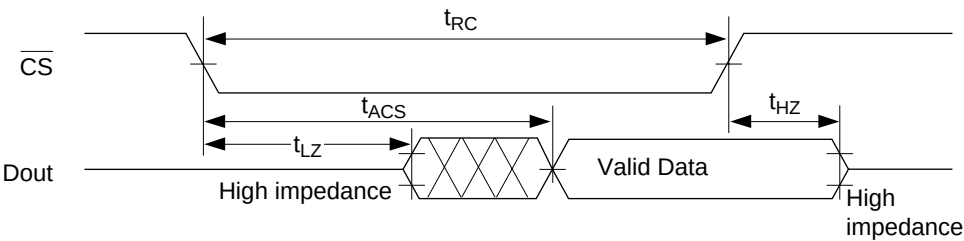
Note: 1. Transition is measured ± 200 mV from steady-state voltage with Load (B).
These parameters are sampled and not 100% tested.

Read Timing Waveform (1)



- Notes: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.

Read Timing Waveform (2)



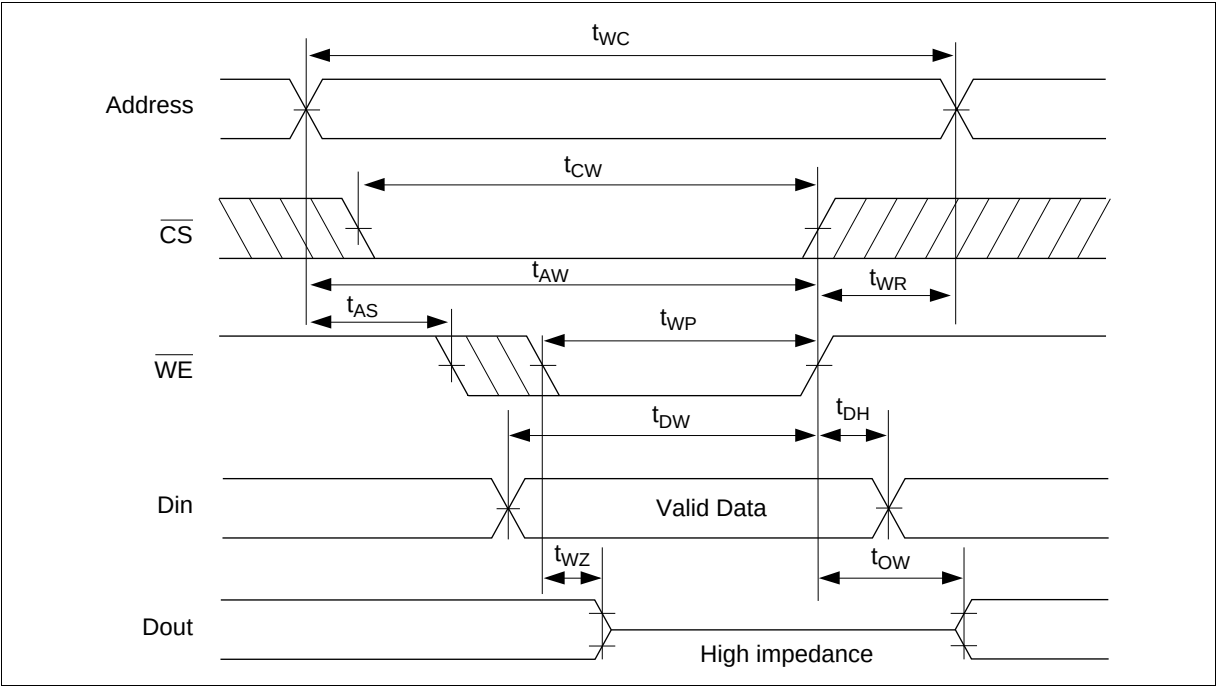
- Notes: 1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to coincident with $\overline{CS}$ transition low.

Write Cycle

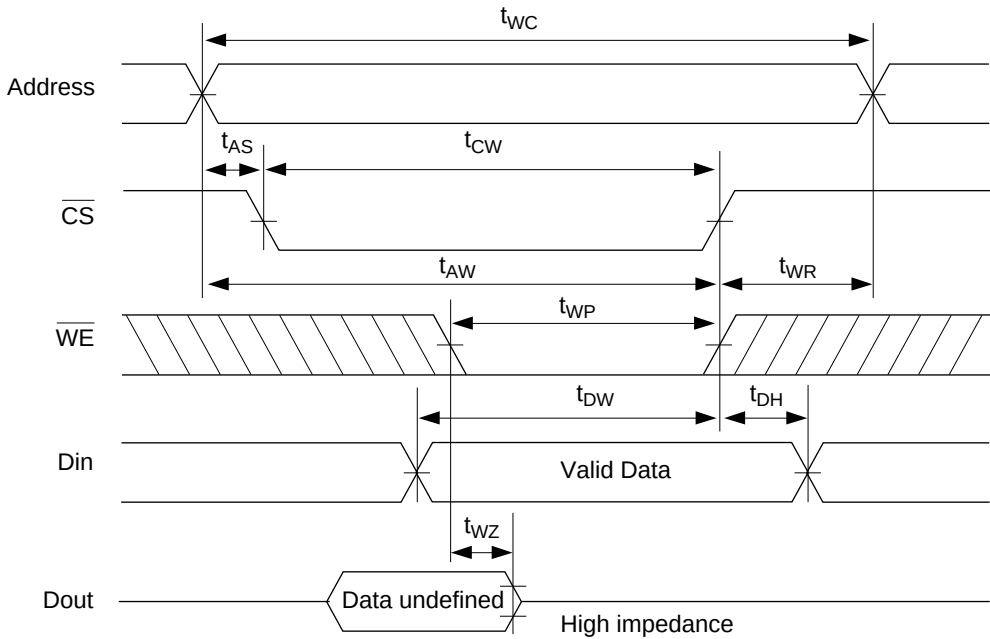
Parameter	Symbol	HM6207H-25		HM6207H-35		HM6207H-45		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	45	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	40	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	40	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	25	—	25	—	ns
Write recovery time	t_{WR}	3	—	3	—	3	—	ns
Data valid to end of write	t_{DW}	15	—	20	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Write enabled to output in high-Z ^{*1}	t_{WZ}	0	15	0	20	0	25	ns
Output active from end of write	t_{OW} ^{*1}	0	—	0	—	0	—	ns

Note: 1. Transition is measured ± 200 mV from high-impedance voltage with Load (B).
This parameter is sampled and is not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{\text{CE}}$ Controlled)



- Notes:
1. A write occurs during the overlap of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.
 2. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of the write cycle.
 3. If the $\overline{\text{CS}}$ low transition occurs simultaneously with the $\overline{\text{WE}}$ low transition, the output buffers remain in a high impedance state.
 4. Dout has the same phase as write data in this write cycle, if t_{WR} is long enough.

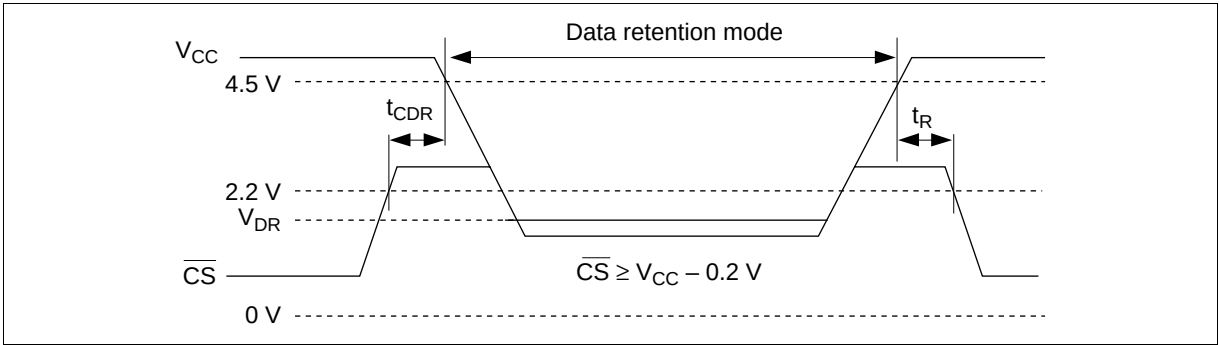
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

These characteristics are guaranteed for the L-version only.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V _{CC} for data retention	V _{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$, $V_{in} \geq V_{CC} - 0.2\text{ V}$, or $0\text{ V} \leq V_{in} \leq 0.2\text{ V}$
Data retention current	I _{CCDR}	—	2	50 ⁻¹	μA	
Chip deselect to data retention time	t _{CDR}	0	—	—	ns	
Operation recovery time	t _R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform

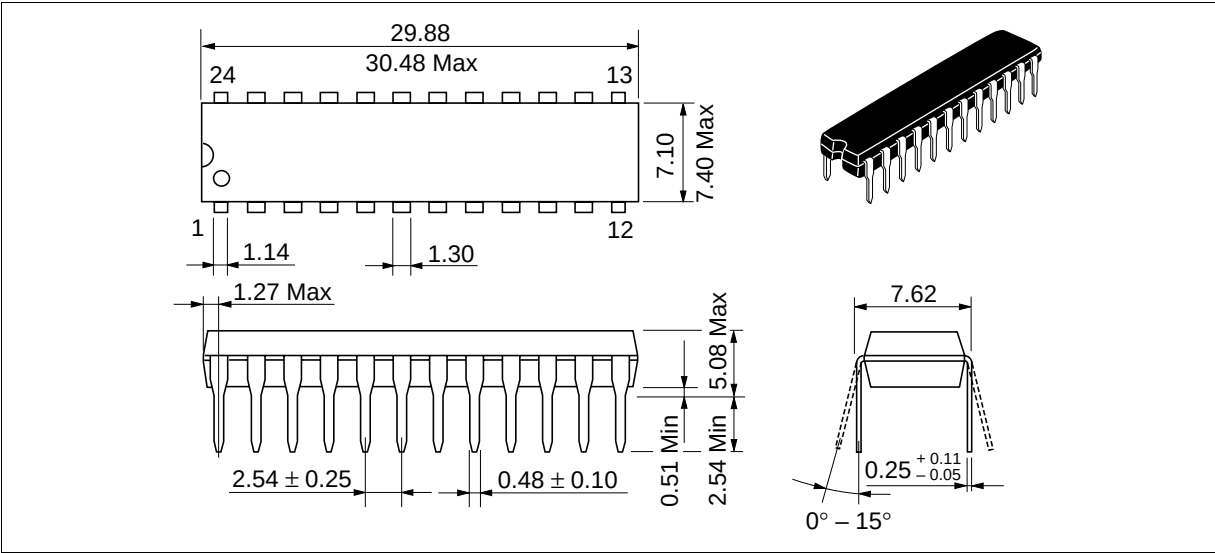


HM6207H Series

Package Dimensions

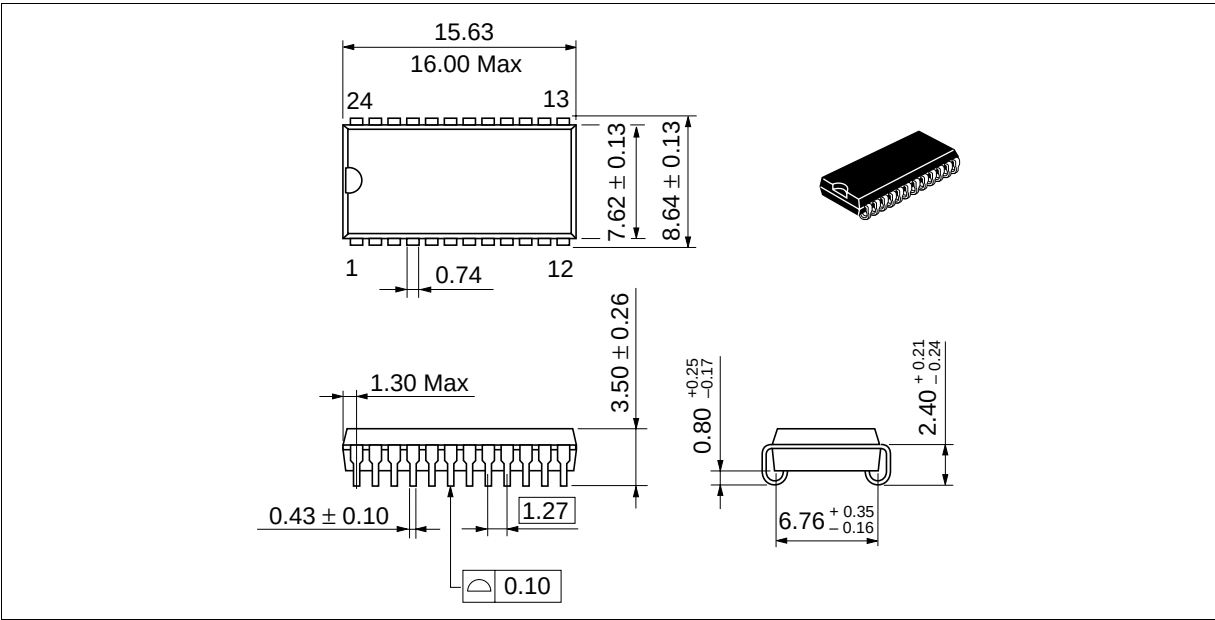
HM6207HP/HLP Series (DP-24NC)

Unit: mm



HM6207HJP/HLJP Series (CP-24D)

Unit: mm



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