

N-channel enhancement mode vertical DMOS FET

ZVN4206

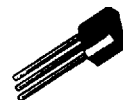
ZETEX SEMICONDUCTORS

FEATURES

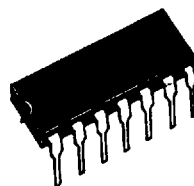
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

A compact cell geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.



E-LINE (TO-92)
SUFFIX A or C



14 LEAD MOULDED DIL
SUFFIX E

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN4206A	60V	0.6 A	1Ω
ZVN4206C	60V	0.6 A	1Ω
ZVN4206E	60V	0.6 A	1Ω

ZVN4206**ZETEX SEMICONDUCTORS****ABSOLUTE MAXIMUM RATINGS**

Parameters		E-line	DIL	Unit
V_{DS}	Drain-source voltage	60	60	V
I_D	Continuous drain current (@ $T_A = 25^\circ\text{C}$)	0.6	0.6	A
I_{DM}	Pulsed drain current	8	3	A
V_{GS}	Gate-source voltage	± 20	± 20	V
P_D	Max. power dissipation (@ $T_A = 25^\circ\text{C}$)	0.7	0.85	W
T_J, T_{stg}	Operating/storage temperature range	- 55 to + 150		$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (at $T = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	—	V	$I_D = 1\text{mA}$, $V_{GS} = 0\text{V}$
$V_{GS(th)}$	Gate-source threshold voltage	1.3	3	V	$I_D = 1\text{mA}$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	—	100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
I_{DSS}	Zero gate voltage drain current	—	10	μA	$V_{DS} = \text{Max. rating}$, $V_{GS} = 0\text{V}$
		—	100	μA	$V_{DS} = 0.8 \times \text{Max. rating}$ $V_{GS} = 0\text{V}$ ($T = 125^\circ\text{C}$) (2)
$I_{D(on)}$	On-state drain current (1)	3	—	A	$V_{DS} = 25\text{V}$, $V_{GS} = 10\text{V}$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	—	1	Ω	$I_D = 1.5\text{A}$, $V_{GS} = 10\text{V}$
		—	1.5	Ω	$I_D = 0.5\text{A}$, $V_{GS} = 5\text{V}$
g_{fs}	Forward transconductance (1) (2)	0.3	—	S	$V_{DS} = 25\text{V}$, $I_D = 1.5\text{A}$
C_{iss}	Input capacitance (2)	—	100	pF	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
C_{oss}	Common source output capacitance (2)	—	60	pF	
C_{rss}	Reverse transfer capacitance (2)	—	20	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	—	8	ns	$V_{DD} \approx 25\text{V}$, $I_D = 1.5\text{A}$
t_r	Rise time (2) (3)	—	12	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	—	12	ns	
t_f	Fall time (2) (3)	—	15	ns	

(1) Measured under pulsed conditions. Width = $300\mu\text{s}$. Duty cycle $\leq 2\%$.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and $< 5\text{ns}$ rise time on a pulse generator.

SOURCE - DRAIN DIODE CHARACTERISTICS

Parameter	Typ.	Unit	Conditions
V _{SD} Diode forward voltage (1)	0.85	V	V _{GS} = 0V, I _S = 0.6A
t _{rr} Reverse recovery time	70	ns	V _{GS} = 0V, I _F = 0.6A I _R = 0.1A

- (1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.
- (2) Sample test.
- (3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

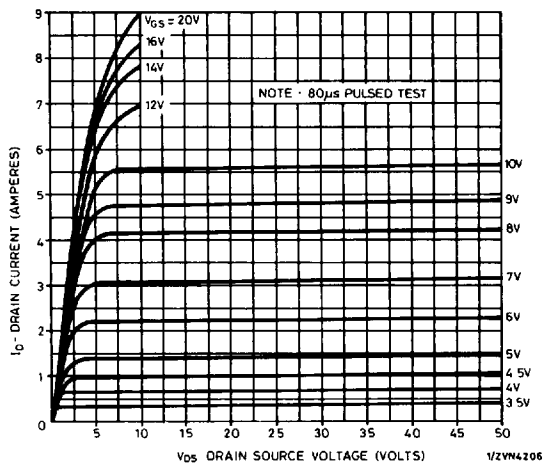


Fig. 1 Typical output characteristics

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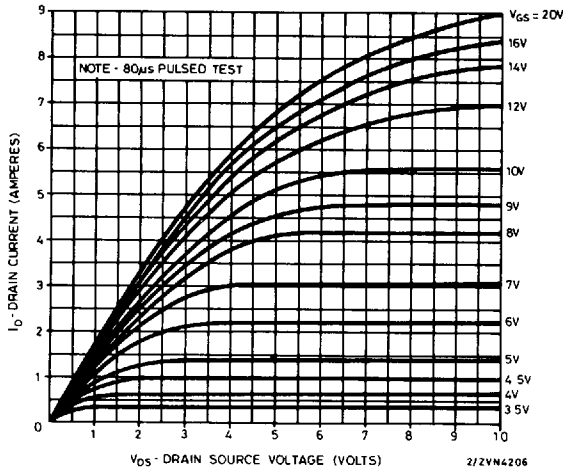


Fig. 2 Typical saturation characteristics

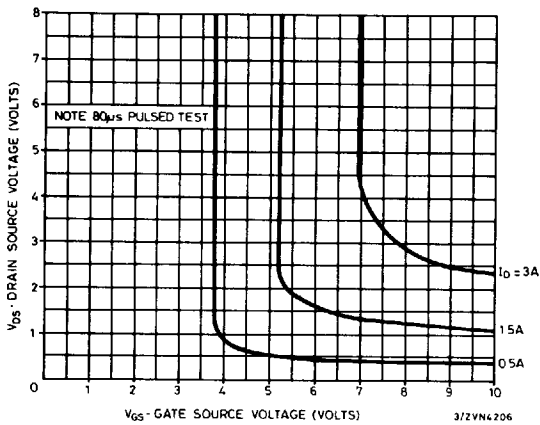


Fig. 3 Typical voltage saturation characteristics

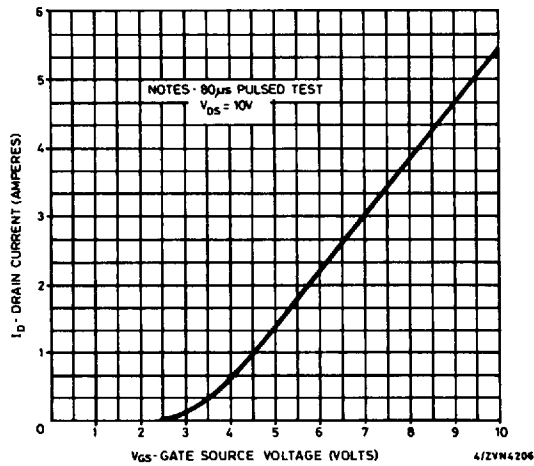


Fig. 4 Typical transfer characteristics

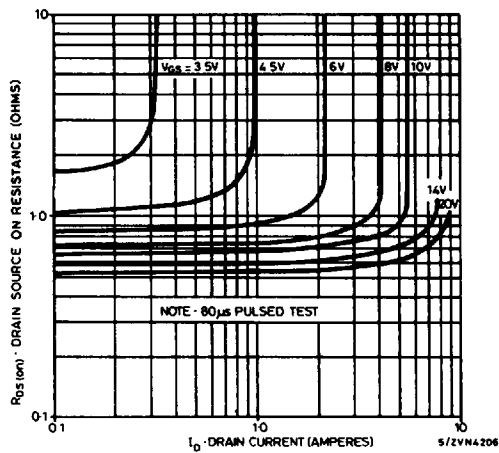
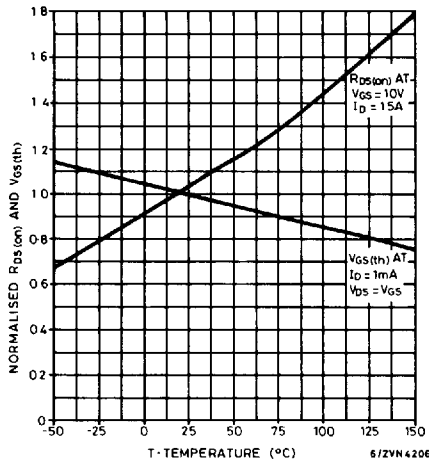
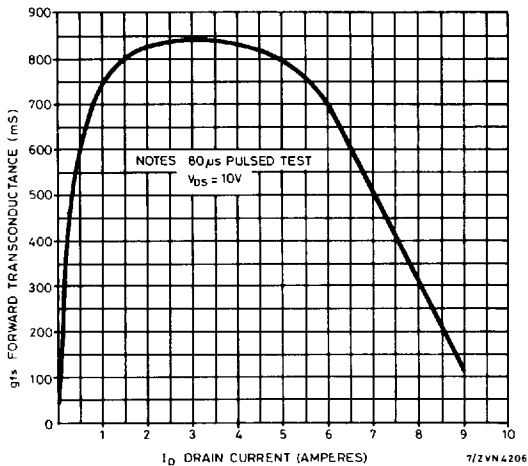


Fig. 5 Typical on-resistance v drain current

ZVN4206**ZETEX SEMICONDUCTORS****Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature****Fig. 7 Typical transconductance v drain current**

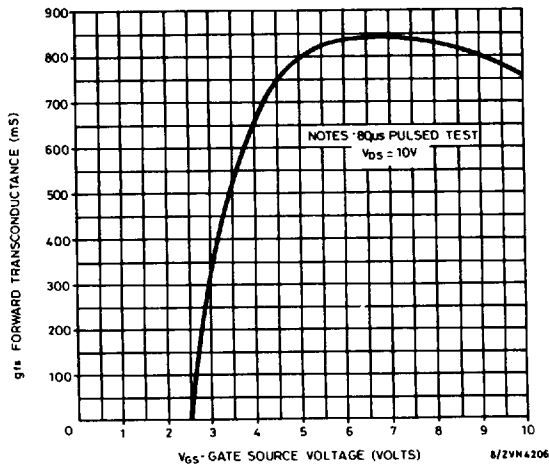


Fig. 8 Typical transconductance v gate-source voltage

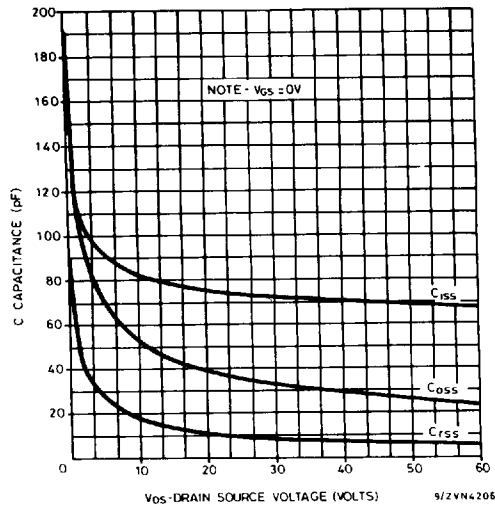


Fig. 9 Typical capacitance v drain-source voltage

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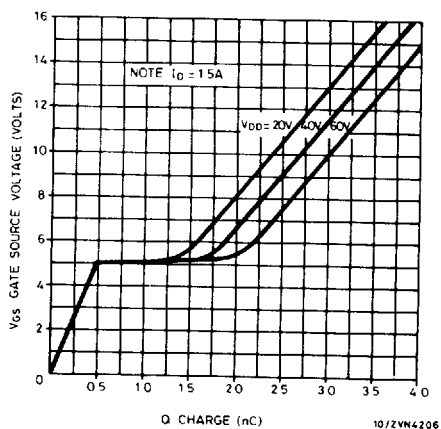


Fig. 10 Typical gate charge v gate-source voltage

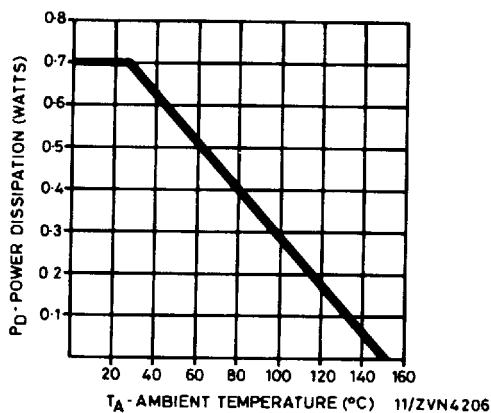


Fig. 11 Power v temperature derating curve (ambient)