NCP1521BEVB

NCP1521B Adjustable Output Voltage Step-Down Converter Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Overview

The NCP1521B step−down PWM DC−DC converter is optimized for portable applications powered from one cell Li−ion or three cell Alkaline/NiCd/NiMH batteries.

The part is available in adjustable output voltage versions ranging from 0.9 V to 3.3 V. It uses synchronous rectification to increase efficiency and reduce external part count. The device also has a built−in 1.5 MHz (nominal) oscillator which reduces component size by allowing smaller inductors and capacitors. Automatic switching PWM/PFM mode offers improved system efficiency.

Additional features include integrated soft−start, cycle−by−cycle current limiting and thermal shutdown protection. The NCP1521B is available in space saving, low profile TSOP5 and UDFN6 packages.

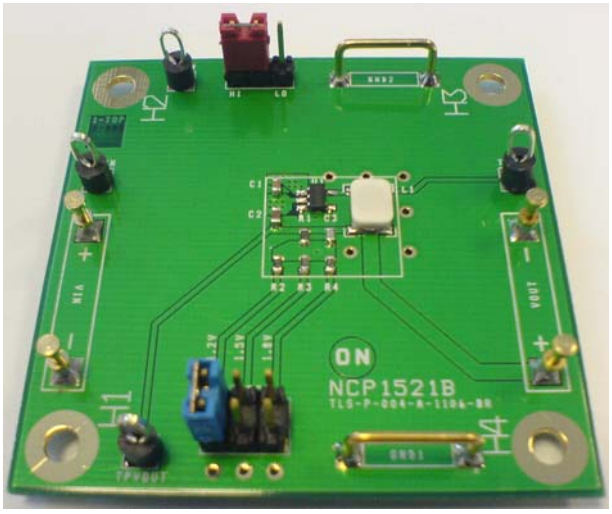

Figure 1. Board Picture in TSOP−5

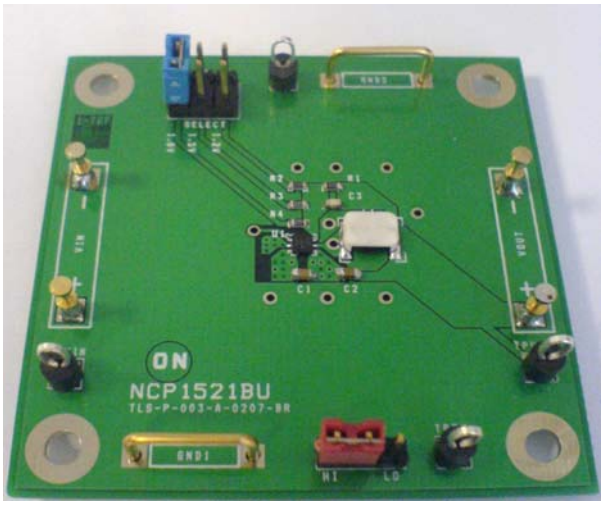

Figure 2. Board Picture in μDFN−6

MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum−rated conditions is not implied. Functional operation should be restricted to the Recommend Operating Conditions (Note 1).

Rating		Symbol	Value	Unit
Minimum Voltage All Pins		V_{min}	−0.3	V
Maximum Voltage All Pins (Note 2)		V_{max}	7.0	V
Maximum Voltage EN1, EN2, FB, LX		V_{max}	V_{IN} + 0.3	V
Thermal Resistance Junction−to−Air	TSOP−5 UDFN−6	$R_{\theta ja}$	300 260	°C/W
Operating Ambient Temperature Range		T_A	−40 to 85	°C
Storage Temperature Range		T_{stg}	−55 to 150	°C
Junction Operating Temperature		T_J	−40 to 125	°C
Latch−up current maximum rating Ta=85°C (Note 4) other pins		L_u	±100	mA
ESD Withstand Voltage (Note 3)	Human Body Model Machine Model	V_{esd}	2.0 200	kV V
Moisture Sensitivity Level (Note 5)		MSL	1	per IPC

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C
2. According JEDEC standard JESD22−A108B
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) per JEDEC standard: JESD22−A114
   Machine Model (MM) per JEDEC standard: JESD22−A115
4. Latchup current maximum rating per JEDEC standard: JESD78.
5. JEDEC Standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS

For Electrical Characteristic, please see our NCP1521B datasheet available at
http://www.onsemi.com/PowerSolutions/product.do?id=NCP1521B

NCP1521B – BOARD CONNECTIONS

Symbol	Switch Descriptions
INPUT POWER	
V_{IN}+	This is the positive connection for power supply.
V_{IN}−	This is the return connection for the power supply
GND1, GND2	Ground clip
SETUP	
ENABLE	To enable the buck converter, connect a shorting jumper between ENABLE−1 and ENABLE−2. To disable the buck converter, connect a shorting jumper between ENABLE−3 and ENABLE−2.
SELECT	A shorting jumper must be used to select an output voltage of 1.2 V, 1.5 V or 1.8 V
OUTPUT POWER	
V_{OUT}+	This is the positive connection of the output voltage.
V_{OUT}−	This is the return connection of the output voltage.
TEST POINT	
T_{PVIN}	This is the test point of the input voltage.
T_{PEN}	This is the test point of the enable pin.
T_{PLX}	This is the test point of the inductor voltage.
T_{PVOUT}	This is the test point of the output voltage.

NCP1521B – BOARD SCHEMATIC

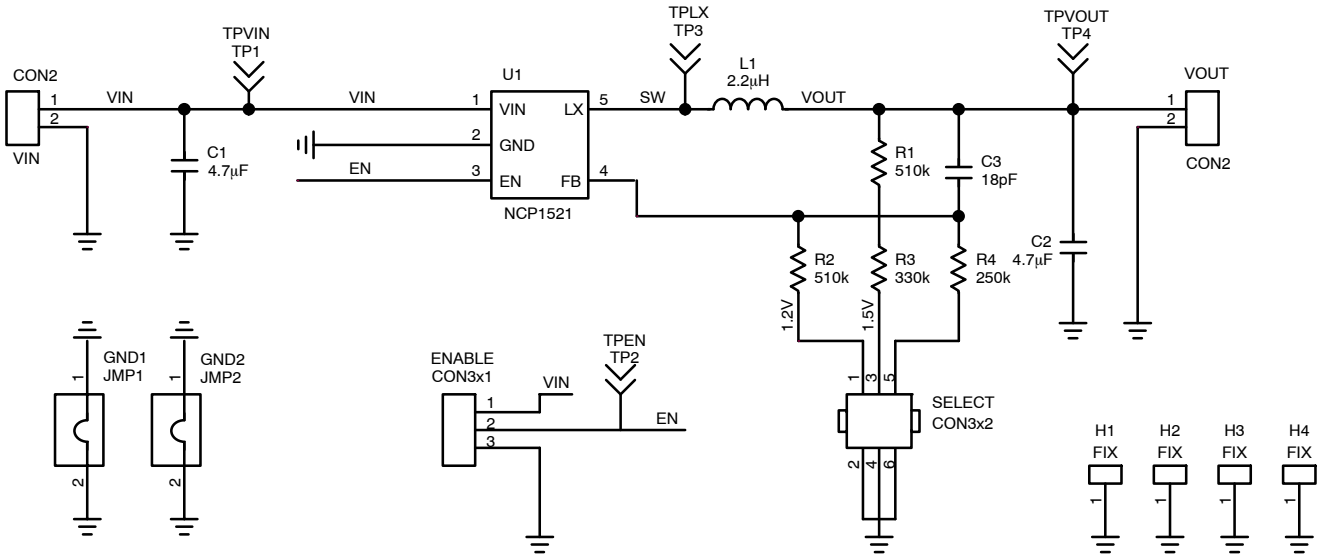

Figure 3. Board Schematic in TSOP−5

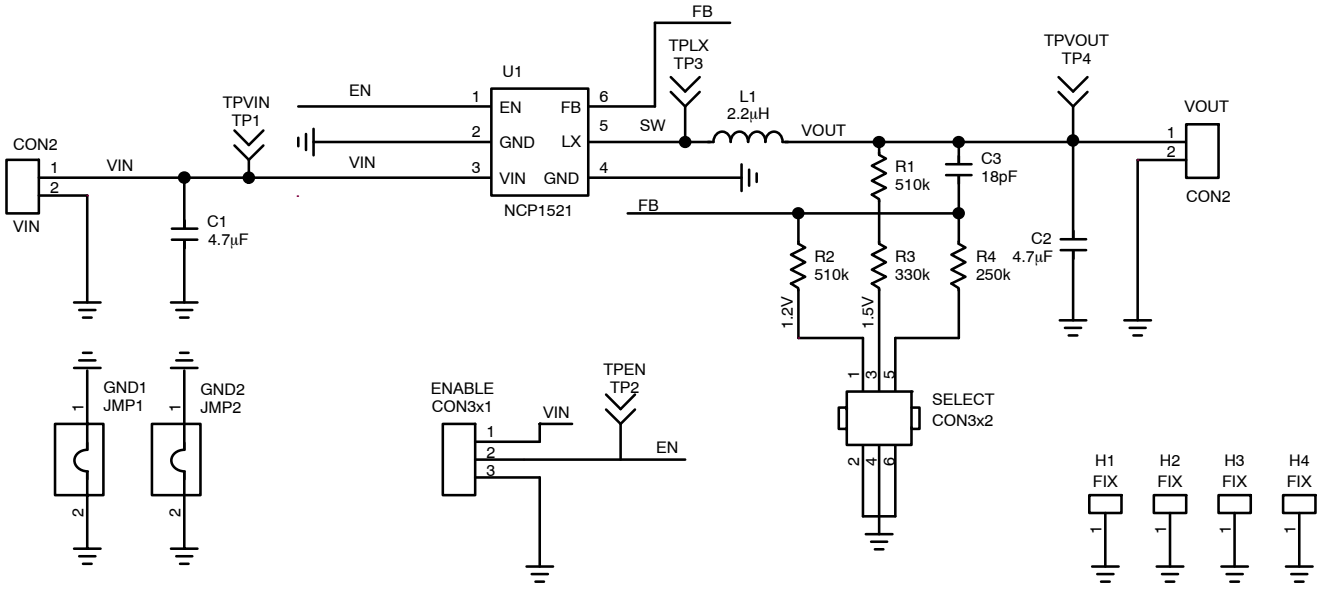

Figure 4. Board Schematic in μDFN−6

NCP1521B – TEST PROCEDURE

Equipment needed

- 10 pt. Times *(list:bull2)*
- Power supply
- Digital Volt Meter
- Digital Amp Meter

Test

1. Jumper ENABLE should be open.
2. Jumper SELECT should be closed to 1.2 V.
3. Set the power supply to 3.6 V and the current limit of at least 800 mA.
4. Connect the power supply connector to connectors V_{IN}+ and V_{IN}−. The DC current measurement on V_{IN} line should be around 0.3 μA.
5. Close ENABLE connector. The DC current measurement on V_{IN} line should be around 40 μA.
6. Measure the output voltage between V_{OUT}+ and V_{OUT}− connectors. You should see around 1.2 V voltage operation.
7. Remove the ENABLE jumper. The DC current measurement on V_{IN} line should be back around 0.3 μA.

NCP1521B – BILL OF MATERIAL

Designator	Qty	Description	Value	Toler-ance	Foot-print	Manufacturer	Manufacturer Part Number
U1	1	IC, Converter, DC/DC	NA	NA	TSOP5 UDFN	ON Semiconductor	NCP1521B NCP1521BU
C1	1	Ceramic capacitor	4.7 μF, 10 V, X5R	10%	0805	TDK	C1608X5R1A475
C2	1	Ceramic capacitor	10 μF, 6,3 V, X5R	10%	0603	TDK	C1608X5R0J105
C3	1	Ceramic capacitor	18 pF, 50 V, COG	5%	0603	TDK	C1608C0G1H180
R1, R2	2	SMD resistor	510k	1%	0603	std	std
R3	1	SMD resistor	330k	1%	0603	std	std
R4	1	SMD resistor	240k	1%	0603	std	std
L1	1	Inductor	2.2 μH	30%	1210	Coilcraft	LPS3008−222NL
VIN, VOUT	4	Connector	NA	NA	NA	Kontek Comatel Cambion	3110014000500 160−1724−02−05−00
ENABLE	1	3 Pin Jumper Header	NA	NA	2.54mm	TYCO/AMP Molex / Waldom	5−826629−0 90120−0160
SELECT	1	3x2 Pin Jumper Header	NA	NA	2.54mm	TYCO/AMP Molex / Waldom	4731955180470 90131−0140
GND1, GND2	2	Jumper for GND	NA	NA	10.16mm	Harwin Molex / Waldom	D3082−01 90120−0160
TPEN, TPLX, TPVIN, TPVOUT	4	Test point type 3	NA	NA	ϕ1.60mm	Keystone	5010
PCB	1	50.8mm x 50.8mm x 1.0 mm 4 Layers	NA	NA	NA	Any	TLS−P−004−A−1106−BR TLS−P−003−A−0207−BR

NCP1521B – PCB LAYOUT

Board Reference: TLS−P−004−A−1106−BR

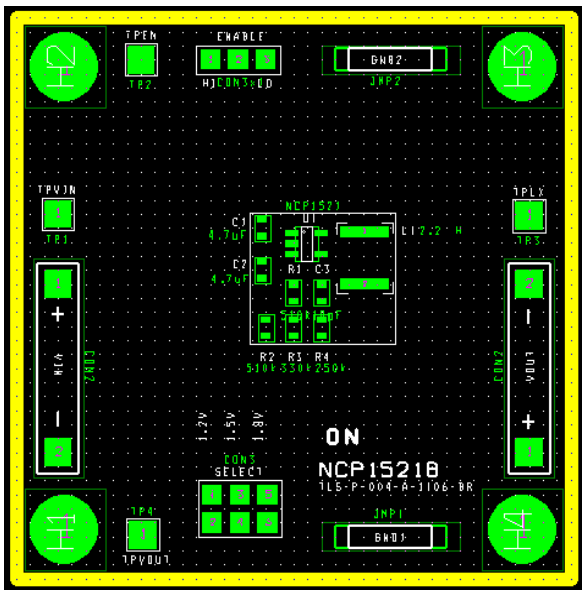

Figure 5. Assembly Layer in TSOP−5

Board Reference: TLS−P−003−A−0207−BR

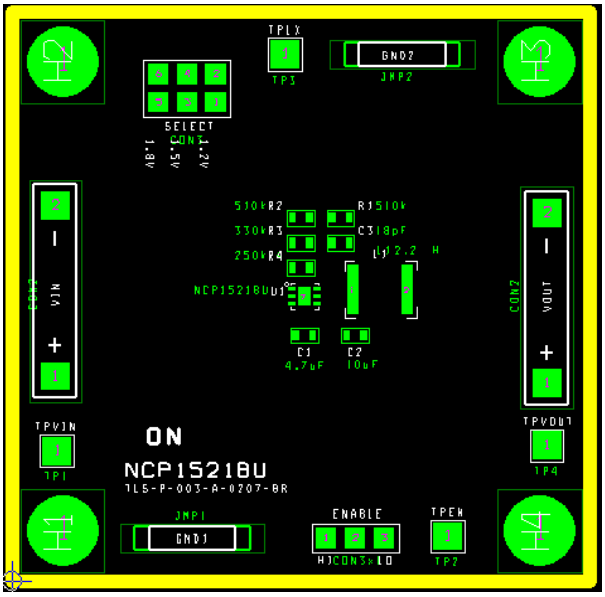

Figure 6. Assembly Layer in μDFN−6

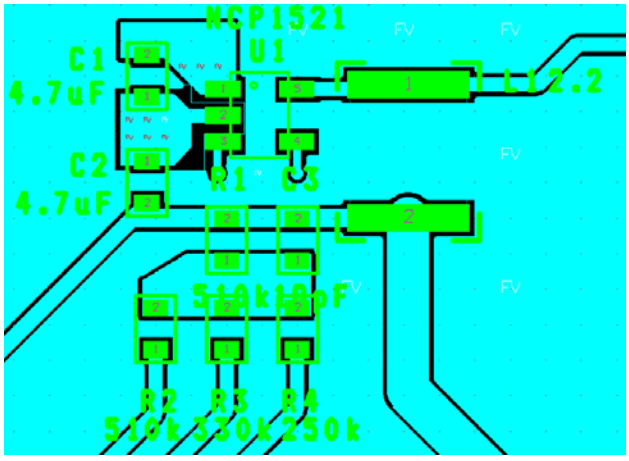

Figure 7. Part Layout in TSOP−5

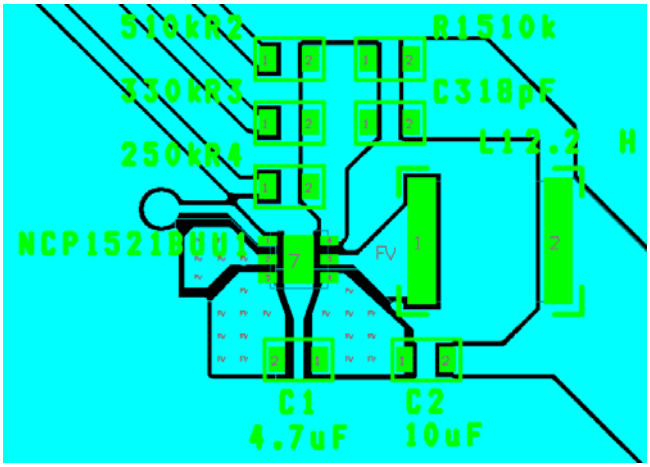

Figure 8. Part Layout in μDFN−6

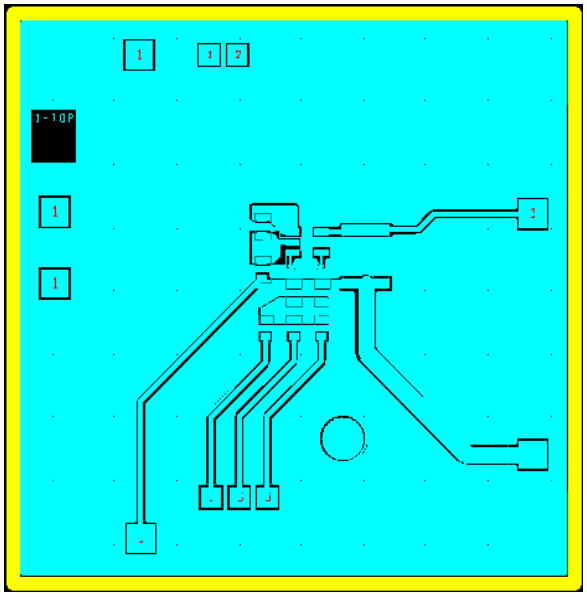

Figure 9. Top Layer Routing in TSOP−5

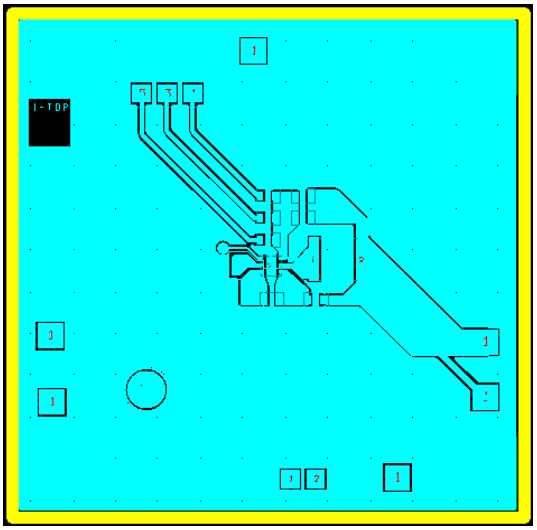

Figure 10. Top Layer Routing in μDFN−6

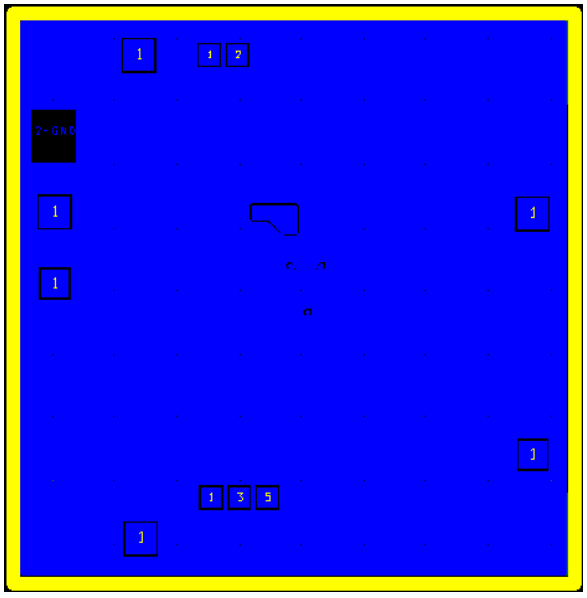

Figure 11. Ground Layer Routing in TSOP−5

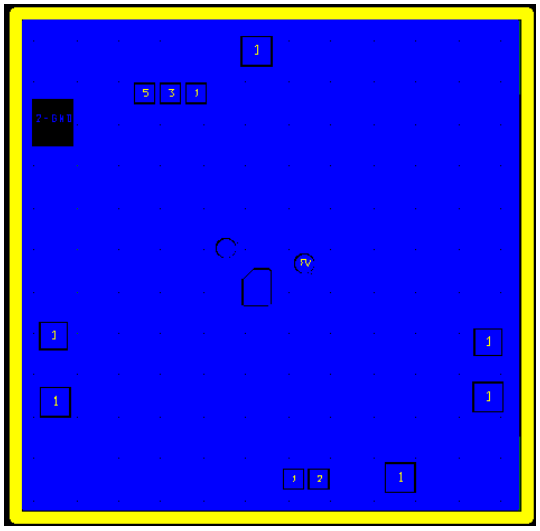

Figure 12. Ground Layer Routing in μDFN−6

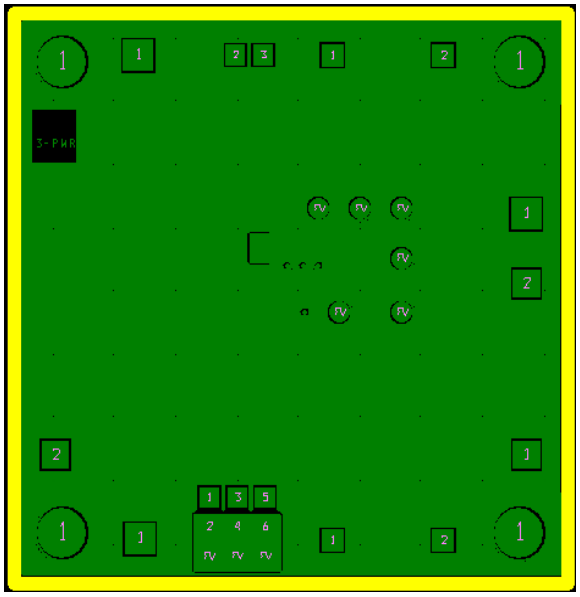

Figure 13. Power Layer Routing in TSOP−5

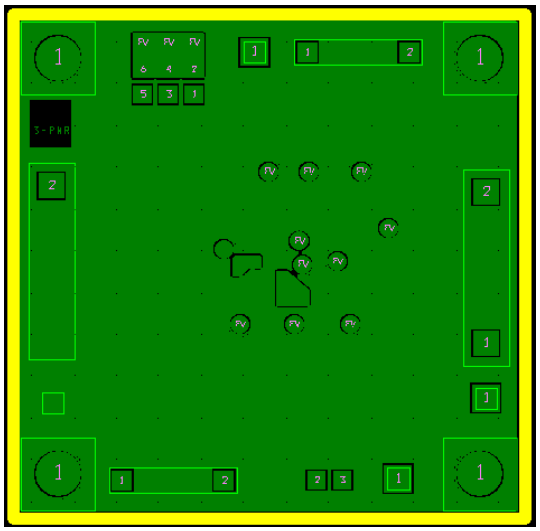

Figure 14. Power Layer Routing in μDFN−6

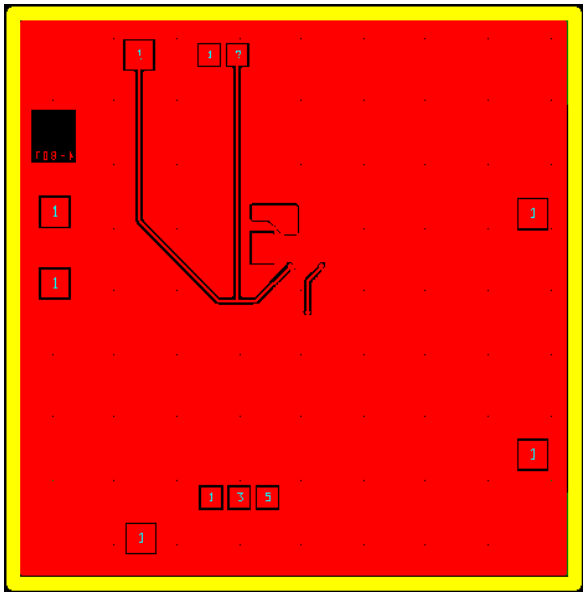

Figure 15. Bottom Layer Routing in TSOP−5

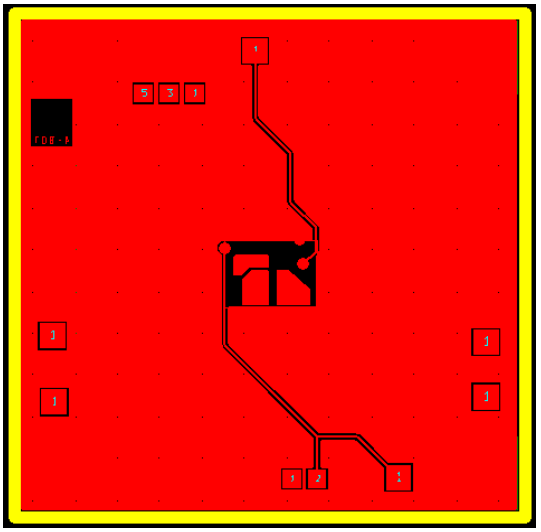

Figure 16. Bottom Layer Routing in μDFN−6

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