INTERSIL

2N3954-2N3958 Monolithic Dual N-Channel JFET

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifiers requiring low offset voltage, drift, noise, and capacitance.

FEATURES

- Offset Voltage < 5 mV • Drift < 5 μV/°C
- Low Capacitance – C_{iss} = 4 pF Max
- Spot Noise Figure = 0.5 dB Max
- Superior Tracking Ability
- Low Output Conductance – g_{os} = 35 μmho Max

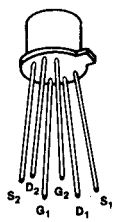
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Any Case-To-Lead Voltage	±100 V
Gate-Drain or Gate-Source Voltage	–50 V
Gate-To-Gate Voltage	±100 V
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

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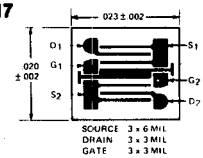

ORDERING INFORMATION

TO-71	WAFER	DICE
2N3954	2N3954/W	2N3954/D
2N3954A	2N3954A/W	2N3954A/D
2N3955	2N3955/W	2N3955/D
2N3955A	2N3955A/W	2N3955A/D
2N3956	2N3956/W	2N3956/D
2N3957	2N3957/W	2N3957/D
2N3958	2N3958/W	2N3958/D

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ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3954		2N3954A		2N3955		2N3955A		2N3956		2N3957		2N3958		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		–100		–100		–100		–100		–100		–100		–100	pA	V_{GS} = –30 V,	
			–500		–500		–500		–500		–500		–500		–500	nA	V_{DS} = 0	T_A = 125°C
BV_{GSS}	Gate-Source Breakdown Voltage	–50		–50		–50		–50		–50		–50		–50		V	V_{DS} = 0 I_G = 1 μA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1.0	–4.5	–1.0	–4.5	–1.0	–4.5	–1.0	–4.5	–1.0	–4.5	–1.0	–4.5	–1.0	–4.5	V	V_{DS} = 20 V, I_D = 1 nA	
$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		2.0		2.0		2.0		2.0	V	V_{DS} = 0 I_G = 1 mA	
V_{GS}	Gate-Source Voltage		–4.2		–4.2		–4.2		–4.2		–4.2		–4.2		–4.2	V	V_{DS} = 20 V	I_D = 50 μA
		–0.5	–4.0	–0.5	–4.0	–0.5	–4.0	–0.4	–4.0	–0.5	–4.0	–0.5	–4.0	–0.5	–4.0	V		I_D = 200 μA
I_G	Gate Operating Current		–50		–50		–50		–50		–50		–50		–50	pA	V_{DS} = 20 V,	
			–250		–250		–250		–250		–250		–250		–250	nA	I_D = 200 μA	T_A = 125°C
I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
		1000		1000		1000		1000		1000		1000		1000				f = 200 MHz
g_{os}	Common-Source Output Conductance		35		35		35		35		35		35		35			f = 1 kHz
C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0		4.0		4.0		4.0		4.0	pF		f = 1 MHz
C_{rss}	Common Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2		1.2		1.2		1.2			
C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		1.5		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
NF	Common-Source Spot Noise Figure		0.5		0.5		0.5		0.5		0.5		0.5		0.5	dB	V_{DS} = 20 V V_{GS} = 0 R_G = 10 MΩ	f = 100 Hz
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		10		10		10		10		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA	T = 125°C
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0		V_{DS} = 20 V V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		5.0		10.0		5.0		15		20		25	mV	V_{DS} = 20 V, I_D = 200 μA	
$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Differential Voltage Change with Temperature		0.8		0.4		2.0		1.2		4.0		6.0		8.0			T = 25°C to –55°C
			1.0		0.5		2.5		1.5		5.0		7.5		10.0			T = 25°C to 125°C
g_{fs1}/g_{fs2}	Transconductance Ratio	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0			f = 1 kHz