

TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Very Low Power . . . 35 μA Per Channel Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage**
850 μV Max at T_A = 25°C (TLC225xA)
- **Macromodel Included**
- **Performance Upgrades for the TS27L2/L4 and TLC27L2/L4**
- **Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards**

description

The TLC2252 and TLC2254 are dual and quaduple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC225x family consumes only 35 μA of supply current per channel. This micropower operation makes them good choices for battery-powered applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Looking at Figure 1, the TLC225x has a noise level of 19 nV/√Hz at 1kHz; four times lower than competitive micropower solutions.

The TLC225x amplifiers, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC225xA family is available and has a maximum input offset voltage of 850 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2252/4 also makes great upgrades to the TLC27L2/L4 or TS27L2/L4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage ranges, see the TLV2432 and TLV2442 devices. If the design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

**EQUIVALENT INPUT NOISE VOLTAGE
VS
FREQUENCY**

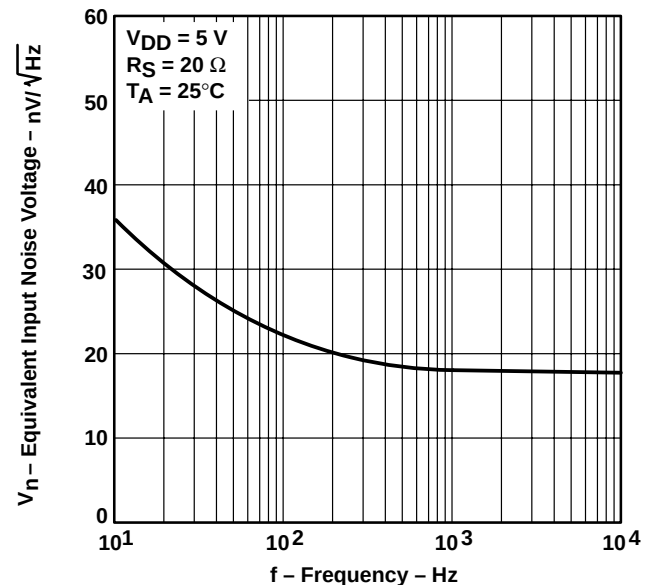


Figure 1



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TLC2252 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP‡ (PW)	CERAMIC FLATPACK (U)
0°C to 70°C	1500 µV	TLC2252CD	—	—	TLC2252CP	TLC2252CPW	—
–40°C to 125°C	850 µV 1500 µV	TLC2252AID TLC2252ID	— —	— —	TLC2252AIP TLC2252IP	TLC2252AIPW —	— —
–40°C to 125°C	850 µV 1500 µV	TLC2252AQD TLC2252QD	— —	— —	— —	— —	— —
–55°C to 125°C	850 µV 1500 µV	— —	TLC2252AMFK TLC2252MFK	TLC2252AMJG TLC2252MJG	— —	— —	TLC2252AMU TLC2252MU

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2262CDR).

‡ The PW package is available only left-ended taped and reeled.

§ Chip forms are tested at 25°C only.

TLC2254 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP‡ (PW)	CERAMIC FLATPACK (W)
0°C to 70°C	1500 µV	TLC2254CD	—	—	TLC2254CN	TLC2254CPW	—
–40°C to 125°C	850 µV 1500 µV	TLC2254AID TLC2254ID	— —	— —	TLC2254AIN TLC2254IN	TLC2254AIPW —	— —
–40°C to 125°C	850 µV 1500 µV	TLC2254AQD TLC2254QD	— —	— —	— —	— —	— —
–55°C to 125°C	850 µV 1500 µV	— —	TLC2254AMFK TLC2254MFK	TLC2254AMJ TLC2254MJ	— —	— —	TLC2254AMW TLC2254MW

† The D packages are available taped and reeled. Add R suffix to the device type (e.g., TLC2254CDR).

‡ The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

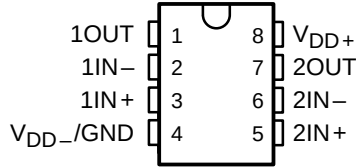
§ Chip forms are tested at 25°C only.



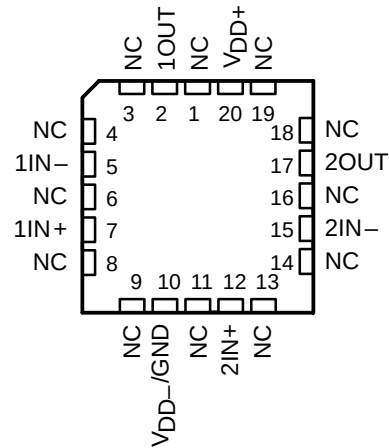
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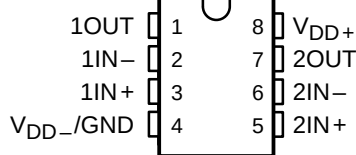
TLC2252C, TLC2252AC
TLC2252I, TLC2252AI
TLC2252Q, TLC2252AQ
D, P, OR PW PACKAGE
(TOP VIEW)



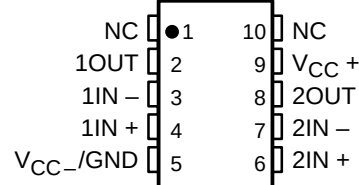
TLC2252M, TLC2252AM . . . FK PACKAGE
(TOP VIEW)



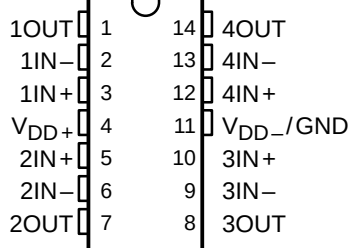
TLC2252M, TLC2252AM . . . JG PACKAGE
(TOP VIEW)



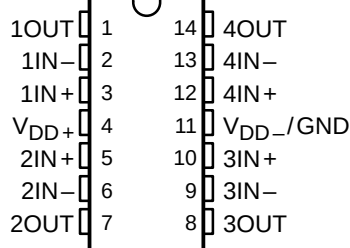
TLC2262M, TLC2252AM . . . U PACKAGE
(TOP VIEW)



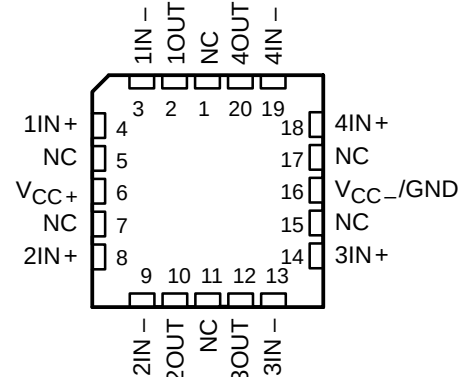
TLC2254C, TLC2254AC
TLC2254I, TLC2254AI
TLC2254Q, TLC2254AQ
D, N, OR PW PACKAGE
(TOP VIEW)



TLC2254M, TLC2254AM
J OR W PACKAGE
(TOP VIEW)



TLC2254M, TLC2254AM
FK PACKAGE
(TOP VIEW)



NC – No internal connection

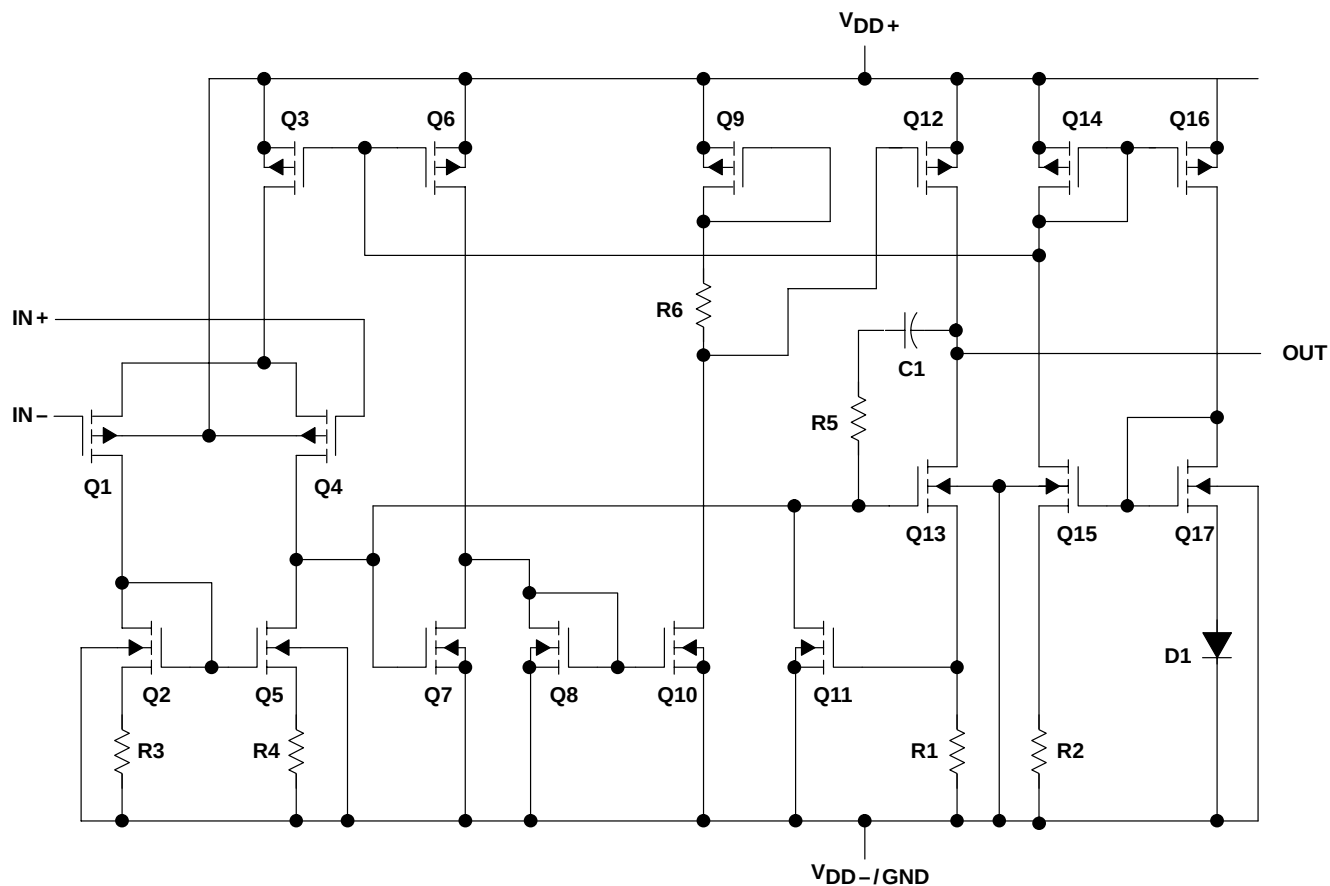
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equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLC2252	TLC2254
Transistors	38	76
Resistors	30	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage, V_I (any input, see Note 1)	±8 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of V_{DD-}	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 125°C
Q suffix	–40°C to 125°C
M suffix	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows when input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D–8	724 mW	5.8 mW/°C	464 mW	377 mW	144 mW
D–14	950 mW	7.6 mW/°C	608 mW	450 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	736 mW	—
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—
PW–8	525 mW	4.2 mW/°C	336 mW	273 mW	—
PW–14	700 mW	5.6 mW/°C	448 mW	448 mW	—
U	700 mW	5.5 mW/°C	246 mW	330 mW	150 mW
W	700 mW	5.5 mW/°C	246 mW	330 mW	150 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V
Operating free-air temperature, T_A	0	70	–40	125	–40	125	–55	125	°C

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2252C			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $V_{DD} \pm \pm 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C		200	1500	μV
		Full range			1750	
αV_{IO} Temperature coefficient of input offset voltage		25°C to 70°C		0.5		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.003		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5	60	pA
		Full range			100	
I_{IB} Input bias current		25°C		1	60	pA
		Full range			100	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	–0.3 to 4.2		V
		Full range	0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C		4.9	4.94	
	Full range			4.8		
	$I_{OH} = -150\ \mu\text{A}$	25°C		4.8	4.88	
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C		0.01		V
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C		0.09	0.15	
		Full range			0.15	
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 1\text{ mA}$	25°C		0.2	0.3	
		Full range			0.3	
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C		0.7	1	
		Full range			1.2	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	350	V/mV
		Full range		10		
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C		1700	
r_{id} Differential input resistance		25°C		10^{12}		Ω
r_{ic} Common-mode input resistance		25°C		10^{12}		Ω
c_{ic} Common-mode input capacitance	$f = 10\text{ kHz}$, P package	25°C		8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C		200		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		dB
		Full range	70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		dB
		Full range	80			
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C		70	125	μA
		Full range			150	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2252C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1.5 V to 3.5 V, R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12	V/μs	
				Full range	0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36		nV/√Hz	
		f = 1 kHz		25°C	19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7		μV	
		f = 0.1 Hz to 10 Hz		25°C	1.1			
I _n	Equivalent input noise current			25°C	0.6		fA/√Hz	
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 10 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			
			A _V = 10		1%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡] ,	25°C	0.2		MHz	
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	30		kHz	
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] ,	C _L = 100 pF [‡]	25°C	63°			
Gain margin				25°C	15		dB	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise specified)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2252C			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, \quad V_O = 0, \quad R_S = 50 \, \Omega$	25°C		200	1500	μV
		Full range			1750	
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage		25°C to 70°C		0.5		$\mu V/^\circ C$
Input offset voltage long-term drift (see Note 4)		25°C		0.003		$\mu V/mo$
I_{IO} Input offset current		25°C		0.5	60	pA
		Full range			100	
I_{IB} Input bias current		25°C		1	60	pA
		Full range			100	
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5 \, mV, \quad R_S = 50 \, \Omega$	25°C	–5 to 4	–5.3 to 4.2		V
		Full range	–5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20 \, \mu A$	25°C		4.98		V
	$I_O = -100 \, \mu A$	25°C		4.9	4.93	
		Full range		4.7		
	$I_O = -200 \, \mu A$	25°C		4.8	4.86	
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, \quad I_O = 50 \, \mu A$	25°C		–4.99		V
	$V_{IC} = 0, \quad I_O = 500 \, \mu A$	25°C		–4.85	–4.91	
		Full range		–4.85		
	$V_{IC} = 0, \quad I_O = 1 \, mA$	25°C		–4.7	–4.8	
		Full range		–4.7		
	$V_{IC} = 0, \quad I_O = 4 \, mA$	25°C		–4	–4.3	
		Full range		–3.8		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4 \, V$	$R_L = 100 \, k\Omega$	25°C	45	650	V/mV
			Full range	10		
		$R_L = 1 \, M\Omega$	25°C		3000	
r_{id} Differential input resistance		25°C		10^{12}		Ω
r_{ic} Common-mode input resistance		25°C		10^{12}		Ω
c_{ic} Common-mode input capacitance	$f = 10 \, kHz, \quad P$ package	25°C		8		pF
z_o Closed-loop output impedance	$f = 25 \, kHz, \quad A_V = 10$	25°C		190		Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5 \, V$ to $2.7 \, V, \quad V_O = 0, \quad R_S = 50 \, \Omega$	25°C		75	88	dB
		Full range		75		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = 2.2 \, V$ to $\pm 8 \, V, \quad V_{IC} = 0, \quad$ No load	25°C		80	95	dB
		Full range		80		
I_{DD} Supply current	$V_O = 0, \quad$ No load	25°C		80	125	μA
		Full range			150	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2252C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±1.9 V, R _L = 100 kΩ, C _L = 100 pF		25°C	0.07	0.12	V/μs	
				Full range	0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38		nV/√Hz	
		f = 1 kHz		25°C	19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8		μV	
		f = 0.1 Hz to 10 Hz		25°C	1.1			
I _n	Equivalent input noise current			25°C	0.6		fA/√Hz	
THD + N	Total harmonic distortion pulse duration	V _O = ±2.3 V, f = 10 kHz, R _L = 50 kΩ	A _V = 1	25°C	0.2%			
			A _V = 10		1%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF	R _L = 50 kΩ,	25°C	0.21		MHz	
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 50 kΩ,	A _V = 1, C _L = 100 pF	25°C	14		kHz	
φ _m	Phase margin at unity gain	R _L = 50 kΩ,	C _L = 100 pF	25°C	63°			
Gain margin				25°C	15		dB	

[†] Full range is 0°C to 70°C.

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2254C			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C		200	1500	μV
		Full range			1750	
α_{VIO} Temperature coefficient of input offset voltage		25°C to 70°C		0.5		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.003		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5	60	pA
		Full range			100	
I_{IB} Input bias current		25°C		1	60	pA
		Full range			100	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega,$ $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		V
		Full range	0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C		4.9	4.94	
		Full range		4.8		
	$I_{OH} = -150\ \mu\text{A}$	25°C		4.8	4.88	V
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C		0.01		
	$V_{IC} = 2.5\text{ V}, I_{OL} = 500\ \mu\text{A}$	25°C		0.09	0.15	
		Full range			0.15	
	$V_{IC} = 2.5\text{ V}, I_{OL} = 1\text{ mA}$	25°C		0.2	0.3	
		Full range			0.3	
	$V_{IC} = 2.5\text{ V}, I_{OL} = 4\text{ mA}$	25°C		0.7	1	
		Full range			1.2	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	350	V/mV
			Full range	10		
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C		1700	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}		Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz},$ N package	25°C		8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz},$ $A_V = 10$	25°C		200		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C		70	83	dB
		Full range		70		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C		80	95	dB
		Full range		80		
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V},$ No load	25°C		140	250	μA
		Full range			300	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1.4 V to 2.6 V R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12	V/μs	
				Full range	0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36		nV/√Hz	
		f = 1 kHz		25°C	19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7		μV	
		f = 0.1 Hz to 10 Hz		25°C	1.1			
I _n	Equivalent input noise current			25°C	0.6		fA/√Hz	
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 10 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			
			A _V = 10		1%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡] ,	25°C	0.2		MHz	
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	30		kHz	
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] ,	C _L = 100 pF [‡]	25°C	63°			
	Gain margin			25°C	15		dB	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

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PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2254C			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50 \Omega$	25°C		200	1500	μV
		Full range			1750	
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage		25°C to 70°C		0.5		$\mu V/^\circ C$
Input offset voltage long-term drift (see Note 4)		25°C		0.003		$\mu V/mo$
I_{IO} Input offset current		25°C		0.5	60	pA
		Full range			100	
I_{IB} Input bias current		25°C		1	60	pA
		Full range			100	
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5$ mV, $R_S = 50 \Omega$	25°C	–5 to 4	–5.3 to 4.2		V
		Full range	–5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20 \mu A$	25°C		4.98		V
	$I_O = -100 \mu A$	25°C		4.9	4.93	
		Full range		4.7		
	$I_O = -200 \mu A$	25°C		4.8	4.86	
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50 \mu A$	25°C		–4.99		V
	$V_{IC} = 0, I_O = 500 \mu A$	25°C		–4.85	–4.91	
		Full range		–4.85		
	$V_{IC} = 0, I_O = 1$ mA	25°C		–4.7	–4.8	
		Full range		–4.7		
	$V_{IC} = 0, I_O = 4$ mA	25°C		–4	–4.3	
		Full range		–3.8		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4$ V	$R_L = 100$ k Ω	25°C	40	150	V/mV
			Full range	10		
		$R_L = 1$ M Ω	25°C		3000	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}		Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10$ kHz, N package	25°C		8		pF
z_o Closed-loop output impedance	$f = 25$ kHz, $A_V = 10$	25°C		190		Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0, R_S = 50 \Omega$	25°C		75	88	dB
		Full range		75		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2$ V to ± 8 V, $V_{IC} = 0$, No load	25°C		80	95	dB
		Full range		80		
I_{DD} Supply current (four amplifiers)	$V_O = 0$, No load	25°C		160	250	μA
		Full range			300	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±1.9 V, R _L = 100 kΩ, C _L = 100 pF		25°C	0.07	0.12		V/μs
				Full range	0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38			nV/√Hz
		f = 1 kHz		25°C	19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			
I _n	Equivalent input noise current			25°C	0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = ± 2.3 V, f = 20 kHz, R _L = 50 kΩ	A _V = 1	25°C	0.2%			
			A _V = 10		1%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF	R _L = 50 kΩ,	25°C	0.21			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 50 kΩ,	A _V = 1, C _L = 100 pF	25°C	14			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ,	C _L = 100 pF	25°C	63°			
Gain margin					25°C	15		

[†] Full range is 0°C to 70°C.

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD±} = ±2.5 V, V _O = 0, V _{IC} = 0, R _S = 50 Ω		25°C	200	1500		200	850	μV	
	Full range			1750			1000				
αV _{IO}	Temperature coefficient of input offset voltage			25°C to 85°C	0.5			0.5			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003			0.003			μV/mo
I _{IO}	Input offset current			25°C	0.5	60		0.5	60	pA	
				Full range	1000			1000			
I _{IB}	Input bias current			25°C	1	60		1	60	pA	
				Full range	1000			1000			
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2	V		
			Full range	0 to 3.5		0 to 3.5					
V _{OH}	High-level output voltage	I _{OH} = −20 μA	25°C	4.98			4.98			V	
		I _{OH} = −75 μA	25°C	4.9	4.94		4.9	4.94			
			Full range	4.8			4.8				
		I _{OH} = −150 μA	25°C	4.8	4.88		4.8	4.88			
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 50 μA	25°C	0.01			0.01			V	
		V _{IC} = 2.5 V, I _{OL} = 500 μA	25°C	0.09	0.15		0.09	0.15			
			Full range	0.15			0.15				
		V _{IC} = 2.5 V, I _{OL} = 4 mA	25°C	0.8	1		0.7	1			
			Full range	1.2			1.2				
		A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V		R _L = 100 kΩ‡			R _L = 100 kΩ‡		
25°C	100				350		100	350			
Full range	10				10						
			25°C	R _L = 1 MΩ‡			R _L = 1 MΩ‡				
			25°C	1700			1700				
r _{id}	Differential input resistance			25°C	10 ¹²			10 ¹²			Ω
r _{ic}	Common-mode input resistance			25°C	10 ¹²			10 ¹²			Ω
c _{ic}	Common-mode input capacitance	f = 10 kHz,	P package	25°C	8			8			pF
z _o	Closed-loop output impedance	f = 25 kHz,	A _V = 10	25°C	200			200			Ω
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V, V _O = 2.5 V, R _S = 50 Ω		25°C	70	83		70	83	dB	
				Full range	70			70			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 4.4 V to 16 V, V _{IC} = V _{DD} /2, No load		25°C	80	95		80	95	dB	
				Full range	80			80			
I _{DD}	Supply current	V _O = 2.5 V, No load		25°C	70	125		70	125	μA	
				Full range	150			150			

† Full range is –40°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A †	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1.5 V to 3.5 V, R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36			36			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7			0.7			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 10 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
	Gain-bandwidth product	f = 50 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡] ,	25°C	0.2			0.2			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡] ,	A _V = 1, R _L = 50 kΩ [‡] ,	25°C	30			30			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] , C _L = 100 pF [‡]		25°C	63°			63°			
	Gain margin			25°C	15			15			dB

† Full range is –40°C to 125°C.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0, V _O = 0, R _S = 50 Ω		25°C	200	1500	200	850	μV		
	Full range			1750			1000				
α _{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C	0.5			0.5		μV/°C	
	Input offset voltage long-term drift (see Note 4)			25°C	0.003			0.003		μV/mo	
I _{IO}	Input offset current			25°C	0.5	60	0.5	60	pA		
				Full range	1000			1000			
I _{IB}	Input bias current			25°C	1	60	1	60	pA		
				Full range	1000			1000			
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤ 5 mV		25°C	–5 to 4	–5.3 to 4.2	–5 to 4	–5.3 to 4.2	V		
				Full range	–5 to 3.5		–5 to 3.5				
V _{OM+}	Maximum positive peak output voltage	I _O = –20 μA		25°C	4.98		4.98		V		
		I _O = –100 μA		25°C	4.9	4.93	4.9	4.93			
				Full range	4.7		4.7				
		I _O = –200 μA		25°C	4.8	4.86	4.8	4.86			
V _{OM–}	Maximum negative peak output voltage	V _{IC} = 0, I _O = 50 μA		25°C	–4.99		–4.99		V		
		V _{IC} = 0, I _O = 500 μA		25°C	–4.85	–4.91	–4.85	–4.91			
				Full range	–4.85		–4.85				
		V _{IC} = 0, I _O = 4 mA		25°C	–4	–4.3	–4	–4.3			
				Full range	–3.8		–3.8				
		A _{VD}	Large-signal differential voltage amplification	V _O = ±4 V	R _L = 50 kΩ	25°C	40	150			40
	Full range				10		10				
R _L = 1 MΩ	25°C				3000		3000				
r _{id}	Differential input resistance			25°C	10 ¹²		10 ¹²		Ω		
r _{ic}	Common-mode input resistance			25°C	10 ¹²		10 ¹²		Ω		
c _{ic}	Common-mode input capacitance	f = 10 kHz,	P package	25°C	8		8		pF		
z _o	Closed-loop output impedance	f = 25 kHz,	A _V = 10	25°C	190		190		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = –5 V to 2.7 V, V _O = 0, R _S = 50 Ω		25°C	75	88	75	88	dB		
				Full range	75		75				
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD±} /ΔV _{IO})	V _{DD} = 4.4 V to 16 V, V _{IC} = V _{DD} /2, No load		25°C	80	95	80	95	dB		
				Full range	80		80				
I _{DD}	Supply current	V _O = 2.5 V, No load		25°C	80	125	80	125	μA		
				Full range	150		150				

† Full range is -40°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A †	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±1.9 V, R _L = 100 kΩ, C _L = 100 pF		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38			38			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8			0.8			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA√Hz
THD + N	Total harmonic distortion plus noise	V _O = ±2.3 V, R _L = 50 kΩ, f = 10 kHz	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
Gain-bandwidth product		f=10 kHz, R _L = 50 kΩ, C _L = 100 pF		25°C	0.21			0.21			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, A _V = 1, R _L = 50 kΩ, C _L = 100 pF		25°C	14			14			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ, C _L = 100 pF		25°C	63°			63°			
Gain margin				25°C	15			15			dB

† Full range is -40°C to 125°C .

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PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254I			TLC2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD} ± = ±2.5 V, V _{IC} = 0, V _O = 0, R _S = 50 Ω		25°C	200		1500	200		850	μV
	Full range					1750	1000				
α _{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C	0.5				0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003				0.003		μV/mo
I _{IO}	Input offset current			25°C	0.5		60	0.5		60	pA
				Full range			1000	1000			
I _{IB}	Input bias current			25°C	1		60	1		60	pA
				Full range			1000	1000			
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤5 mV	25°C	0 to 4	−0.3 to 4.2			0 to 4	−0.3 to 4.2	V	
			Full range	0 to 3.5				0 to 3.5			
V _{OH}	High-level output voltage	I _{OH} = −20 μA		25°C	4.98				4.98	V	
		I _{OH} = −75 μA		25°C	4.9	4.94	4.9		4.94		
				Full range	4.8		4.8				
		I _{OH} = −150 μA		25°C	4.8	4.88	4.8		4.88		
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 50 μA	25°C	0.01				0.01		V	
		V _{IC} = 2.5 V, I _{OL} = 500 μA	25°C	0.09		0.15	0.09		0.15		
			Full range	0.15		0.15					
		V _{IC} = 2.5 V, I _{OL} = 4 mA	25°C	0.8		1	0.7		1		
			Full range	1.2		1.2					
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 100 kΩ [‡]	25°C	100	350	100		350	V/mV	
				Full range	10		10				
			R _L = 1 MΩ [‡]	25°C	1700		1700				
r _{i(d)}	Differential input resistance			25°C	10 ¹²		10 ¹²		Ω		
r _{i(c)}	Common-mode input resistance			25°C	10 ¹²		10 ¹²		Ω		
c _{i(c)}	Common-mode input capacitance	f = 10 kHz, N package	25°C	8		8		pF			
z _o	Closed-loop output impedance	f = 25 kHz, A _V = 10	25°C	200		200		Ω			
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V, V _O = 2.5 V, R _S = 50 Ω	25°C	70	83	70		83	dB		
			Full range	70		70					
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 4.4 V to 16 V, V _{IC} = V _{DD} /2, No load	25°C	80	95	80		95	dB		
			Full range	80		80					
I _{DD}	Supply current (four amplifiers)	V _O = 2.5 V, No load	25°C	140	250	140		250	μA		
			Full range	300		300					

† Full range is -40°C to 125°C .

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T_A †	TLC2254I			TLC2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.4\text{ V to }2.6\text{ V}$, $R_L = 100\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$		25°C	0.07	0.12		0.07	0.12		V/ μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C		36			36		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C		0.7			0.7		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$	25°C		0.2%			0.2%		
			$A_V = 10$			1%			1%		
	Gain-bandwidth product	$f = 50\text{ kHz}$, $C_L = 100\text{ pF}^\ddagger$	$R_L = 50\text{ k}\Omega^\ddagger$	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$, $C_L = 100\text{ pF}^\ddagger$	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger$	$C_L = 100\text{ pF}^\ddagger$	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is –40°C to 125°C.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254I			TLC2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0, V _O = 0, R _S = 50 Ω		25°C	200		1500	200		850	μV
	Full range			1750		1000					
α _{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C	0.5		0.5		μV/°C		
	Input offset voltage long-term drift (see Note 4)			25°C	0.003		0.003		μV/mo		
I _{IO}	Input offset current			25°C	0.5		60	0.5		60	pA
				Full range	1000		1000				
I _{IB}	Input bias current			25°C	1		60	1		60	pA
				Full range	1000		1000				
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤ 5 mV		25°C	–5 to 4	–5.3 to 4.2	–5 to 4	–5.3 to 4.2	V		
				Full range	–5 to 3.5		–5 to 3.5				
V _{OM+}	Maximum positive peak output voltage	I _O = –20 μA		25°C	4.98		4.98		V		
		I _O = –100 μA		25°C	4.9	4.93	4.9	4.93			
				Full range	4.7		4.7				
		I _O = –200 μA		25°C	4.8	4.86	4.8	4.86			
V _{OM–}	Maximum negative peak output voltage	V _{IC} = 0, I _O = 50 μA		25°C	–4.99		–4.99		V		
		V _{IC} = 0, I _O = 500 μA		25°C	–4.85	–4.91	–4.85	–4.91			
				Full range	–4.85		–4.85				
		V _{IC} = 0, I _O = 4 mA		25°C	–4	–4.3	–4	–4.3			
				Full range	–3.8		–3.8				
		A _{VD}	Large-signal differential voltage amplification	V _O = ±4 V	R _L = 100 kΩ	25°C	40	150			40
R _L = 1 MΩ	Full range				10		10				
	25°C				3000		3000				
r _{i(d)}	Differential input resistance			25°C	10 ¹²		10 ¹²		Ω		
r _{i(c)}	Common-mode input resistance			25°C	10 ¹²		10 ¹²		Ω		
c _{i(c)}	Common-mode input capacitance	f = 10 kHz,	N package	25°C	8		8		pF		
z _o	Closed-loop output impedance	f = 25 kHz,	A _V = 10	25°C	190		190		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = –5 V to 2.7 V, V _O = 0, R _S = 50 Ω		25°C	75	88	75	88	dB		
				Full range	75		75				
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD±} /ΔV _{IO})	V _{DD±} = ±2.2 V to ±8 V, V _{IC} = V _{DD} /2, No load		25°C	80	95	80	95	dB		
				Full range	80		80				
I _{DD}	Supply current (four amplifiers)	V _O = 0, No load		25°C	160	250	160	250	μA		
				Full range	300		300				

† Full range is -40°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254I			TLC2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±1.9 V, R _L = 100 kΩ, C _L = 100 pF		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38			38			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8			0.8			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = ±2.3 V, R _L = 50 kΩ, f = 20 kHz	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF	R _L = 50 kΩ,	25°C	0.21			0.21			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 50 kΩ,	A _V = 1, C _L = 100 pF	25°C	14			14			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ, C _L = 100 pF		25°C	63°			63°			
Gain margin				25°C	15			15			dB

† Full range is -40°C to 125°C .

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2252Q TLC2252M			TLC2252AQ TLC2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	200	1500		200	850		μV
		Full range		1750			1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		Full range		1000			1000		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		Full range		1000			1000		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.98			4.98			V
	$I_{OH} = -75\ \mu\text{A}$	25°C	4.9	4.94		4.9	4.94		
		Full range	4.8			4.8			
	$I_{OH} = -150\ \mu\text{A}$	25°C	4.8	4.88		4.8	4.88		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	0.01			0.01			V
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15		0.09	0.15		
		Full range		0.15			0.15		
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C	0.8	1		0.7	1		
		Full range		1.2			1.2		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	350	100	350		V/mV
			Full range	10		10			
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C	1700		1700			
r_{id} Differential input resistance		25°C	10^{12}			10^{12}			Ω
r_{ic} Common-mode input resistance		25°C	10^{12}			10^{12}			Ω
c_{ic} Common-mode input capacitance	$f = 10\text{ kHz}$, $f = 10\text{ kHz}$	25°C	8			8			pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C	200			200			Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		70	83		dB
		Full range	70			70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C	70	125		70	125		μA
		Full range		150			150		

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2252Q TLC2252M			TLC2252AQ TLC2252AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 0.5 V to 3.5 V, R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36			36			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7			0.7			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 10 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
	Gain-bandwidth product	f = 50 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡] ,	25°C	0.2			0.2			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	30			30			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] , C _L = 100 pF [‡]		25°C	63°			63°			
	Gain margin			25°C	15			15			dB

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2252Q TLC2252M			TLC2252AQ TLC2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C	200	1500		200	850		μV
		Full range		1750			1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		Full range		1000			1000		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		Full range		1000			1000		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	–5 to 4	–5.3 to 4.2		–5 to 4	–5.3 to 4.2		V
		Full range	–5 to 3.5			–5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C	4.98			4.98			V
	$I_O = -100\ \mu\text{A}$	25°C	4.9	4.93		4.9	4.93		
		Full range	4.7			4.7			
	$I_O = -200\ \mu\text{A}$	25°C	4.8	4.86		4.8	4.86		
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50\ \mu\text{A}$	25°C	–4.99			–4.99			V
	$V_{IC} = 0, I_O = 500\ \mu\text{A}$	25°C	–4.85	–4.91		–4.85	–4.91		
		Full range	–4.85			–4.85			
	$V_{IC} = 0, I_O = 4\text{ mA}$	25°C	–4	–4.3		–4	–4.3		
		Full range	–3.8			–3.8			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$	$R_L = 100\text{ k}\Omega$	25°C	40	150	40	150		V/mV
			Full range	10		10			
		$R_L = 1\text{ M}\Omega$	25°C	3000		3000			
r_{id} Differential input resistance		25°C	10^{12}			10^{12}			Ω
r_{ic} Common-mode input resistance		25°C	10^{12}			10^{12}			Ω
C_{ic} Common-mode input capacitance	$f = 10\text{ kHz}, \text{ P package}$	25°C	8			8			pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}, A_V = 10$	25°C	190			190			Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5\text{ V to } 2.7\text{ V}, V_O = 0, R_S = 50\ \Omega$	25°C	75	88		75	88		dB
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = \pm 2.2\text{ V to } \pm 8\text{ V}, V_{IC} = 0, \text{ No load}$	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}, \text{ No load}$	25°C	80	125		80	125		μA
		Full range		150			150		

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2252Q TLC2252M			TLC2252AQ TLC2252AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±2 V, R _L = 100 kΩ, C _L = 100 pF		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38			38			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8			0.8			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA√Hz
THD + N	Total harmonic distortion plus noise	V _O = ±2.3 V, R _L = 50 kΩ, f = 10 kHz	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
Gain-bandwidth product		f = 10 kHz, R _L = 50 kΩ, C _L = 100 pF		25°C	0.21			0.21			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, A _V = 1, R _L = 50 kΩ, C _L = 100 pF		25°C	14			14			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ, C _L = 100 pF		25°C	63°			63°			
Gain margin				25°C	15			15			dB

[†] Full range is – 40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254Q TLC2254M			TLC2254AQ TLC2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD±} = ±2.5 V, V _{IC} = 0, V _O = 0, R _S = 50 Ω		25°C	200	1500		200	850	μV	
	Full range			1750			1000				
αV _{IO}	Temperature coefficient of input offset voltage			25°C to 125°C	0.5				0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003				0.003		μV/mo
I _{IO}	Input offset current			25°C	0.5	60		0.5	60	pA	
				125°C	1000				1000		
I _{IB}	Input bias current			25°C	1	60		1	60	pA	
				125°C	1000				1000		
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2	V		
			Full range	0 to 3.5		0 to 3.5					
V _{OH}	High-level output voltage	I _{OH} = −20 μA	25°C	4.98			4.98		V		
		I _{OH} = −75 μA	25°C	4.9	4.94		4.9	4.94			
			Full range	4.8			4.8				
		I _{OH} = −150 μA	25°C	4.8	4.88		4.8	4.88			
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 50 μA	25°C	0.01			0.01		V		
		V _{IC} = 2.5 V, I _{OL} = 500 μA	25°C	0.09	0.15		0.09	0.15			
			Full range	0.15			0.15				
		V _{IC} = 2.5 V, I _{OL} = 4 mA	25°C	0.8	1		0.7	1			
			Full range	1.2			1.2				
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 100 kΩ [‡]	25°C	100	350		100	350	V/mV	
				Full range	10		10				
			R _L = 1 MΩ [‡]	25°C	1700			1700			
r _{i(d)}	Differential input resistance			25°C	10 ¹²			10 ¹²	Ω		
r _{i(c)}	Common-mode input resistance			25°C	10 ¹²			10 ¹²	Ω		
c _{i(c)}	Common-mode input capacitance	f = 10 kHz, N package	25°C	8			8		pF		
z _o	Closed-loop output impedance	f = 25 kHz, A _V = 10	25°C	200			200		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V, V _O = 2.5 V, R _S = 50 Ω	25°C	70	83		70	83	dB		
			Full range	70		70					
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 4.4 V to 16 V, V _{IC} = V _{DD} /2, No load	25°C	80	95		80	95	dB		
			Full range	80		80					
I _{DD}	Supply current (four amplifiers)	V _O = 2.5 V, No load	25°C	140	250		140	250	μA		
			Full range	300			300				

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	TLC2254Q TLC2254M			TLC2254AQ TLC2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 0.5\text{ V to }3.5\text{ V}$, $R_L = 100\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$		25°C	0.07	0.12		0.07	0.12		V/ μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C		36			36		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C		0.7			0.7		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$	25°C		0.2%			0.2%		
			$A_V = 10$			1%			1%		
	Gain-bandwidth product	$f = 50\text{ kHz}$, $C_L = 100\text{ pF}^\ddagger$	$R_L = 50\text{ k}\Omega^\ddagger$	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$, $C_L = 100\text{ pF}^\ddagger$	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger$	$C_L = 100\text{ pF}^\ddagger$	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2254Q TLC2254M			TLC2254AQ TLC2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50 \Omega$	25°C	200	1500		200	850		μV
		Full range		1750			1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu V/^\circ C$
Input offset voltage long-term drift (See Note 4)		25°C	0.003			0.003			$\mu V/mo$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		125°C		1000			1000		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		125°C		1000			1000		
V_{ICR} Common-mode input voltage range	$R_S = 50 \Omega, V_{IO} \leq 5$ mV	25°C	–5 to 4	–5.3 to 4.2		–5 to 4	–5.3 to 4.2		V
		Full range	–5 to 3.5			–5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20 \mu A$	25°C	4.98			4.98			V
	$I_O = -100 \mu A$	25°C	4.9	4.93		4.9	4.93		
		Full range	4.7			4.7			
	$I_O = -200 \mu A$	25°C	4.8	4.86		4.8	4.86		
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50 \mu A$	25°C	–4.99			–4.99			V
	$V_{IC} = 0, I_O = 500 \mu A$	25°C	–4.85	–4.91		–4.85	–4.91		
		Full range	–4.85			–4.85			
	$V_{IC} = 0, I_O = 4$ mA	25°C	–4	–4.3		–4	–4.3		
		Full range	–3.8			–3.8			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4$ V	$R_L = 100$ k Ω	25°C	40	150	40	150		V/mV
			Full range	10		10			
		$R_L = 1$ M Ω	25°C	3000		3000			
$r_{i(d)}$ Differential input resistance		25°C	10 ¹²			10 ¹²			Ω
$r_{i(c)}$ Common-mode input resistance		25°C	10 ¹²			10 ¹²			Ω
$c_{i(c)}$ Common-mode input capacitance	$f = 10$ kHz, N package	25°C	8			8			pF
z_o Closed-loop output impedance	$f = 25$ kHz, $A_V = 10$	25°C	190			190			Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0, R_S = 50 \Omega$	25°C	75	88		75	88		dB
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2$ V to ± 8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current (four amplifiers)	$V_O = 0$, No load	25°C	160	250		160	250		μA
		Full range		300			300		

† Full range is –40°C to 125°C for Q suffix, –55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254Q TLC2254M			TLC2254AQ TLC2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±2 V, C _L = 100 pF	R _L = 100 kΩ,	25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38			38			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8			0.8			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = ±2.3 V, R _L = 50 kΩ, f = 20 kHz	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF	R _L = 50 kΩ,	25°C	0.21			0.21			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 50 kΩ,	A _V = 1, C _L = 100 pF	25°C	14			14			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ,	C _L = 100 pF	25°C	63°			63°			
Gain margin				25°C	15			15			dB

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

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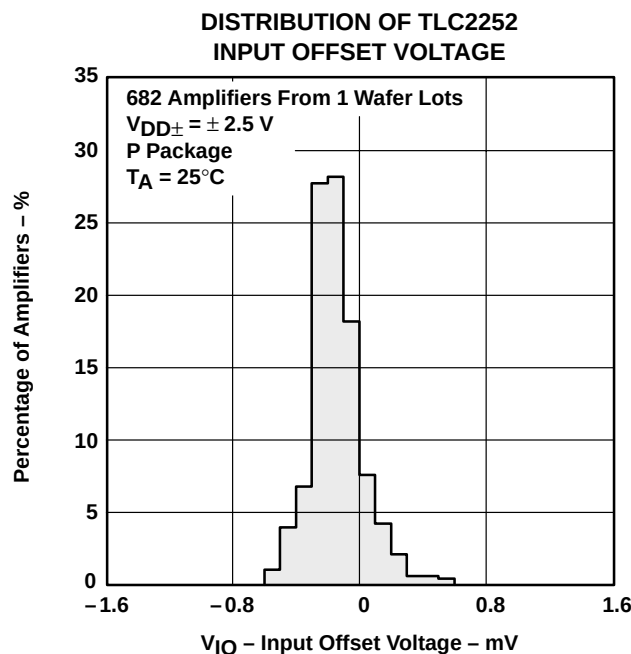


Figure 2

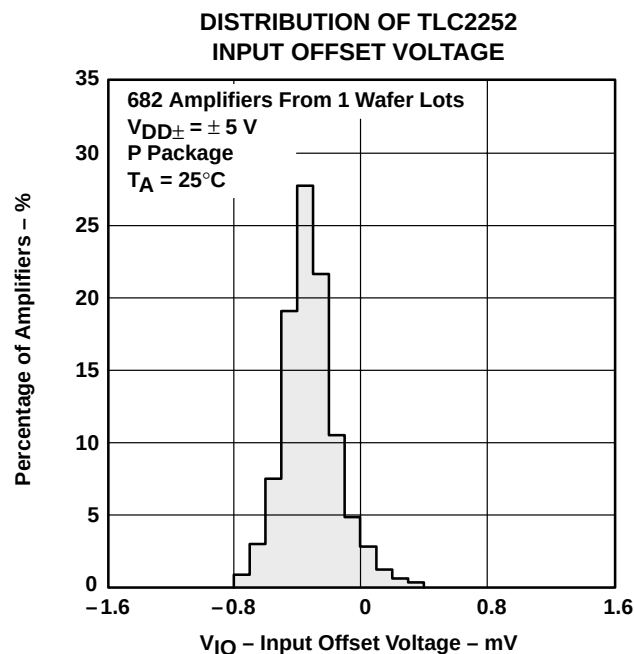


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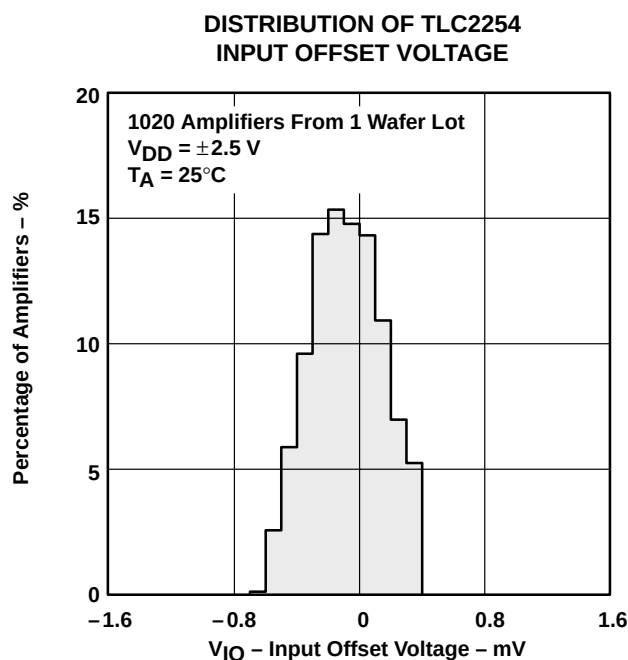


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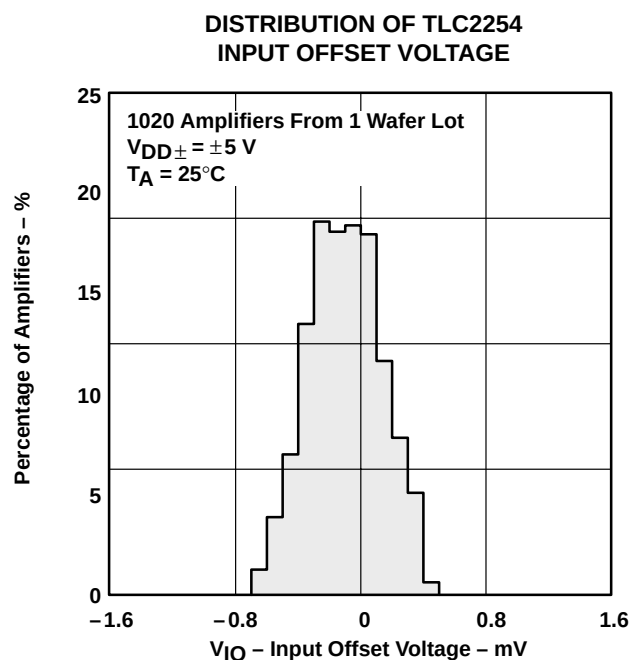


Figure 5

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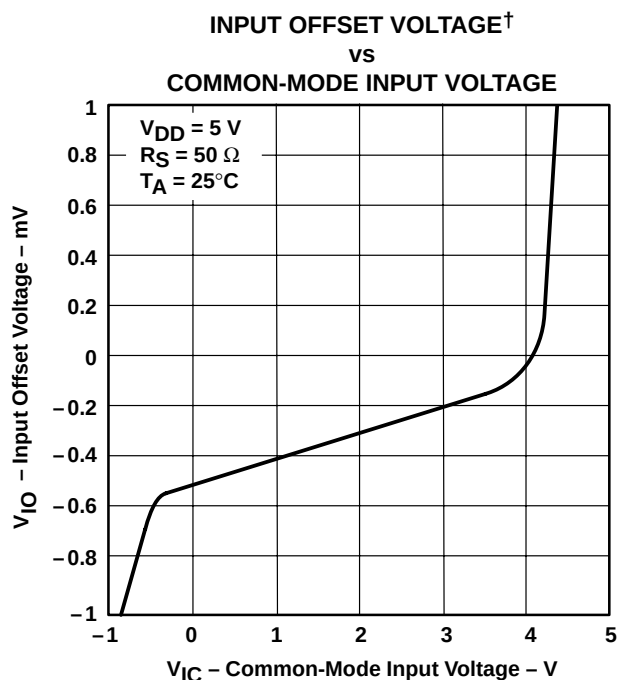


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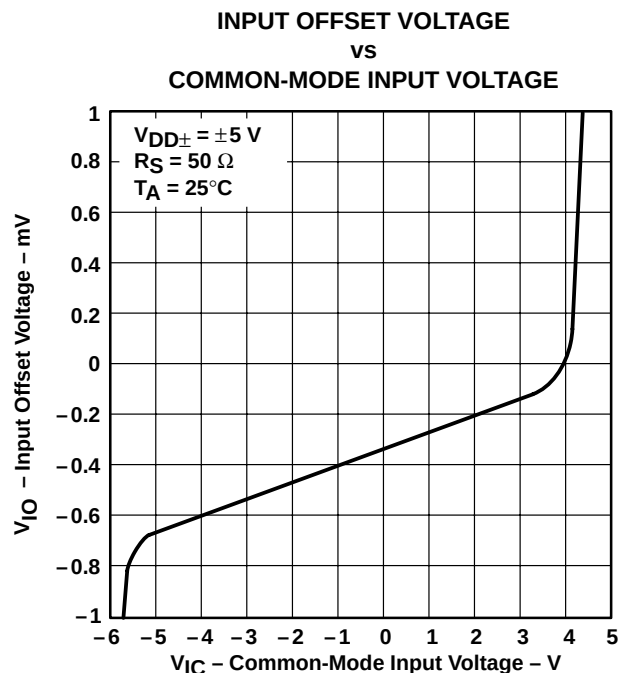


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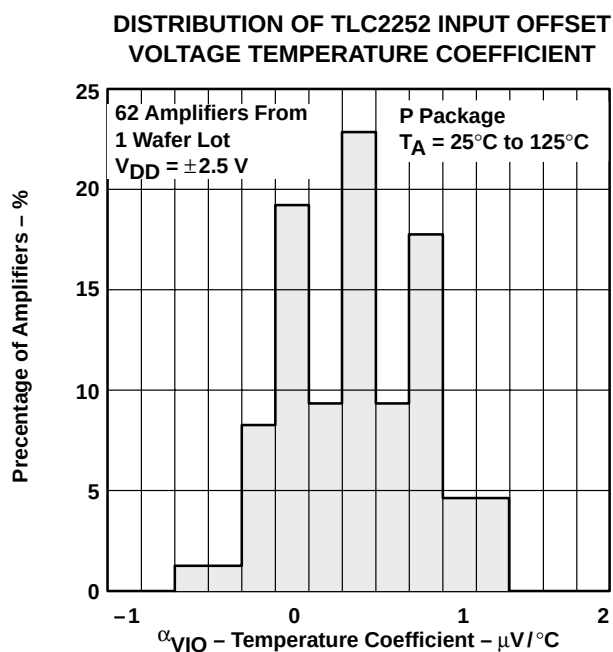


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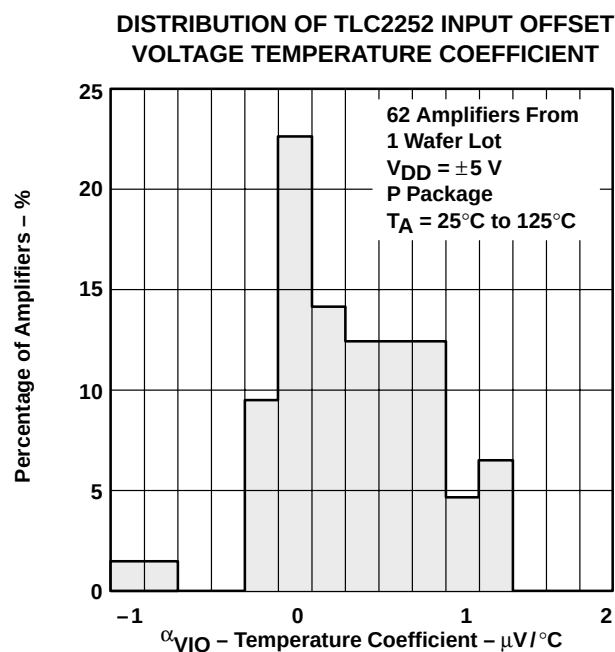


Figure 9

[†] For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V .

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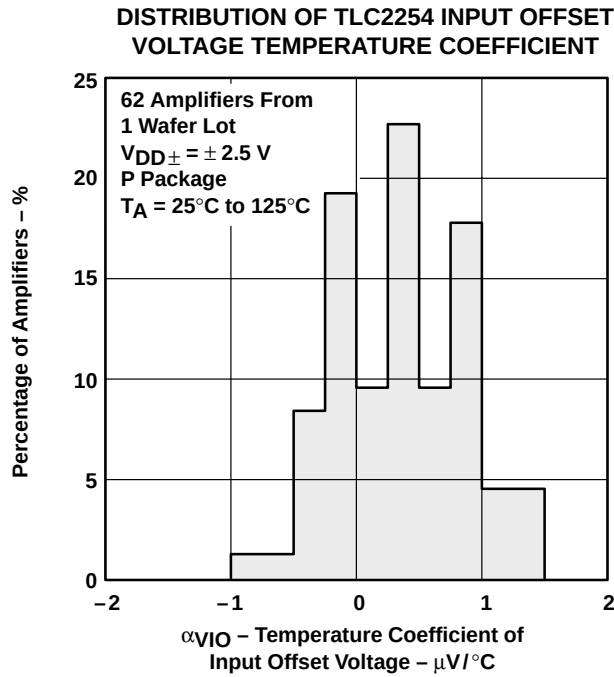


Figure 10

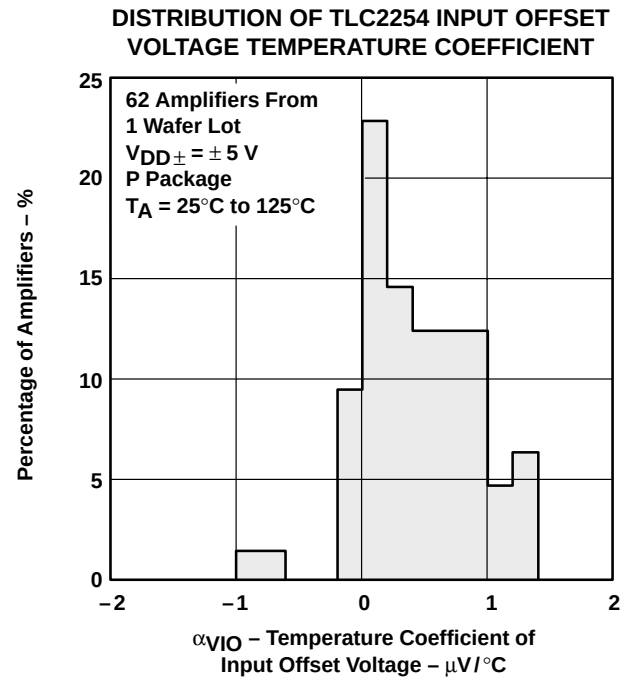


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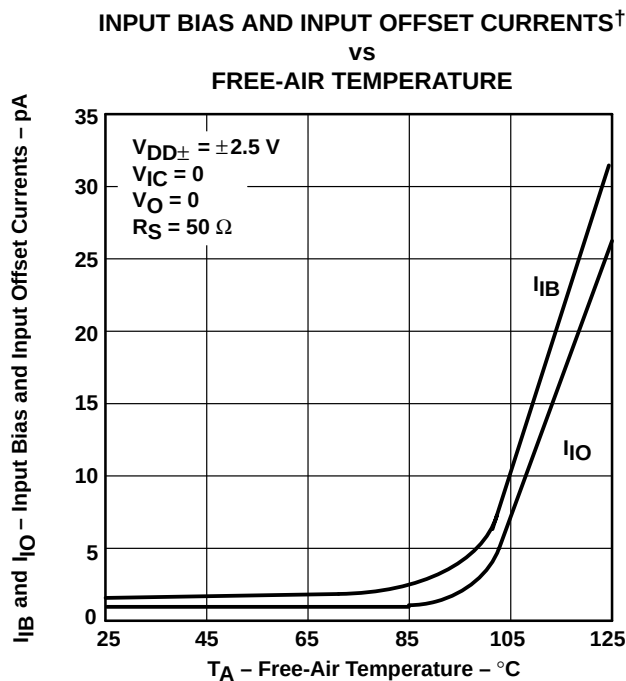


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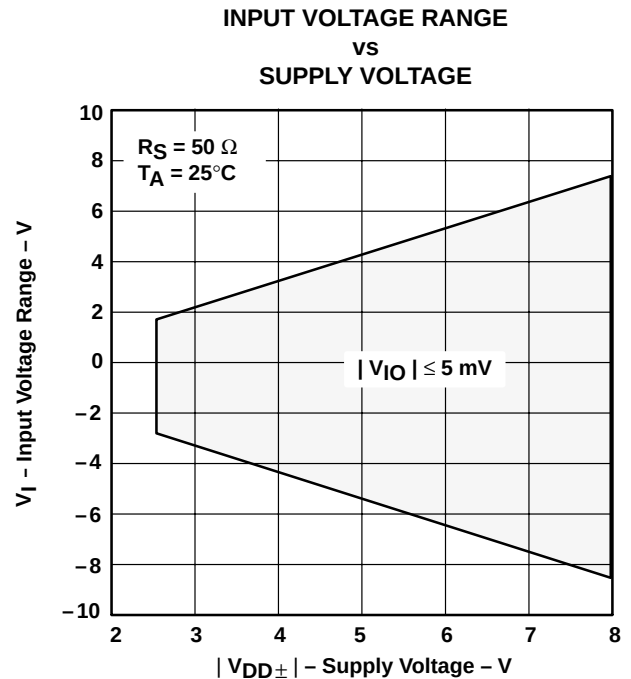


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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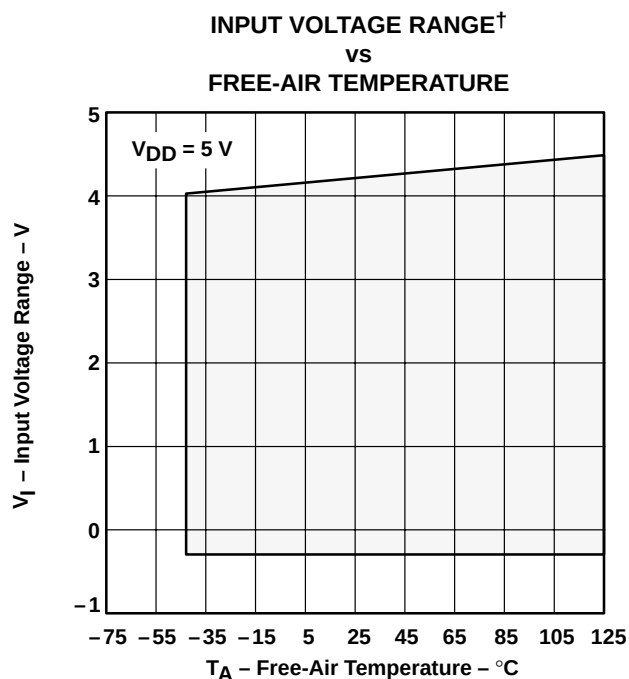


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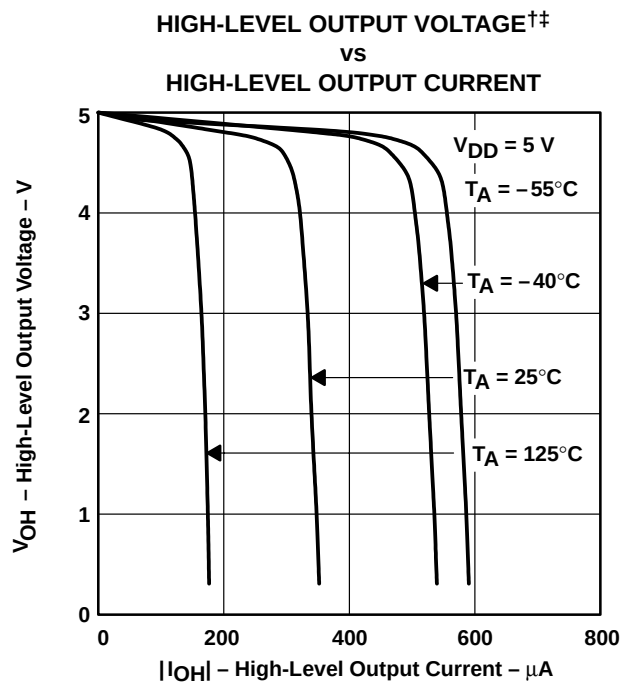


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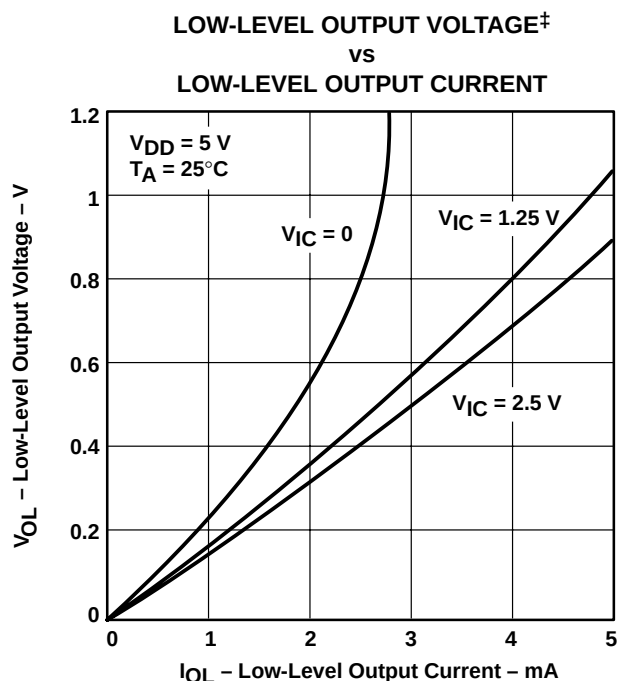


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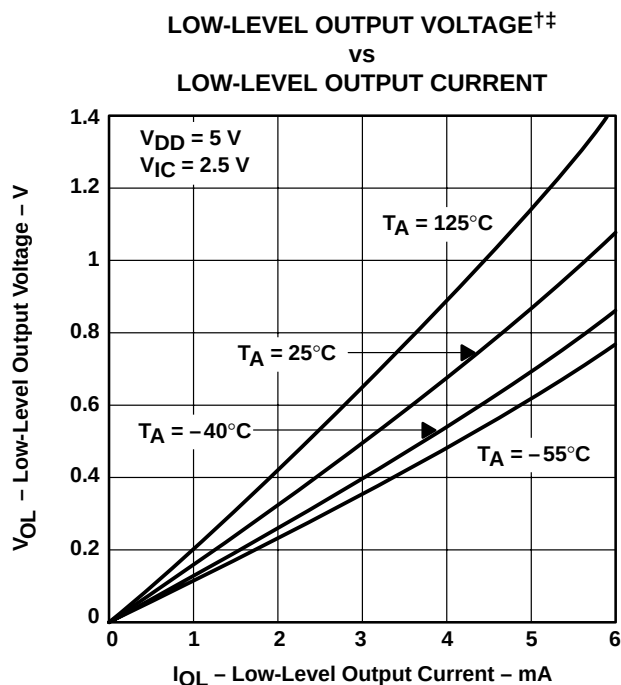
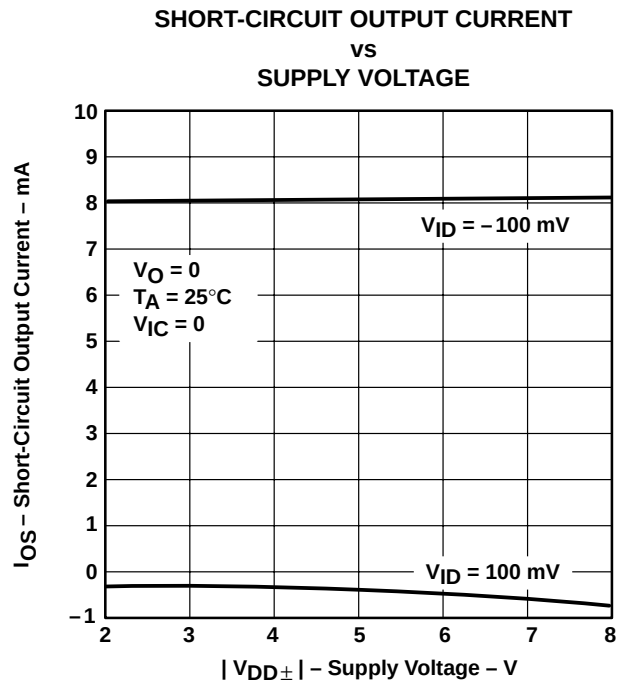
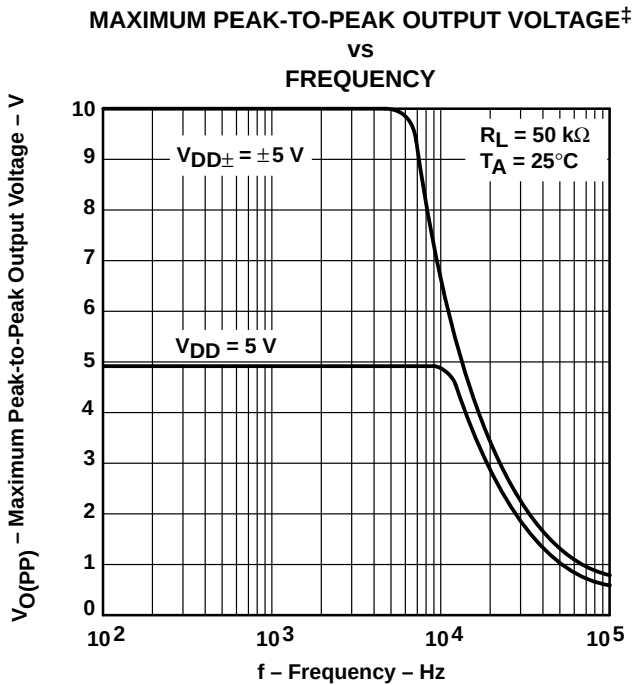
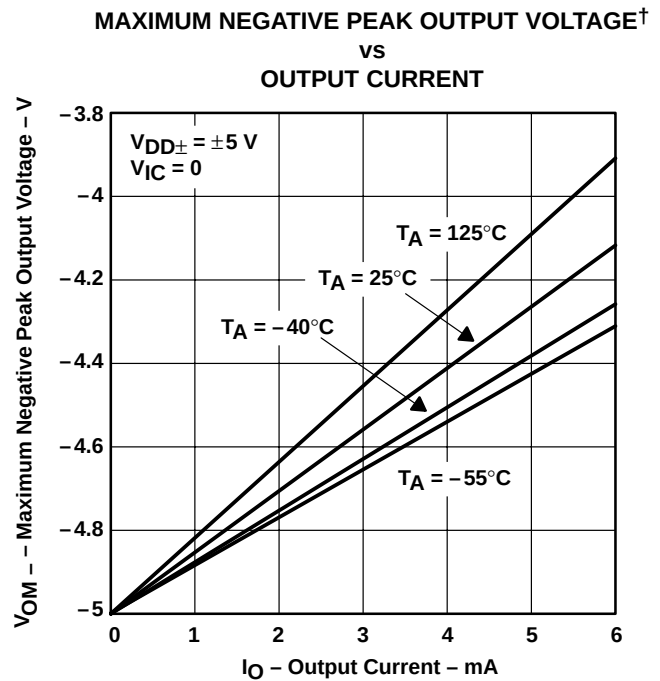
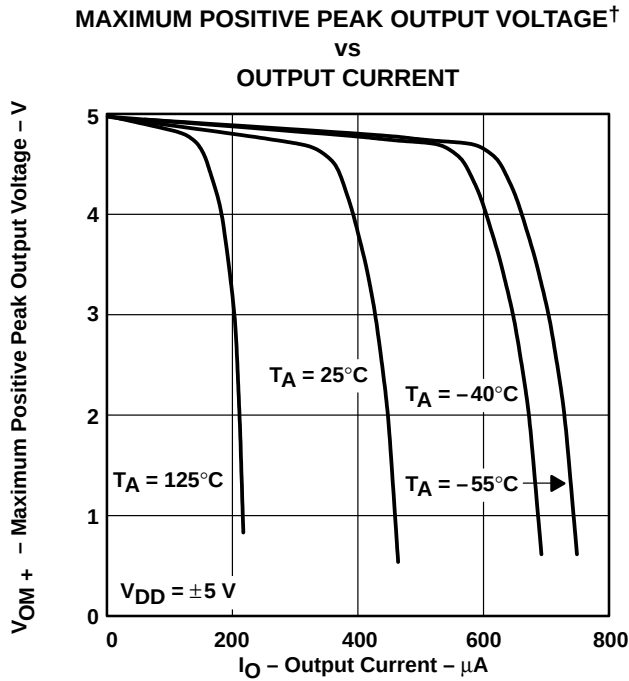


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V .

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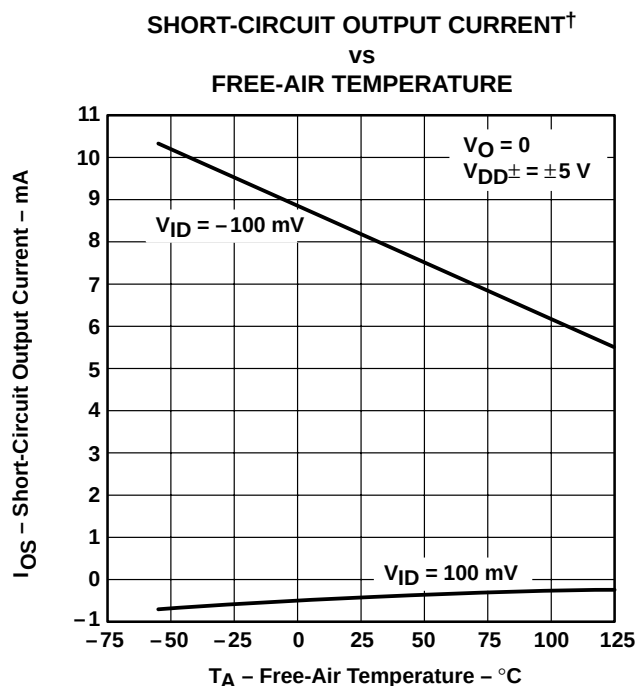


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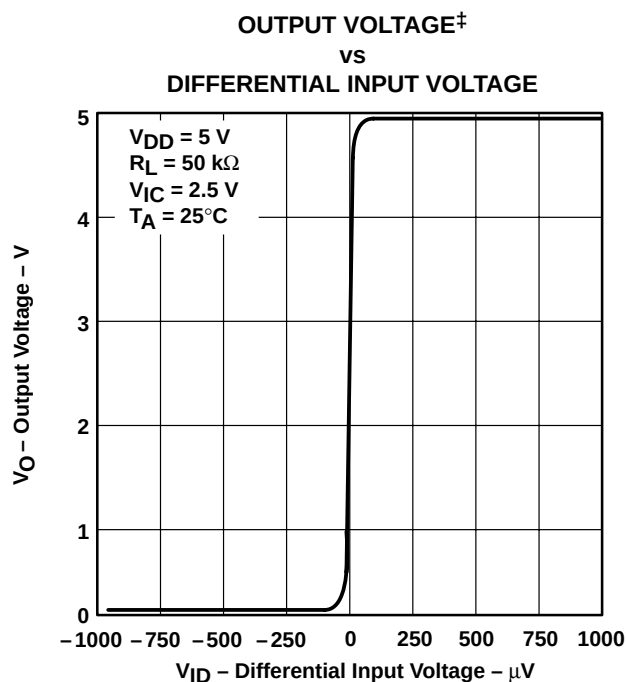


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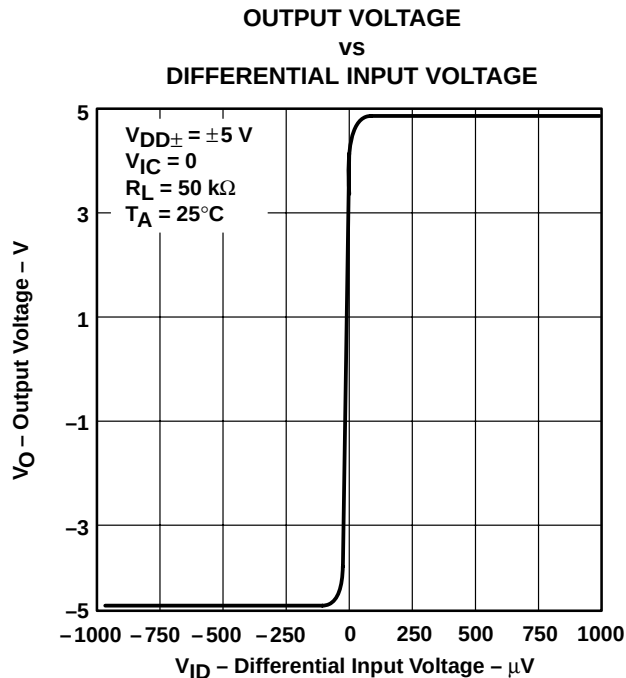


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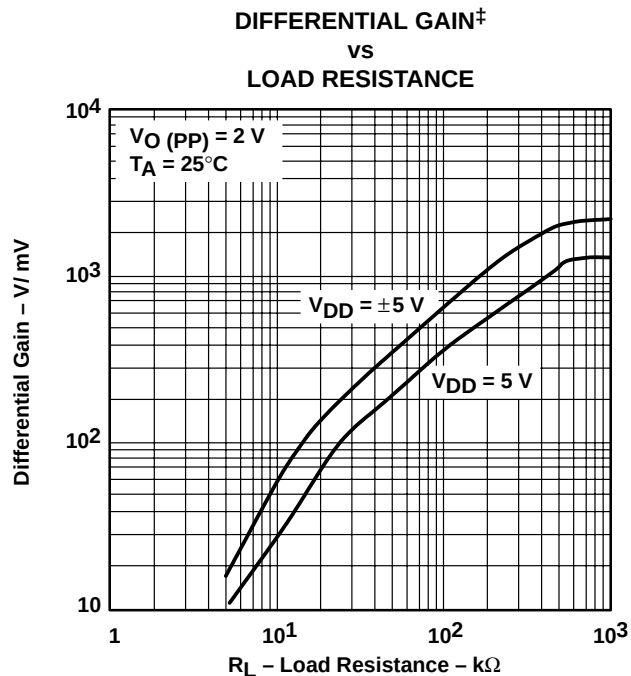


Figure 25

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V.

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LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN†

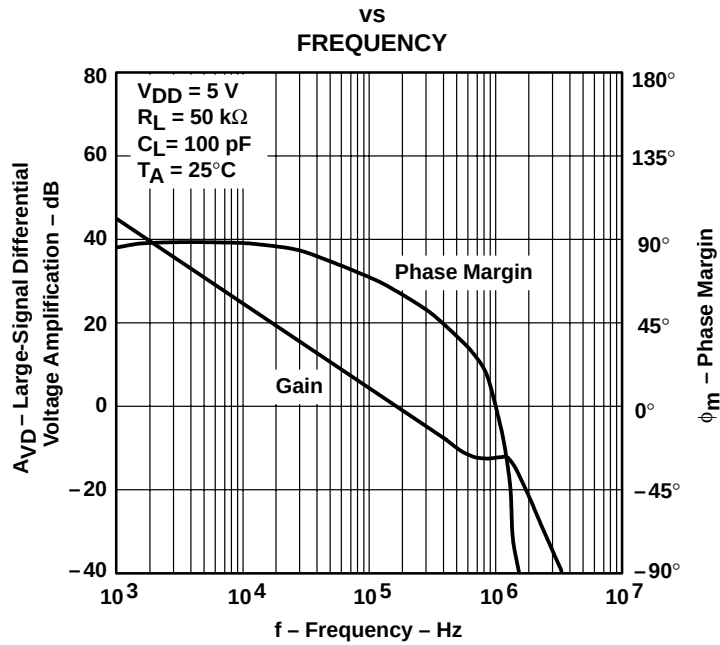


Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN

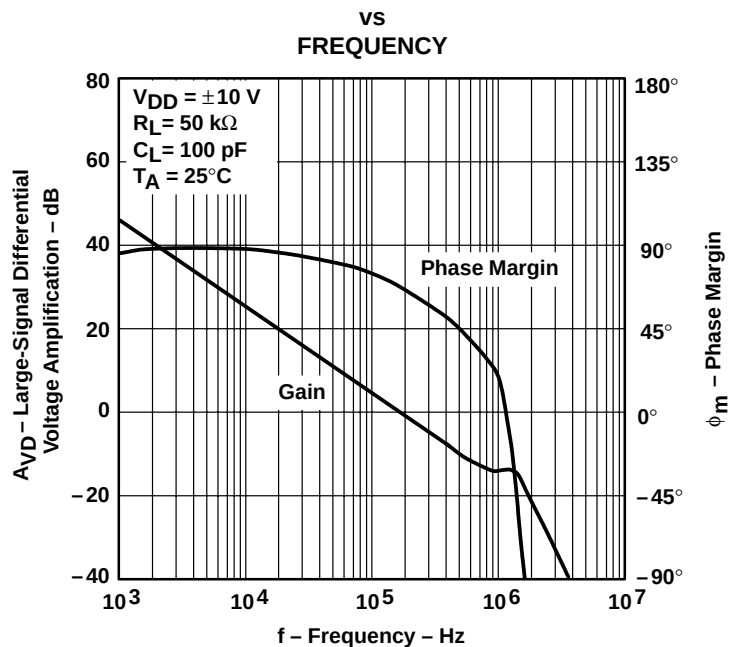


Figure 27

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

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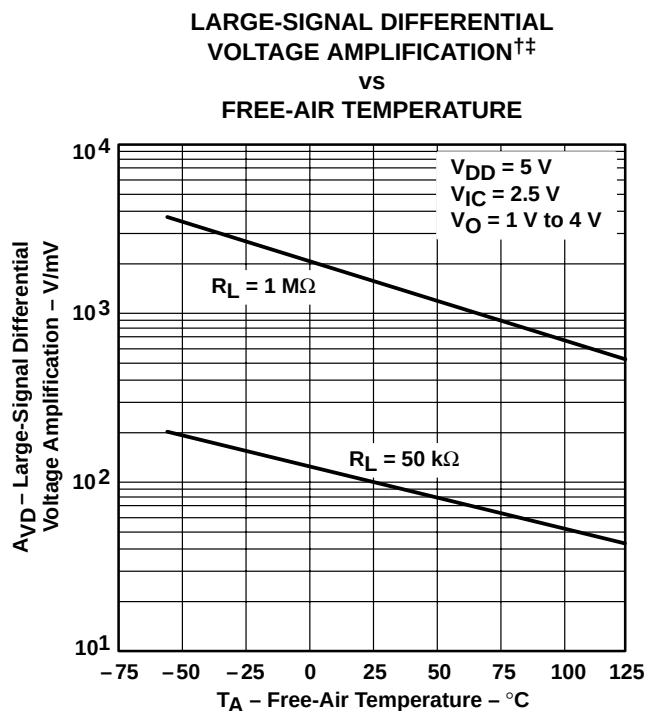


Figure 28

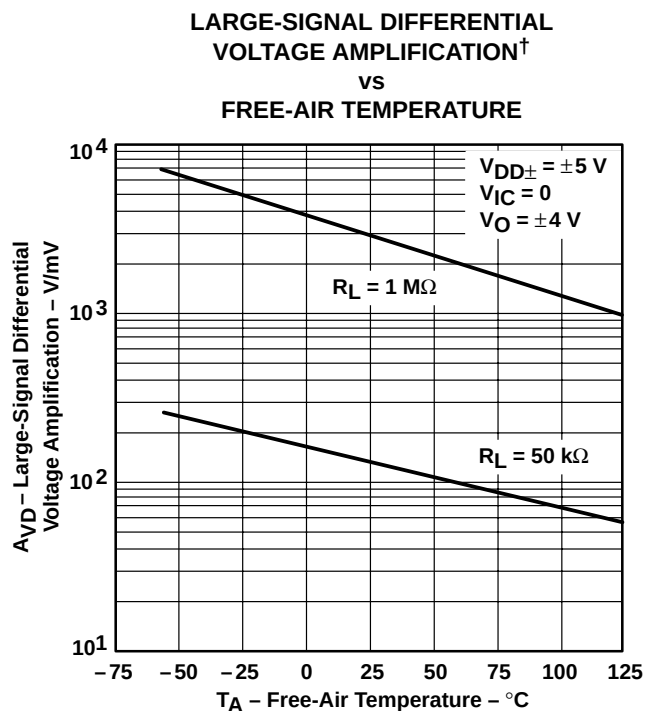


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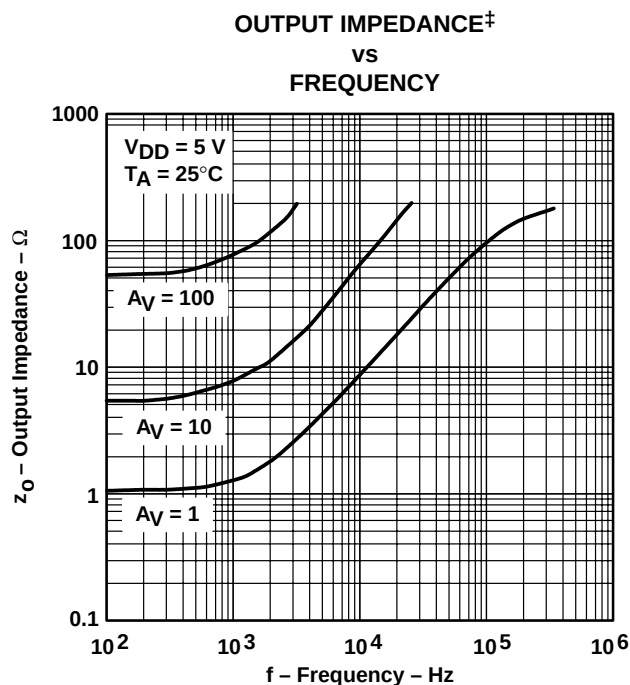


Figure 30

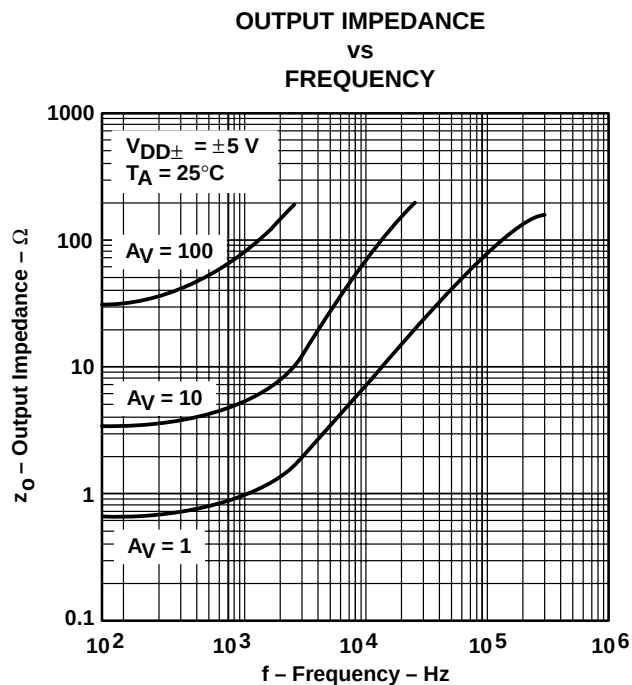
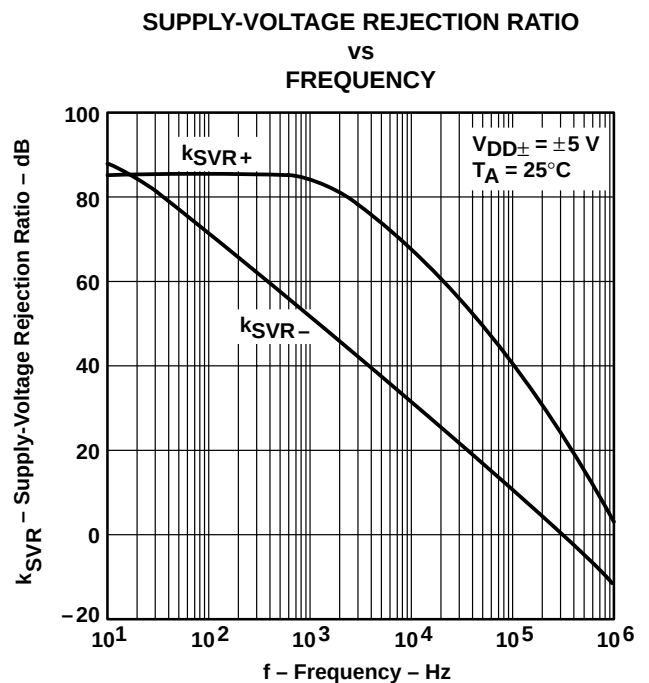
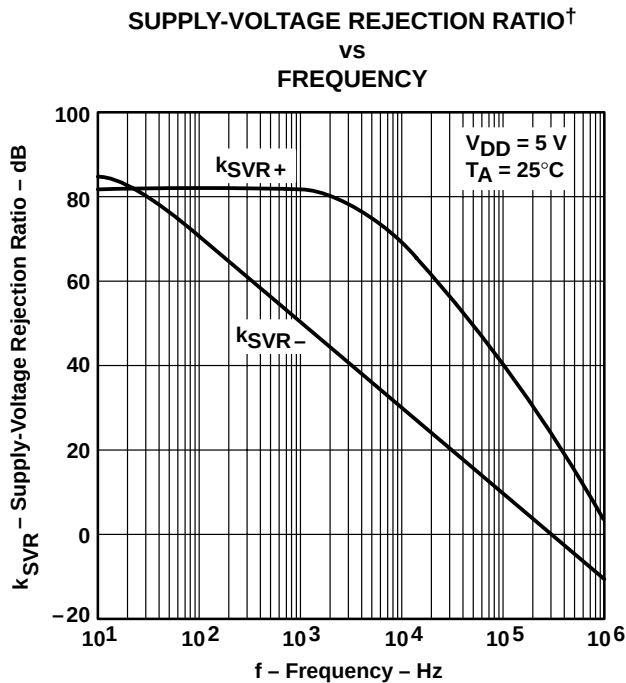
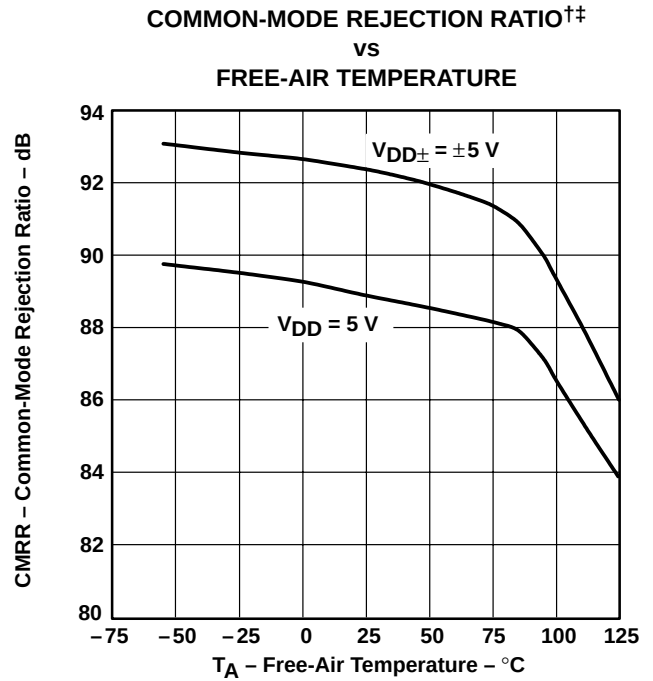
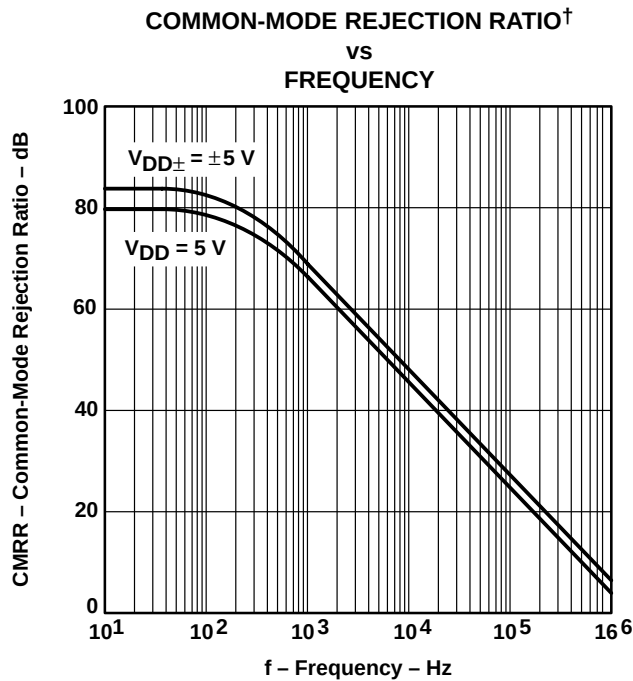


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



[†] For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V .

[‡] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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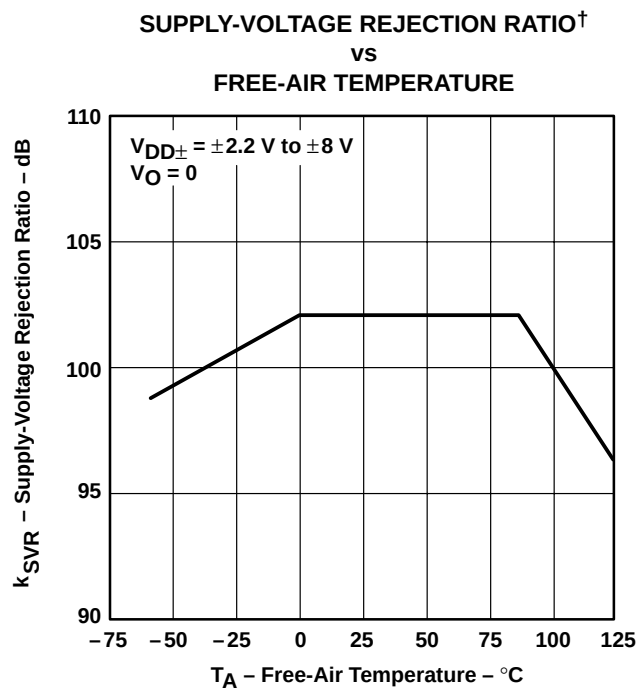


Figure 36

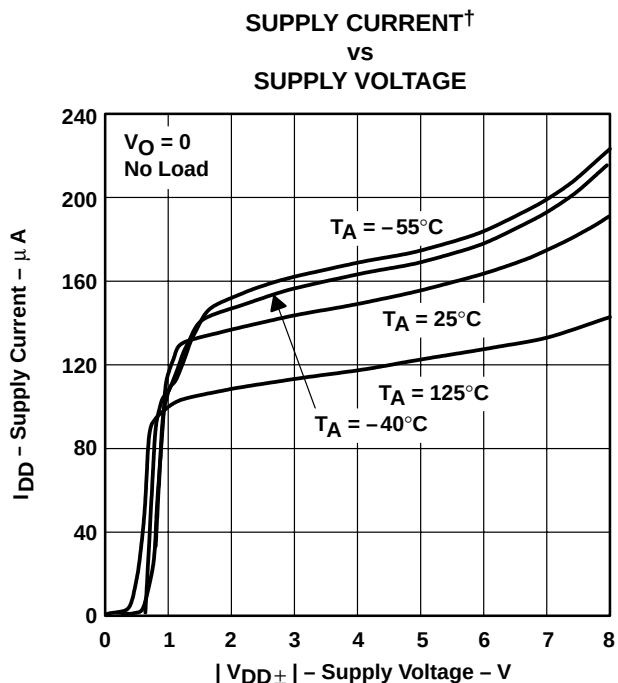


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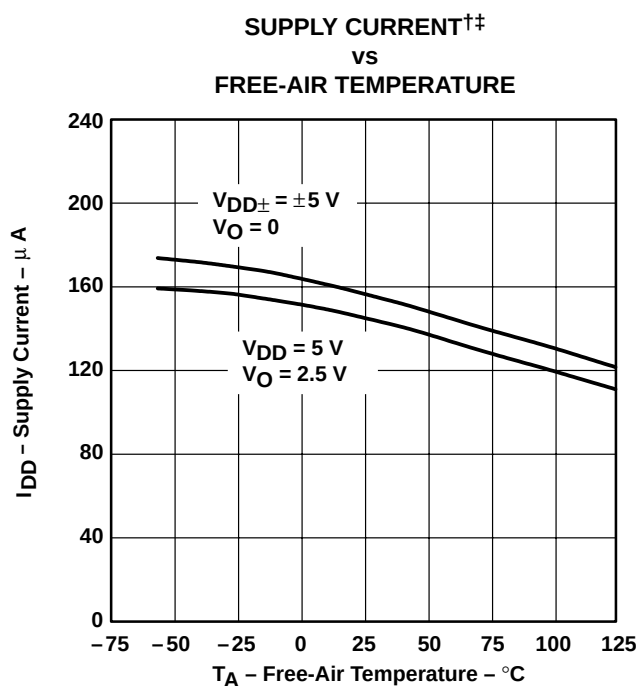


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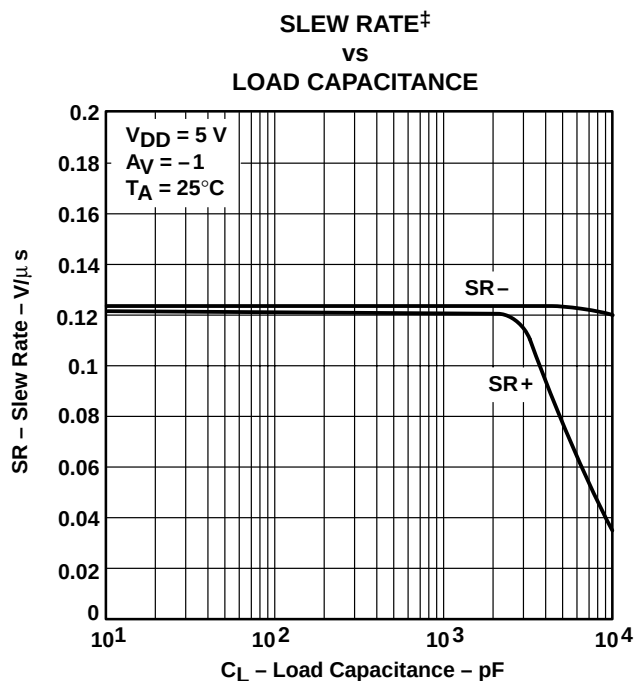
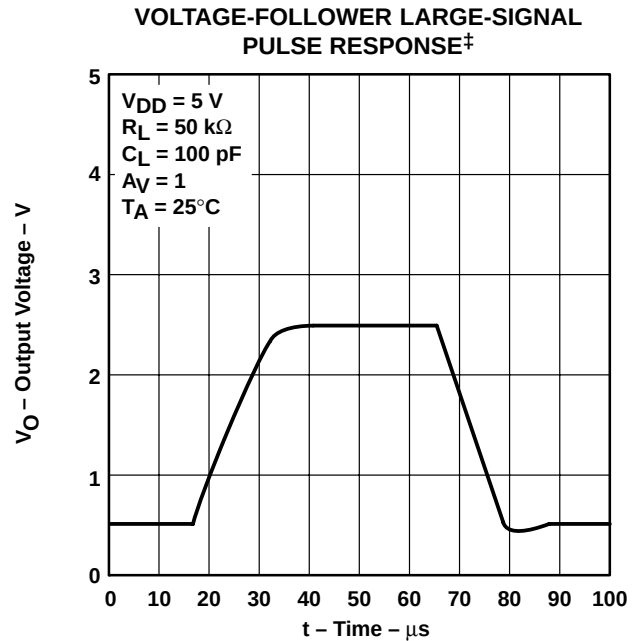
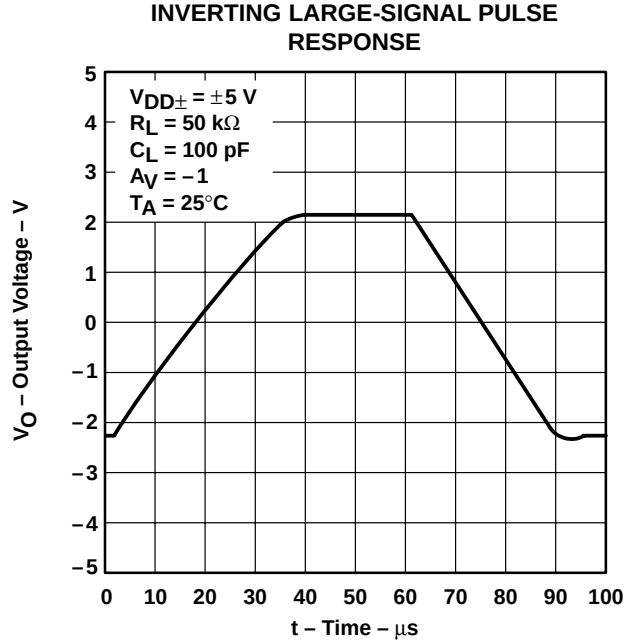
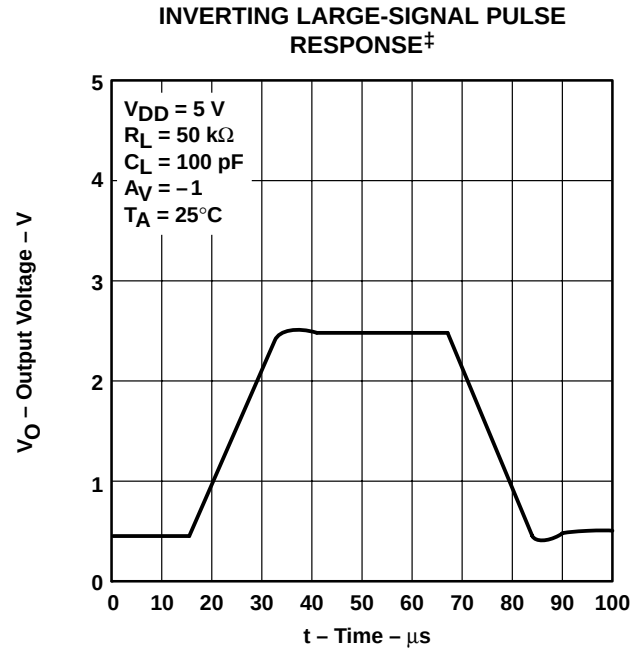
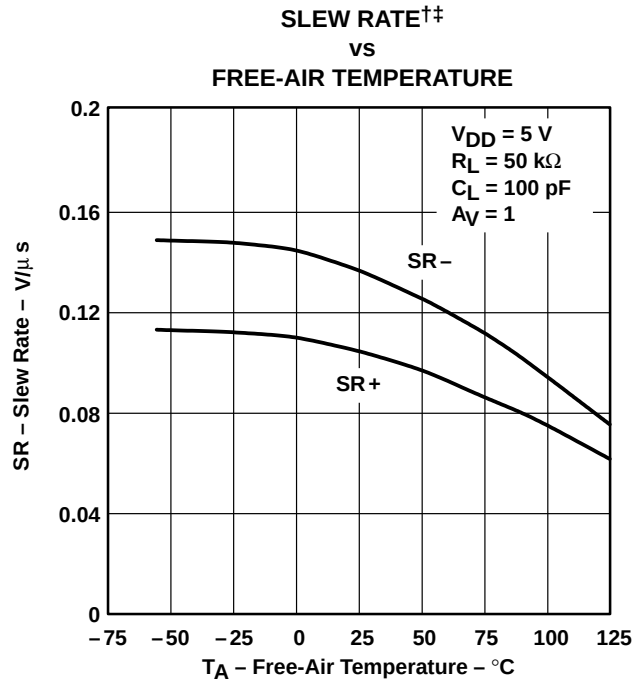


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

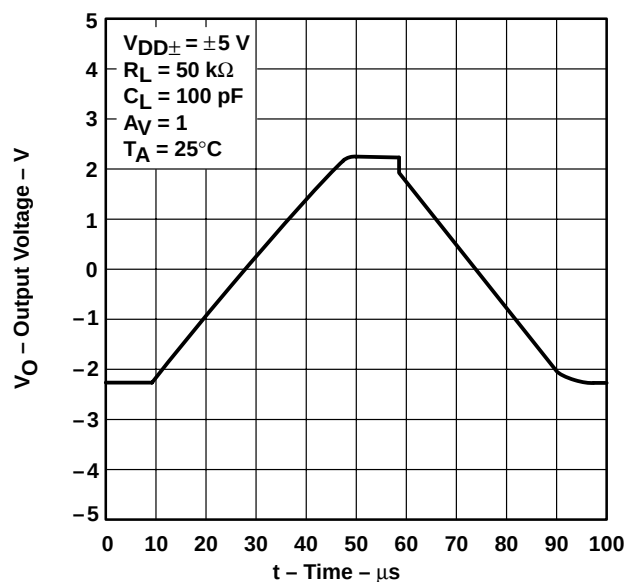


Figure 44

INVERTING SMALL-SIGNAL PULSE RESPONSE†

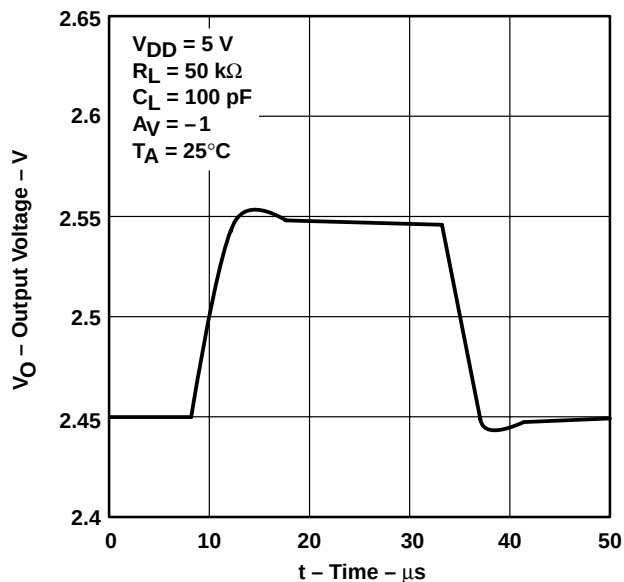


Figure 45

INVERTING SMALL-SIGNAL PULSE RESPONSE

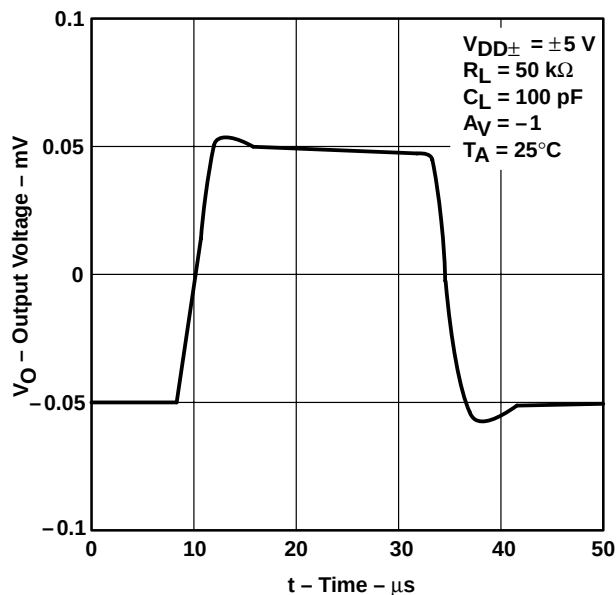


Figure 46

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

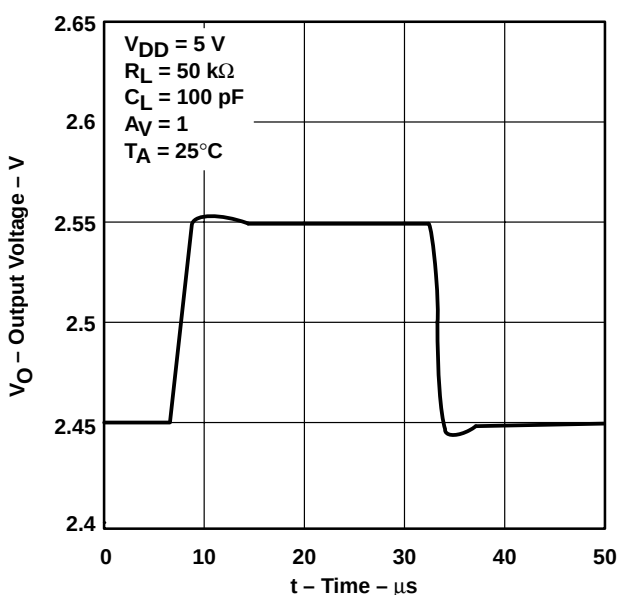


Figure 47

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

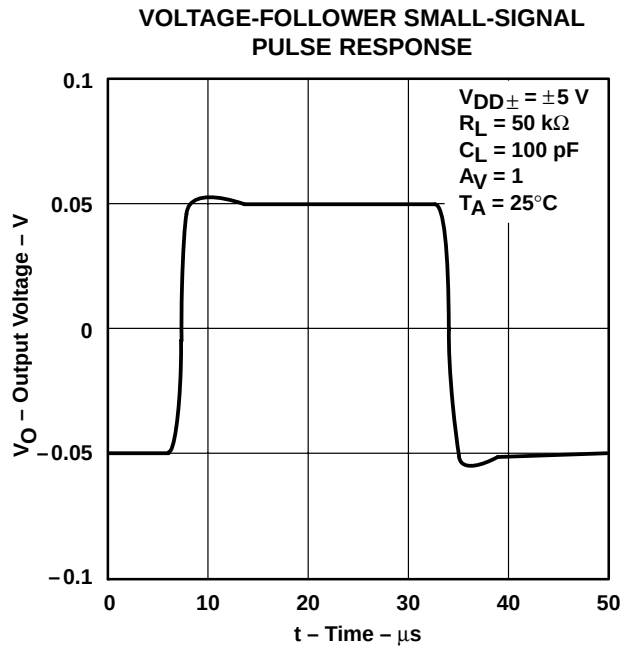


Figure 48

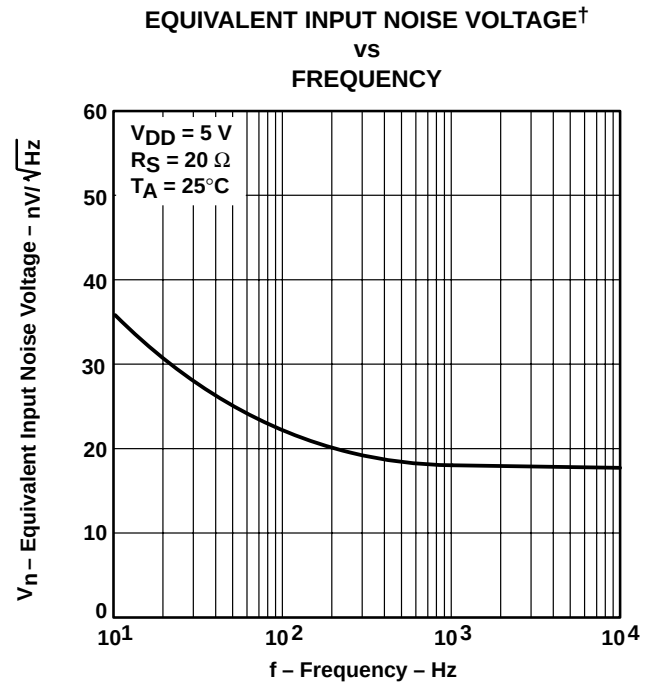


Figure 49

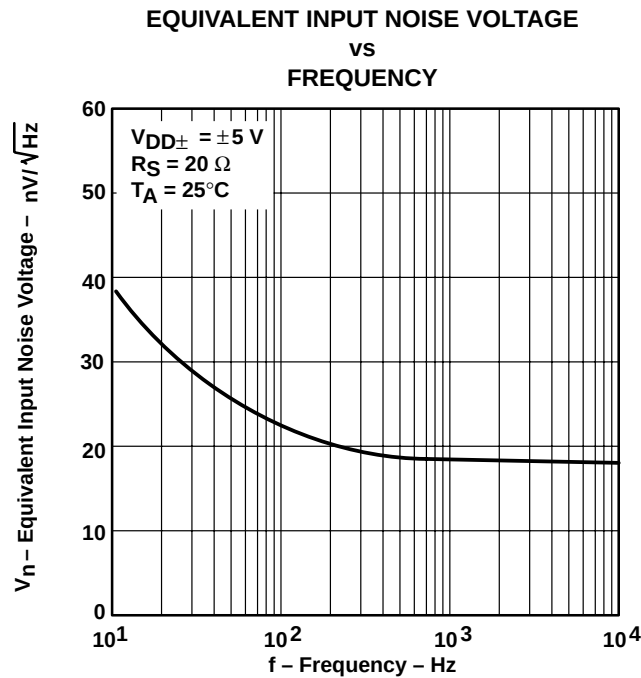


Figure 50

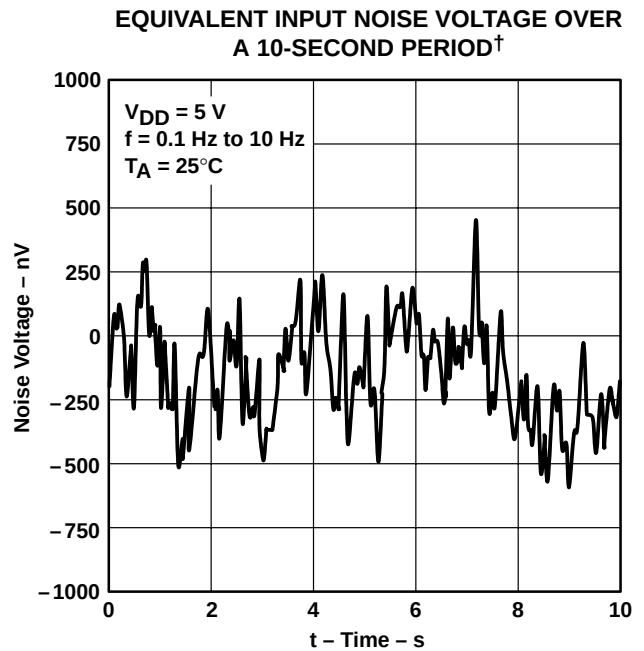


Figure 51

† For curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V.

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

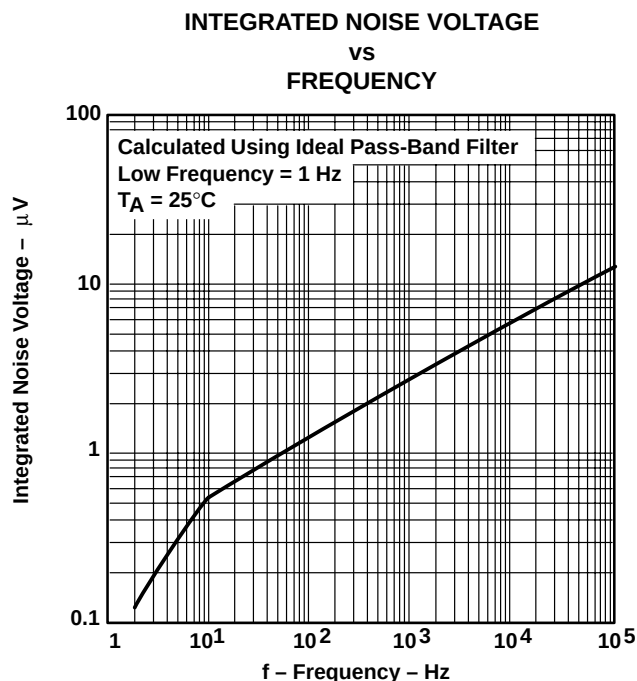


Figure 52

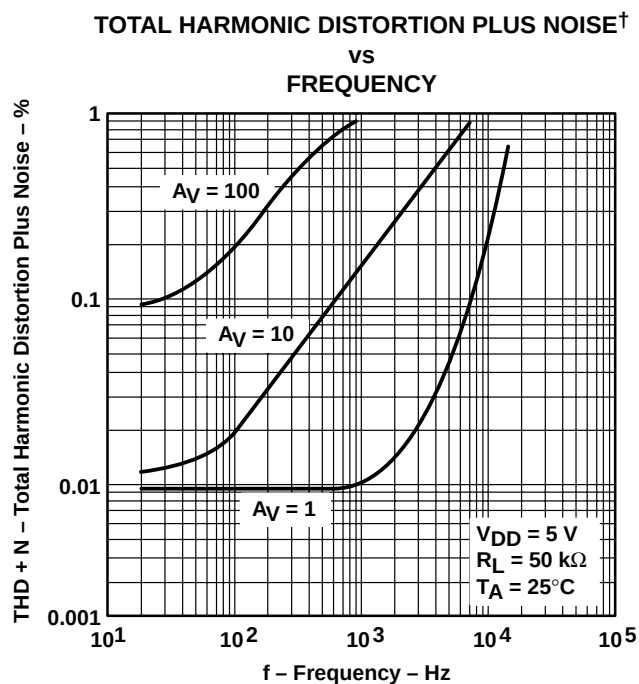


Figure 53

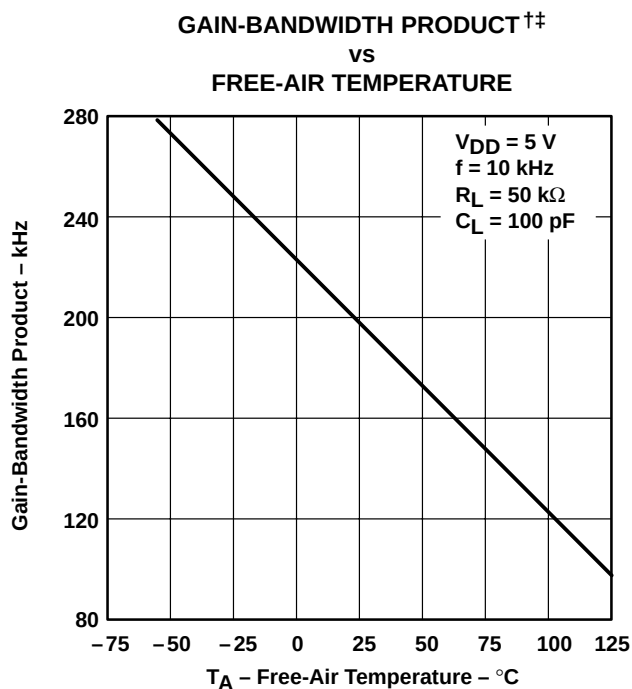


Figure 54

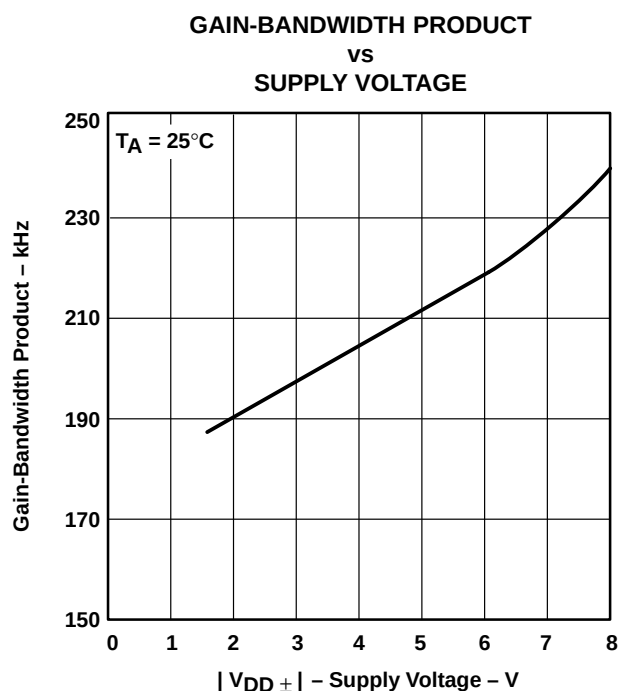
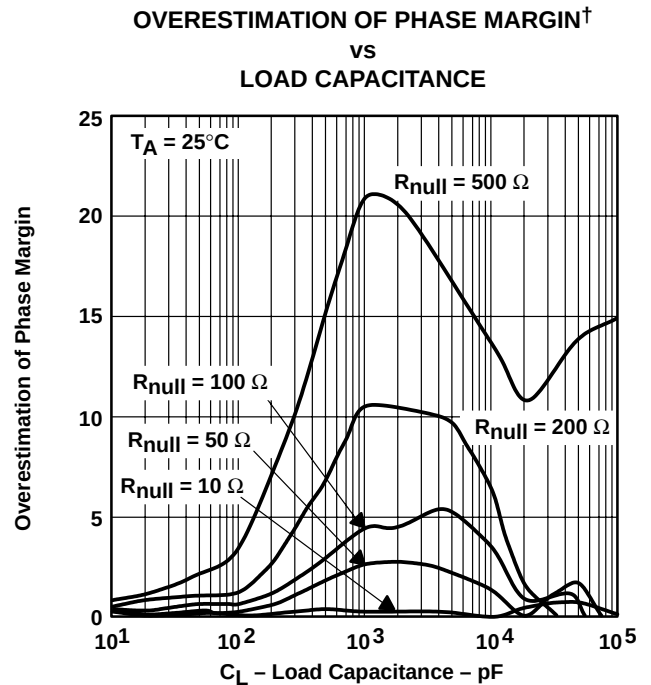
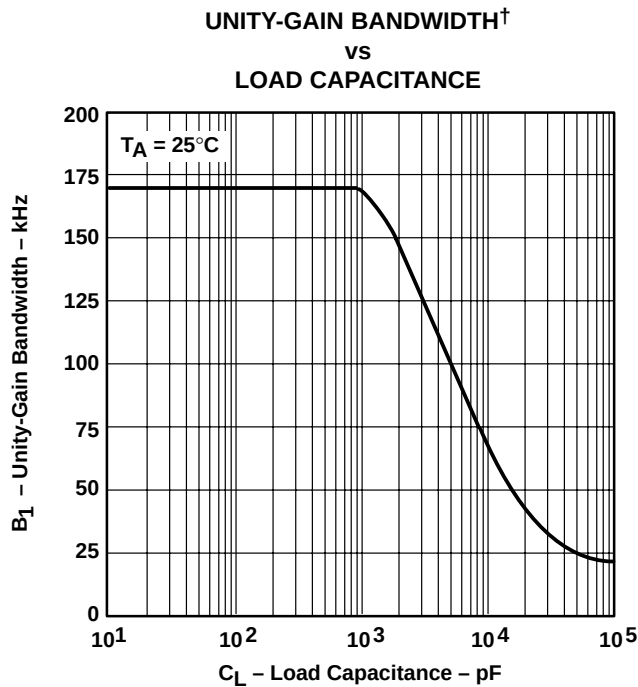
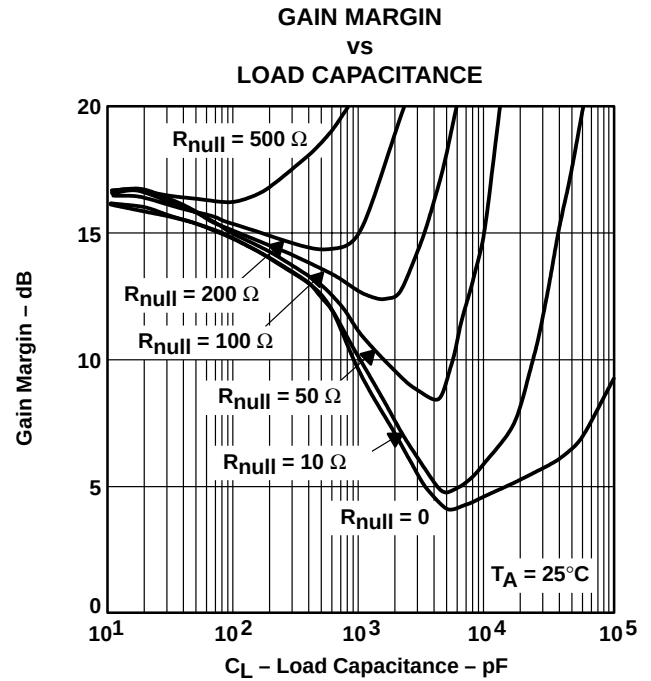
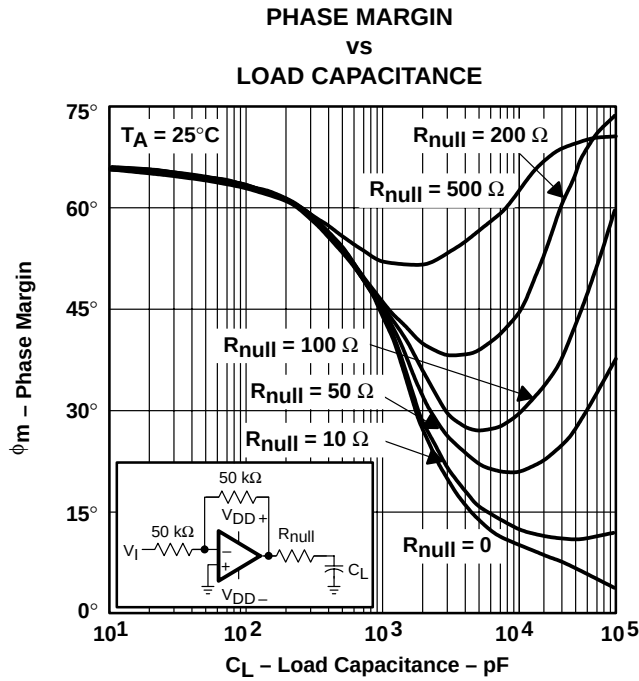


Figure 55

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V .

‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



† See application information

APPLICATION INFORMATION

driving large capacitive loads

The TLC225x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 56 and Figure 57 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 60) improves the gain and phase margins when driving large capacitive loads. Figure 56 and Figure 57 show the effects of adding series resistances of 10 Ω , 50 Ω , 100 Ω , 200 Ω , and 500 Ω . The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \quad (1)$$

Where :

- $\Delta\phi_{m1}$ = Improvement in phase margin
- UGBW = Unity-gain bandwidth frequency
- R_{null} = Output series resistance
- C_L = Load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 58). To use equation 1, UGBW must be approximated from Figure 58.

Using equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 59. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 60, with equation 1 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

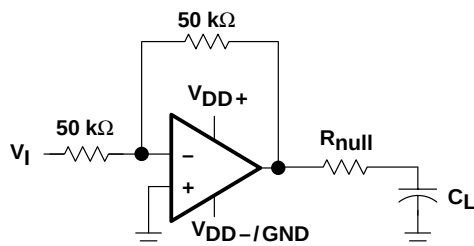


Figure 60. Series-Resistance Circuit

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using MicroSim *Parts*™, the model generation software used with MicroSim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 61 are generated using the TLC225x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

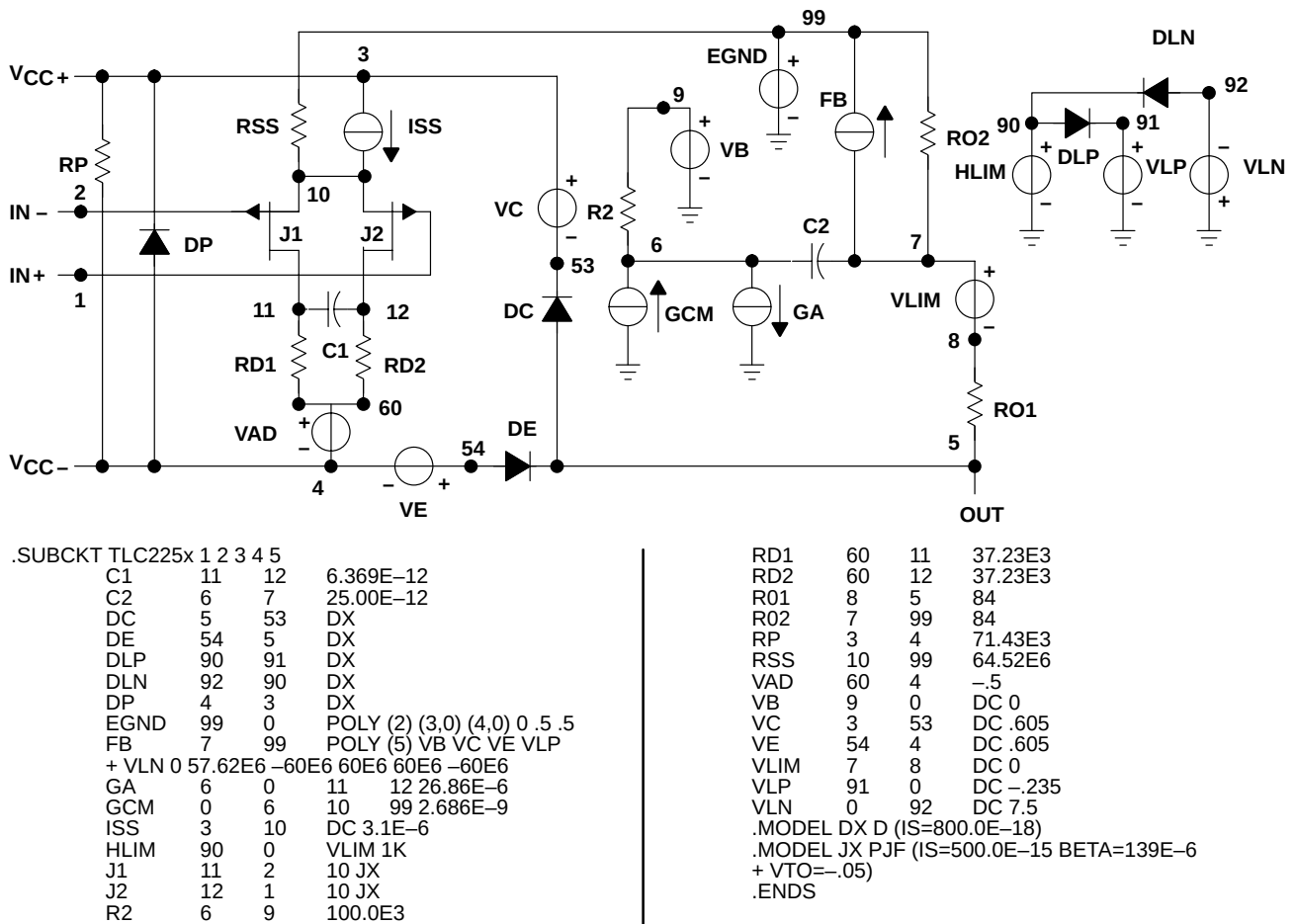


Figure 61. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9564001Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9564001Q2A TLC2252 MFKB
5962-9564001QHA	Active	Production	CFP (U) 10	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9564001QHA TLC2252M
5962-9564001QPA	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9564001QPA TLC2252M
5962-9564002Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9564002Q2A TLC2254 MFKB
5962-9564002QDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9564002QD A TLC2254MWB
5962-9564003NXD	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q2252A
5962-9564003NXDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q2252A
5962-9564003NXDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q2252A
5962-9564003Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9564003Q2A TLC2252 AMFKB
5962-9564003QHA	Active	Production	CFP (U) 10	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9564003QHA TLC2252AM
5962-9564003QPA	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9564003QPA TLC2252AM
5962-9564004Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9564004Q2A TLC2254 AMFKB
5962-9564004QDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9564004QD A TLC2254AMWB
TLC2252AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2252AI

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2252AID.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252AI
TLC2252AIDG4	Active	Production	SOIC (D) 8	75 TUBE	-	Call TI	Call TI	See TLC2252AID	
TLC2252AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2252AI
TLC2252AIDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252AI
TLC2252AIDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Call TI	See TLC2252AIDR	
TLC2252AIP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC2252AI
TLC2252AIP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC2252AI
TLC2252AIPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	Y2252A
TLC2252AIPWR.B	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2252A
TLC2252AMFKB	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9564003Q2A TLC2252 AMFKB
TLC2252AMFKB.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9564003Q2A TLC2252 AMFKB
TLC2252AMJGB	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9564003QPA TLC2252AM
TLC2252AMJGB.A	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9564003QPA TLC2252AM
TLC2252AMUB	Active	Production	CFP (U) 10	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9564003QHA TLC2252AM
TLC2252AMUB.A	Active	Production	CFP (U) 10	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9564003QHA TLC2252AM
TLC2252AQDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2252A
TLC2252AQDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2252A
TLC2252CD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2252C
TLC2252CD.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2252C
TLC2252CDG4	Active	Production	SOIC (D) 8	75 TUBE	-	Call TI	Call TI	0 to 70	
TLC2252CDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2252C
TLC2252CDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2252C
TLC2252CP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2252CP

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2252CP.B	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2252CP
TLC2252CPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2252
TLC2252CPWR.B	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2252
TLC2252IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252I
TLC2252IDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252I
TLC2252IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC2252IP
TLC2252IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC2252IP
TLC2252MFKB	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9564001Q2A TLC2252 MFKB
TLC2252MFKB.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9564001Q2A TLC2252 MFKB
TLC2252MJGB	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9564001QPA TLC2252M
TLC2252MJGB.A	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9564001QPA TLC2252M
TLC2252MUB	Active	Production	CFP (U) 10	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9564001QHA TLC2252M
TLC2252MUB.A	Active	Production	CFP (U) 10	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9564001QHA TLC2252M
TLC2254AID	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2254AI
TLC2254AID.B	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	See TLC2254AID	2254AI
TLC2254AIDG4	Active	Production	SOIC (D) 14	50 TUBE	-	Call TI	Call TI	See TLC2254AID	
TLC2254AIDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2254AI
TLC2254AIDR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See TLC2254AIDR	2254AI
TLC2254AIDRG4	Active	Production	SOIC (D) 14	2500 LARGE T&R	-	Call TI	Call TI	See TLC2254AIDR	
TLC2254AIN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC2254AIN
TLC2254AIN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	See TLC2254AIN	TLC2254AIN
TLC2254AIPW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-	Y2254A
TLC2254AIPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	Y2254A

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2254AIPWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See TLC2254AIPWR	Y2254A
TLC2254AIPWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	-	Call TI	Call TI	See TLC2254AIPWR	
TLC2254AMFKB	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9564004Q2A TLC2254 AMFKB
TLC2254AMFKB.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9564004Q2A TLC2254 AMFKB
TLC2254AMWB	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9564004QD A TLC2254AMWB
TLC2254AMWB.A	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9564004QD A TLC2254AMWB
TLC2254CDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2254C
TLC2254CDR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2254C
TLC2254CN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2254CN
TLC2254CN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2254CN
TLC2254CPW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2254
TLC2254CPW.B	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2254
TLC2254CPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2254
TLC2254CPWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2254
TLC2254ID	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC2254I
TLC2254ID.B	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2254I
TLC2254IDG4	Active	Production	SOIC (D) 14	50 TUBE	-	Call TI	Call TI	See TLC2254ID	
TLC2254IDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC2254I
TLC2254IDR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2254I
TLC2254IN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC2254IN
TLC2254IN.B	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2254IN

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2254MFKB	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9564002Q2A TLC2254 MFKB
TLC2254MFKB.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9564002Q2A TLC2254 MFKB
TLC2254MWB	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9564002QD A TLC2254MWB
TLC2254MWB.A	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9564002QD A TLC2254MWB

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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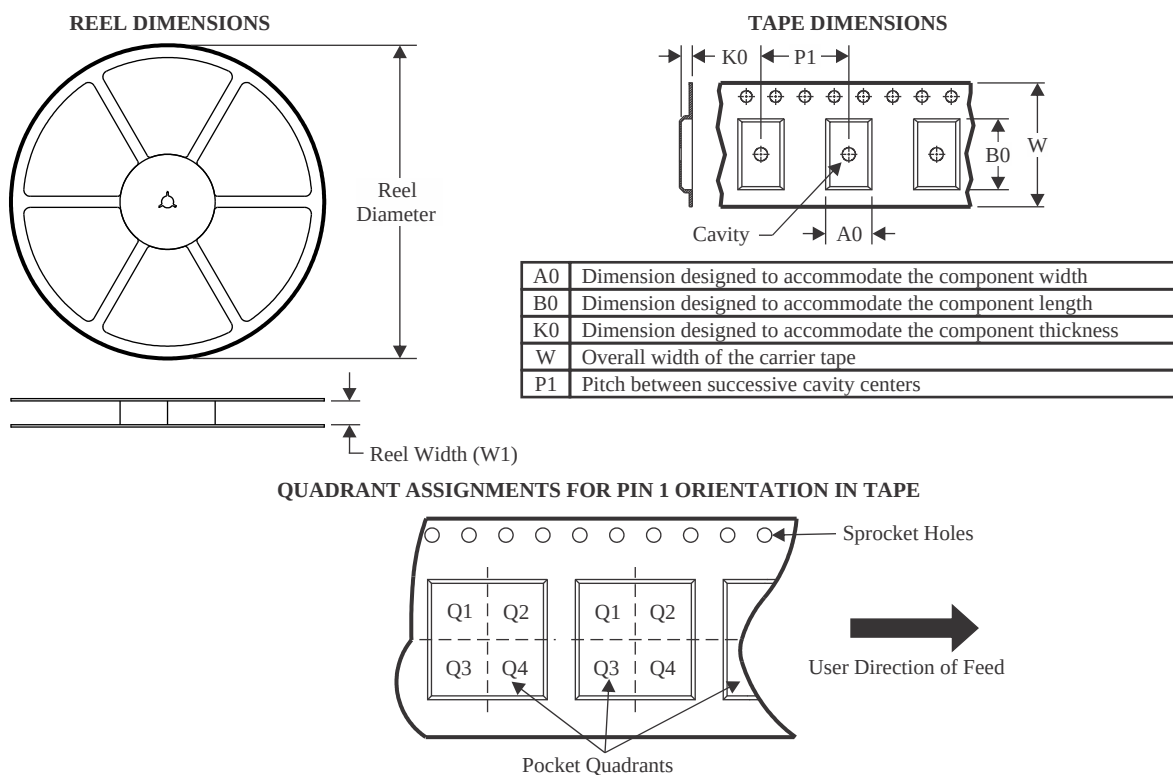
OTHER QUALIFIED VERSIONS OF TLC2252, TLC2252A, TLC2252AM, TLC2252M, TLC2254, TLC2254A, TLC2254AM, TLC2254M :

- Catalog : [TLC2252A](#), [TLC2252](#), [TLC2254A](#), [TLC2254](#)
- Automotive : [TLC2252A-Q1](#), [TLC2252A-Q1](#), [TLC2254A-Q1](#), [TLC2254A-Q1](#)
- Enhanced Product : [TLC2252A-EP](#), [TLC2252A-EP](#), [TLC2254A-EP](#), [TLC2254A-EP](#)
- Military : [TLC2252M](#), [TLC2252AM](#), [TLC2254M](#), [TLC2254AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

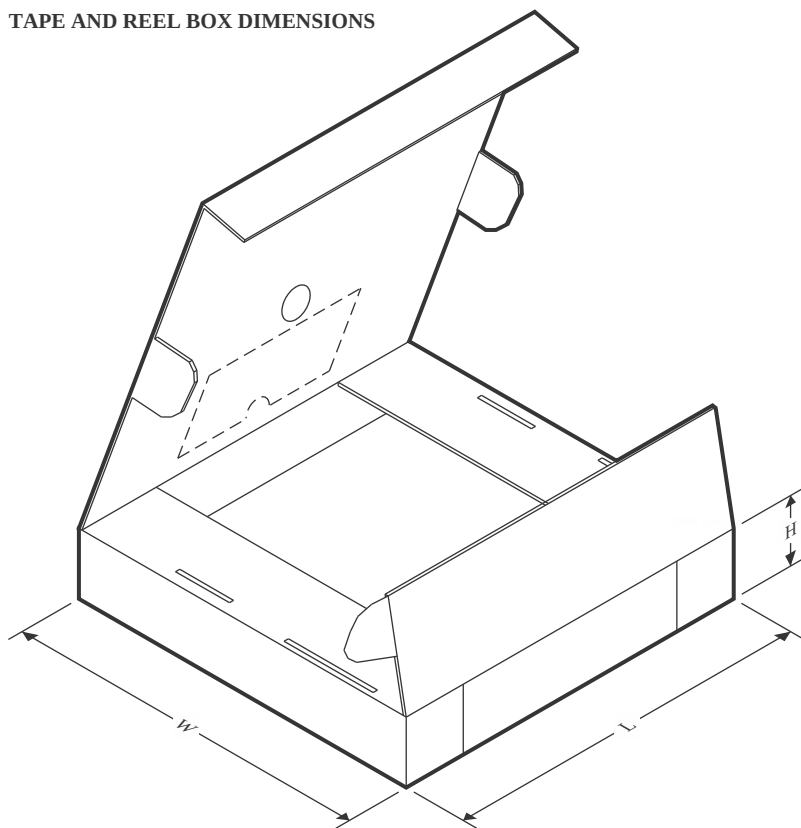
TAPE AND REEL INFORMATION



*All dimensions are nominal

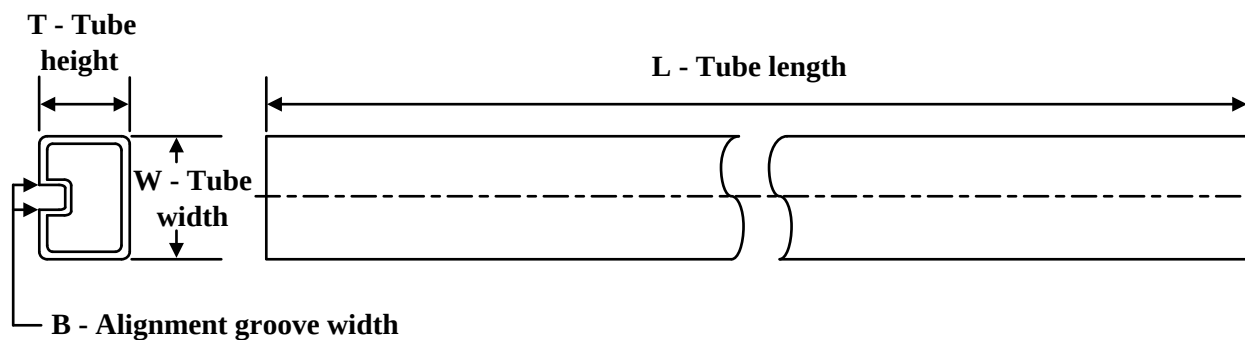
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
5962-9564003NXDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2252AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2252AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2252AQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TLC2252CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2252CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2252IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2254AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2254AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2254CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2254CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2254IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
5962-9564003NXDR	SOIC	D	8	2500	350.0	350.0	43.0
TLC2252AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC2252AIPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC2252AQDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC2252CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC2252CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC2252IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC2254AIDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC2254AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLC2254CDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2254CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLC2254IDR	SOIC	D	14	2500	333.2	345.9	28.6

TUBE


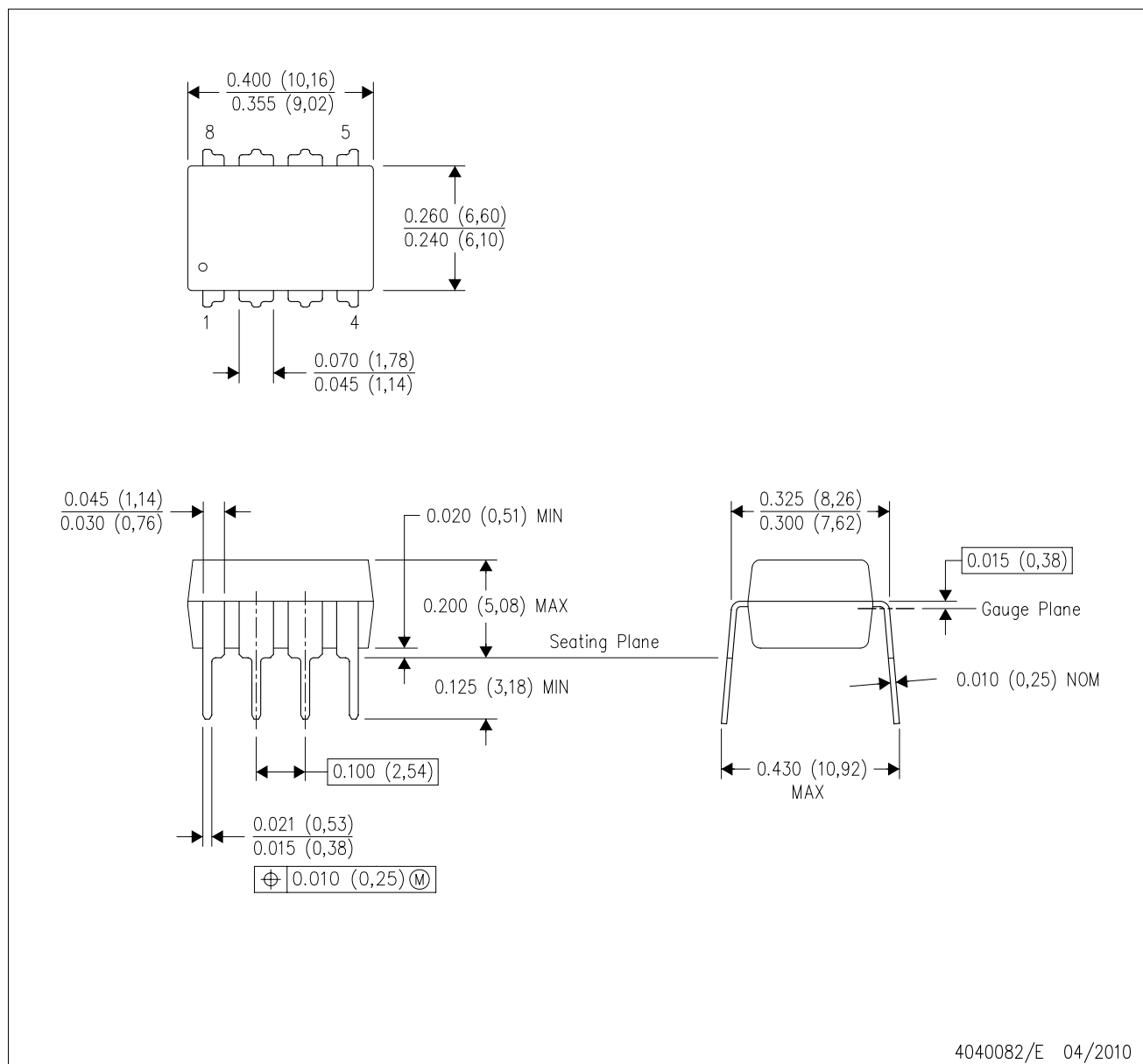
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9564001Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9564001QHA	U	CFP	10	25	506.98	26.16	6220	NA
5962-9564002Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9564002QDA	W	CFP	14	25	506.98	26.16	6220	NA
5962-9564003Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9564003QHA	U	CFP	10	25	506.98	26.16	6220	NA
5962-9564004Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9564004QDA	W	CFP	14	25	506.98	26.16	6220	NA
TLC2252AID	D	SOIC	8	75	507	8	3940	4.32
TLC2252AID	D	SOIC	8	75	505.46	6.76	3810	4
TLC2252AID.B	D	SOIC	8	75	505.46	6.76	3810	4
TLC2252AID.B	D	SOIC	8	75	507	8	3940	4.32
TLC2252AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC2252AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC2252AMFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2252AMFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2252AMUB	U	CFP	10	25	506.98	26.16	6220	NA
TLC2252AMUB.A	U	CFP	10	25	506.98	26.16	6220	NA
TLC2252CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC2252CD	D	SOIC	8	75	507	8	3940	4.32
TLC2252CD.B	D	SOIC	8	75	505.46	6.76	3810	4
TLC2252CD.B	D	SOIC	8	75	507	8	3940	4.32
TLC2252CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC2252CP.B	P	PDIP	8	50	506	13.97	11230	4.32
TLC2252IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC2252IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC2252MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2252MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2252MUB	U	CFP	10	25	506.98	26.16	6220	NA

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC2252MUB.A	U	CFP	10	25	506.98	26.16	6220	NA
TLC2254AID	D	SOIC	14	50	505.46	6.76	3810	4
TLC2254AID.B	D	SOIC	14	50	505.46	6.76	3810	4
TLC2254AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLC2254AIN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLC2254AMFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2254AMFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2254AMWB	W	CFP	14	25	506.98	26.16	6220	NA
TLC2254AMWB.A	W	CFP	14	25	506.98	26.16	6220	NA
TLC2254CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC2254CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLC2254CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC2254CPW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC2254ID	D	SOIC	14	50	507	8	3940	4.32
TLC2254ID	D	SOIC	14	50	505.46	6.76	3810	4
TLC2254ID.B	D	SOIC	14	50	505.46	6.76	3810	4
TLC2254ID.B	D	SOIC	14	50	507	8	3940	4.32
TLC2254IN	N	PDIP	14	25	506	13.97	11230	4.32
TLC2254IN.B	N	PDIP	14	25	506	13.97	11230	4.32
TLC2254MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2254MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2254MWB	W	CFP	14	25	506.98	26.16	6220	NA
TLC2254MWB.A	W	CFP	14	25	506.98	26.16	6220	NA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

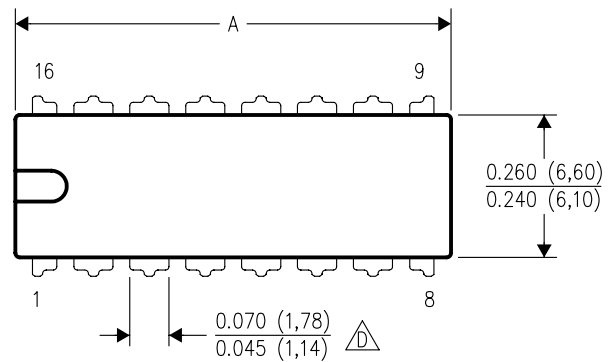


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

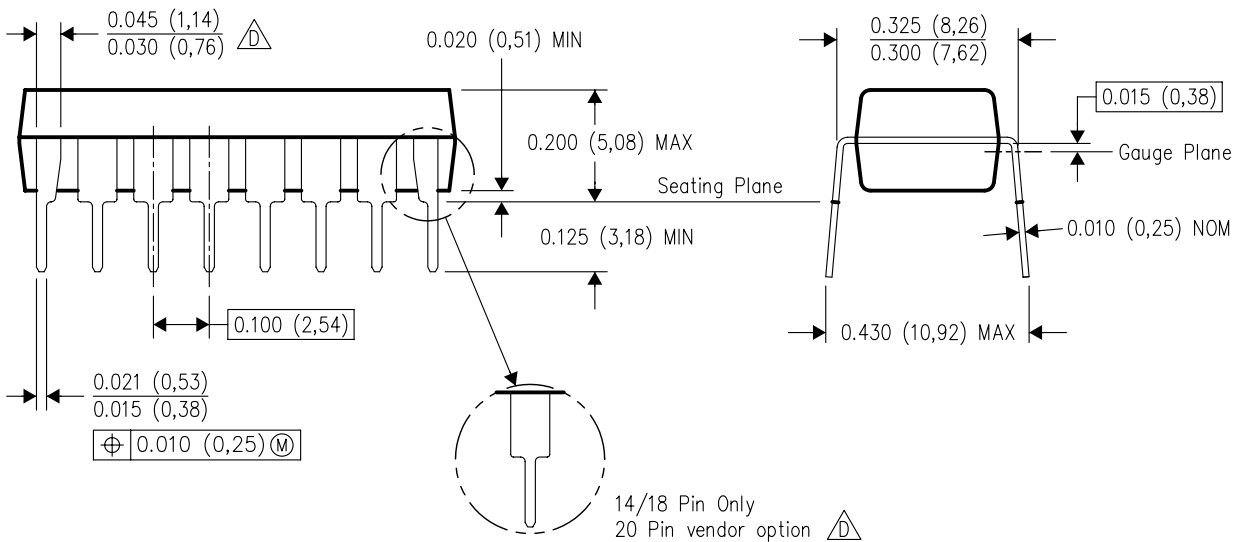
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



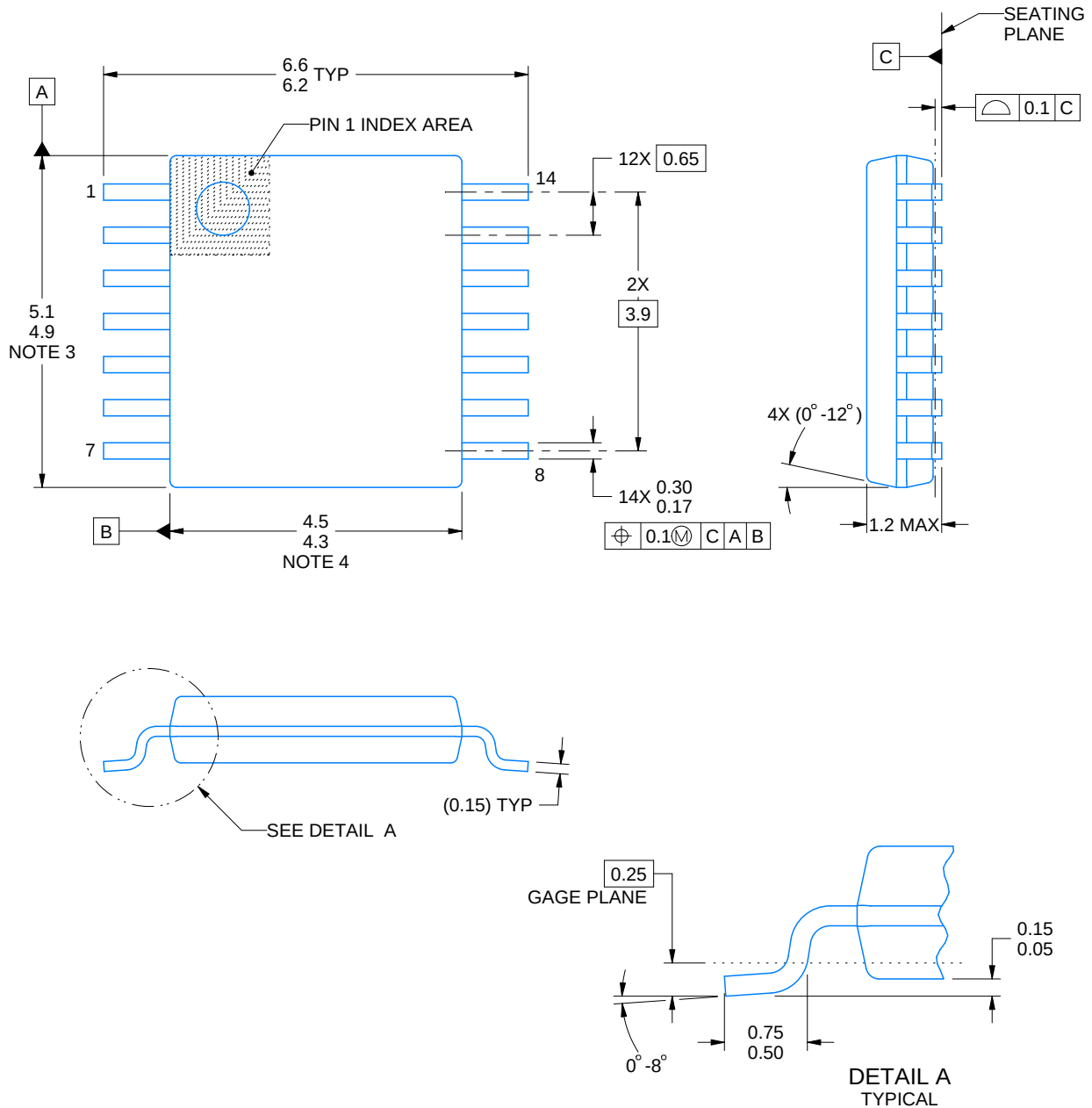
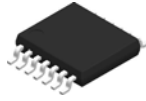
PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220202/B 12/2023

NOTES:

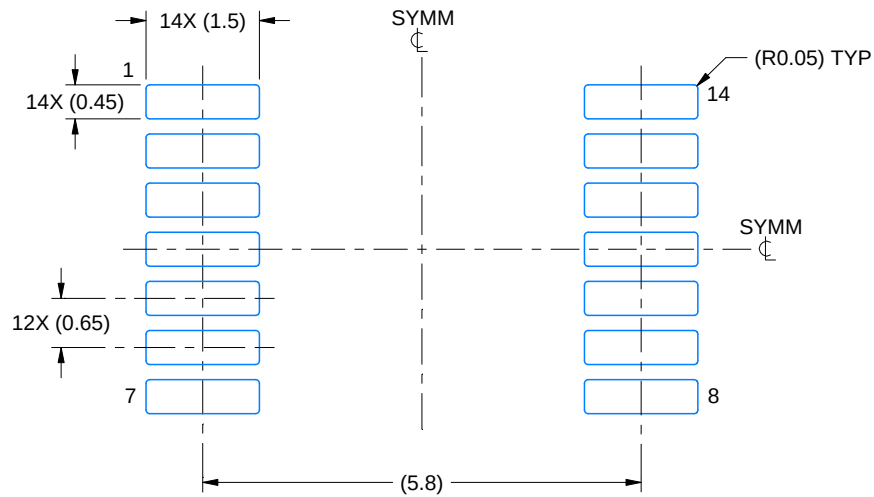
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

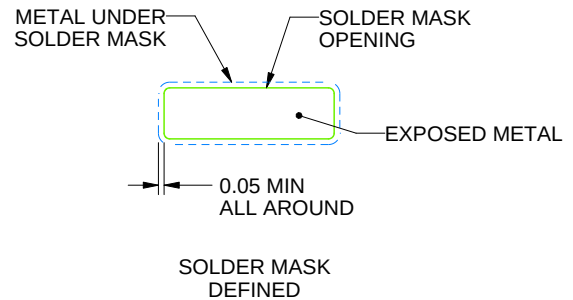
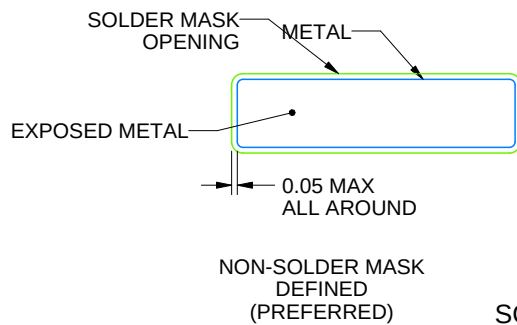
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

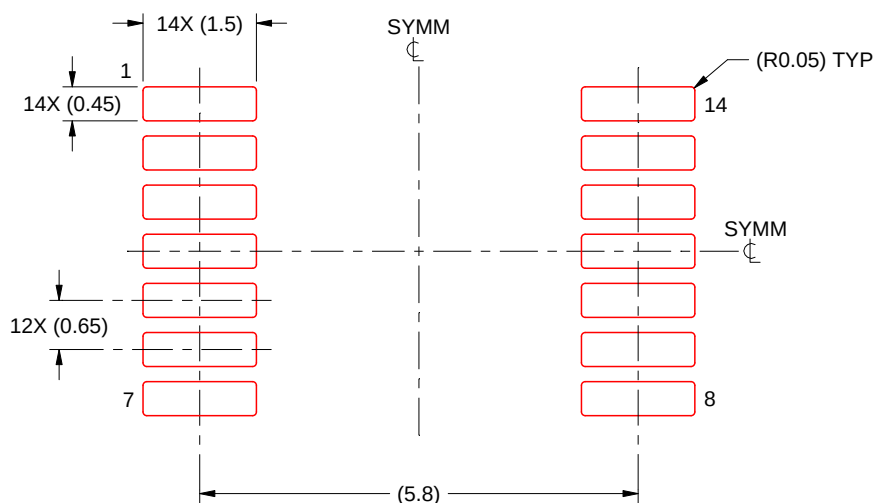
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

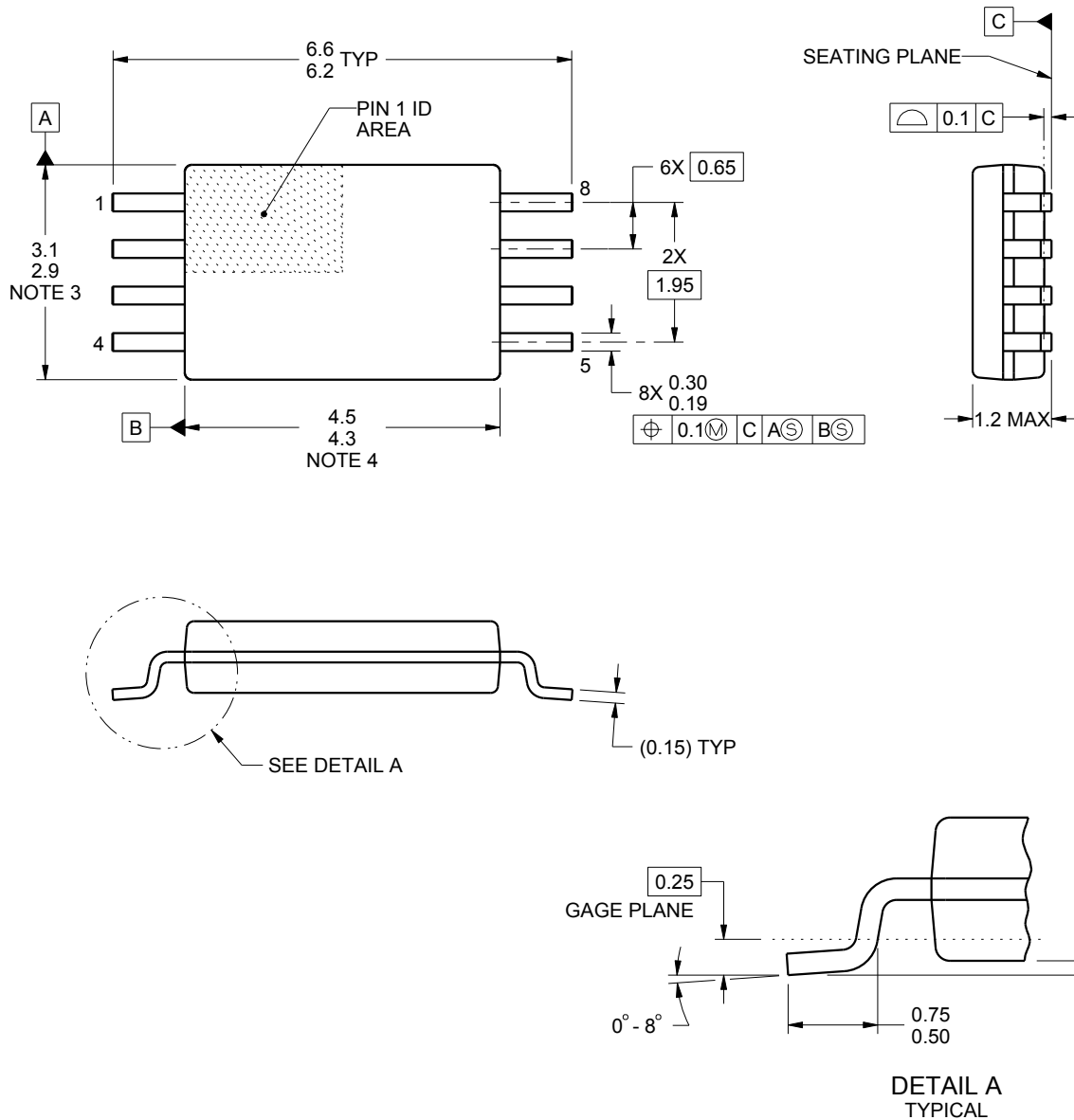
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

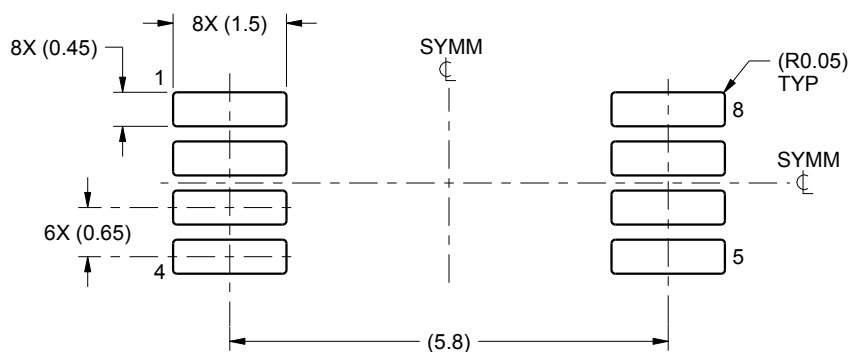
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

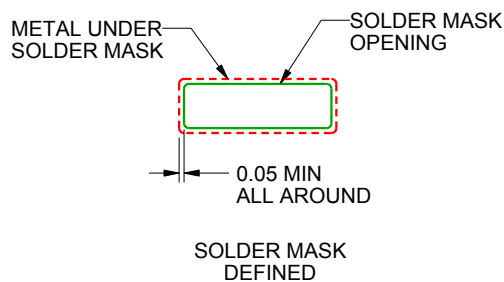
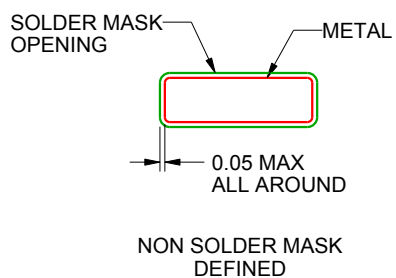
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

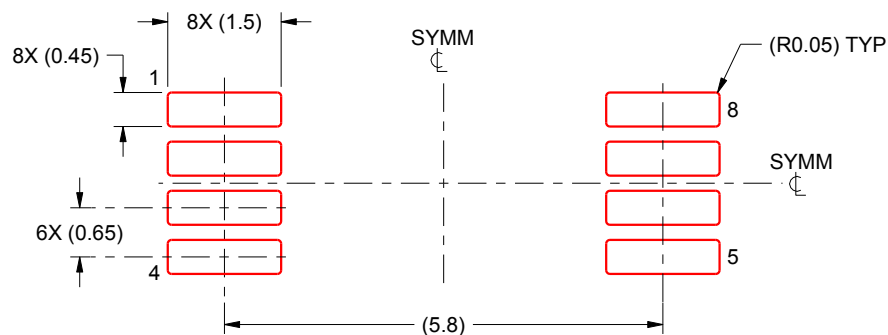
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

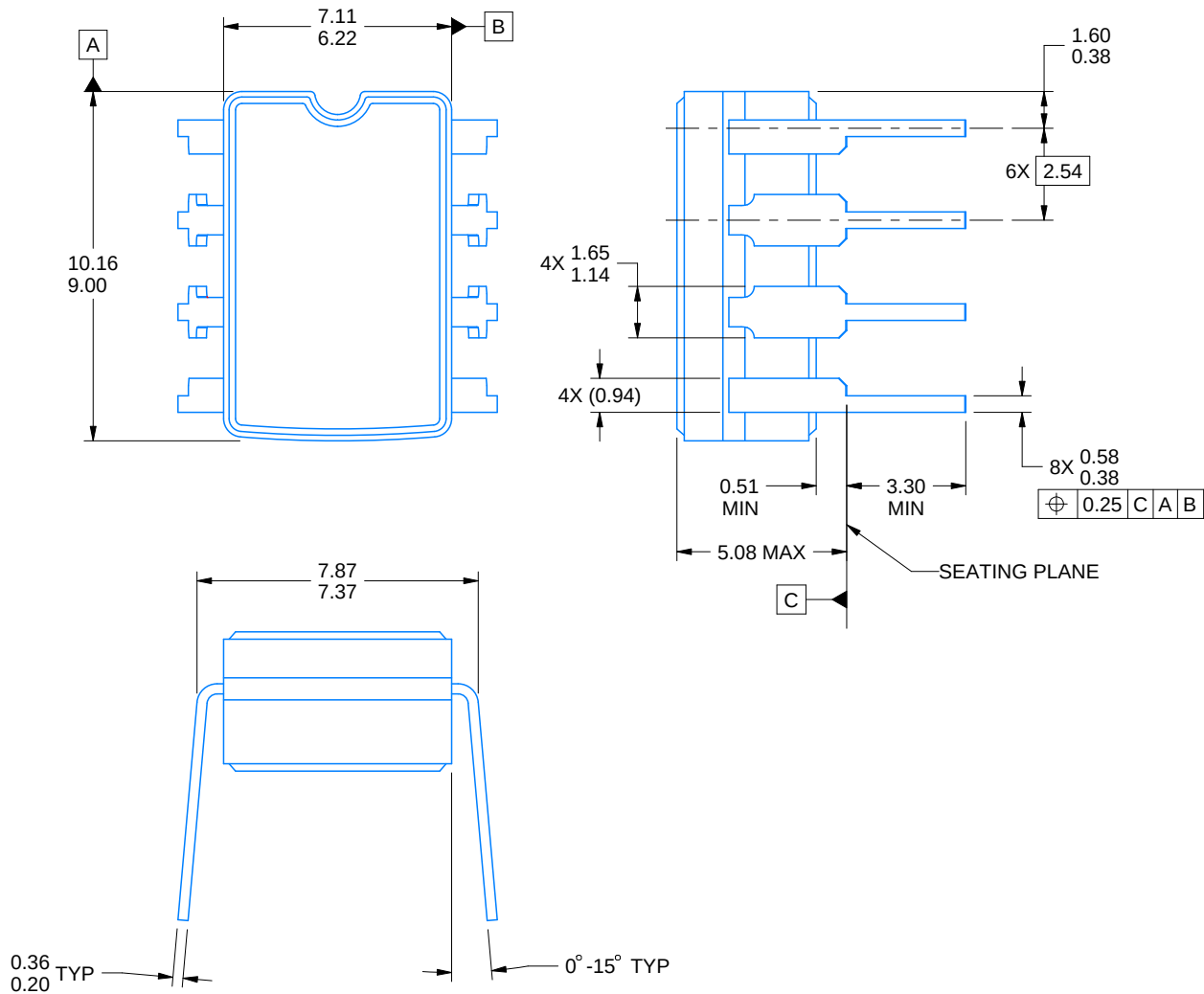
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG0008A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

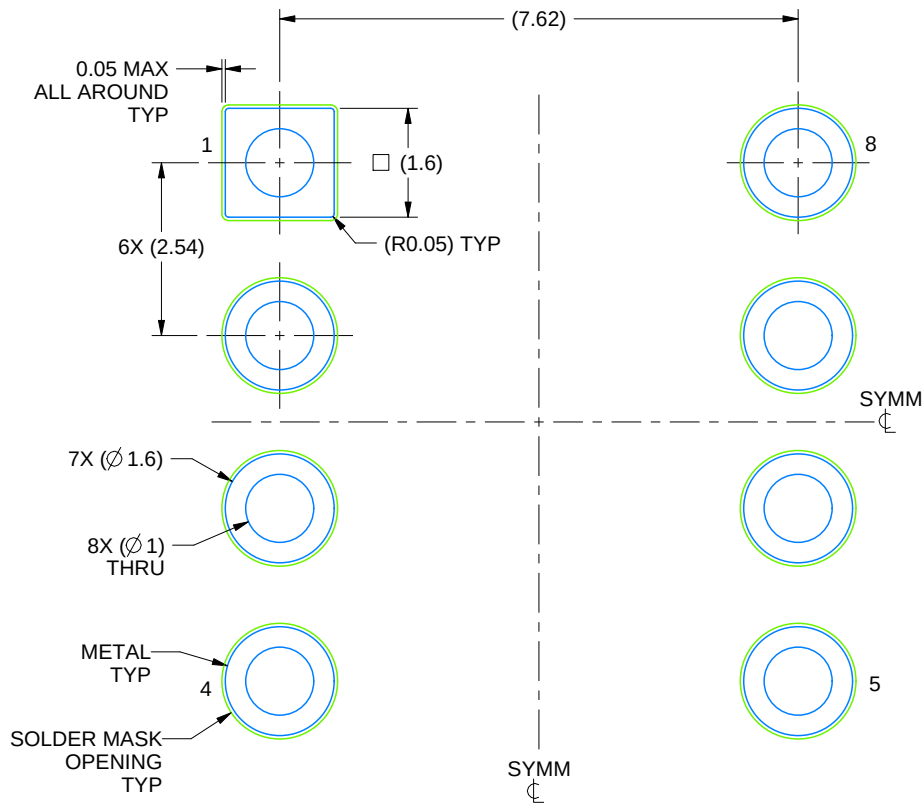
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

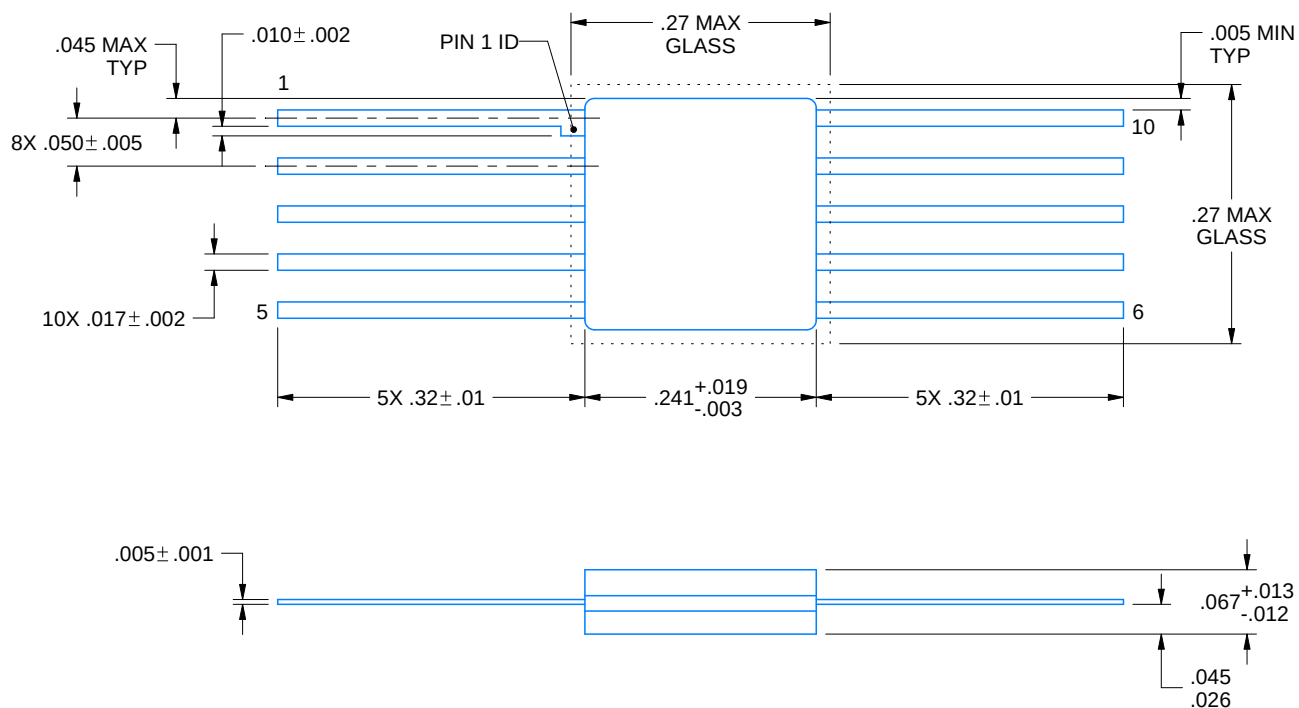
U0010A



PACKAGE OUTLINE

CFP - 2.03 mm max height

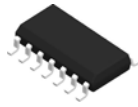
CERAMIC FLATPACK



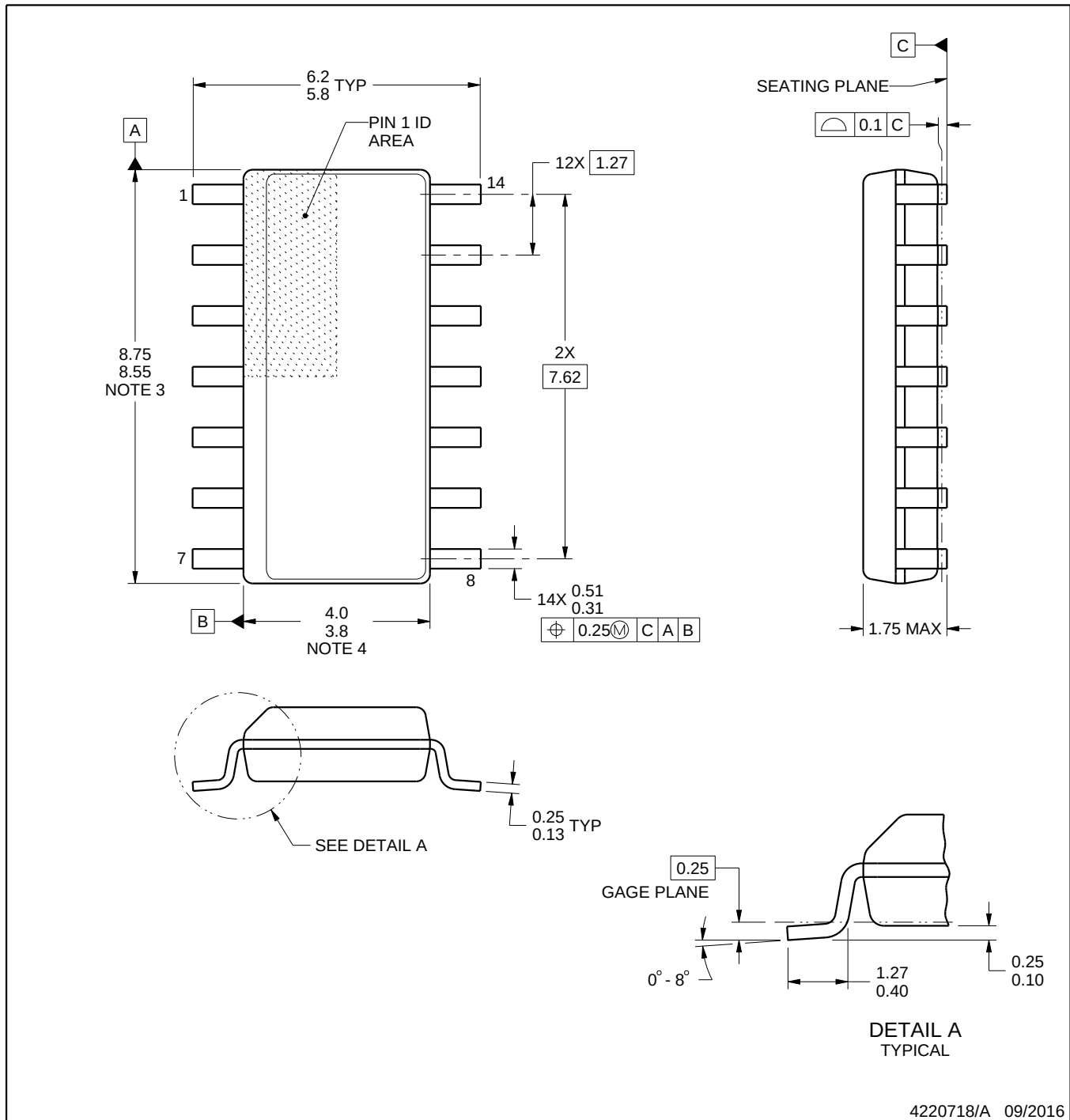
4225582/A 01/2020

NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

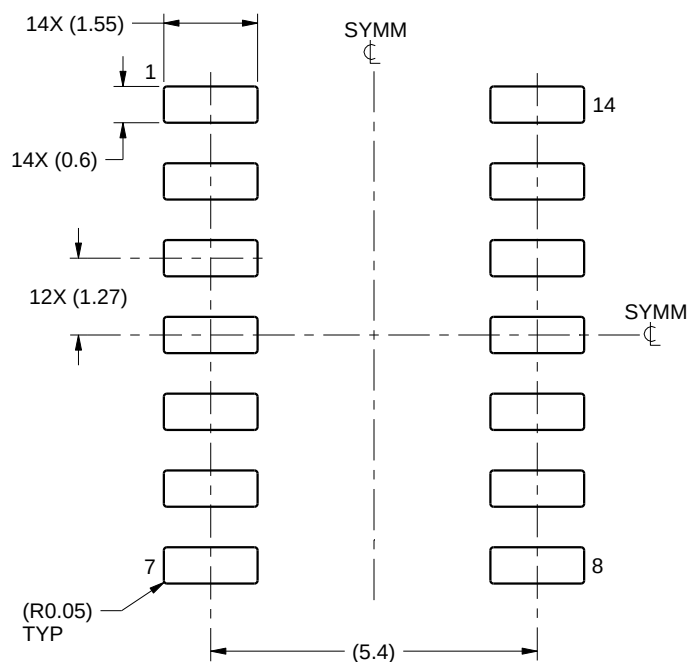
**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

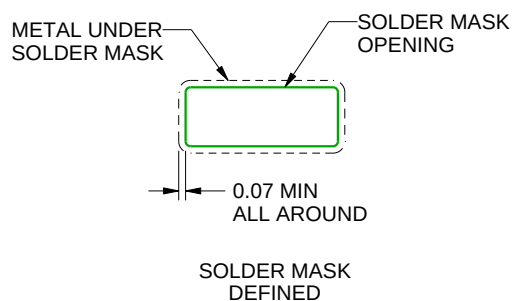
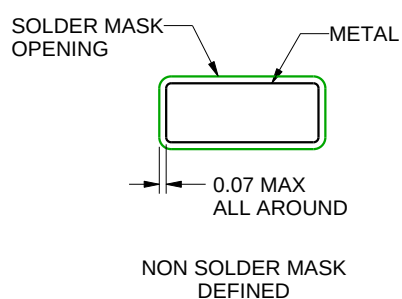
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

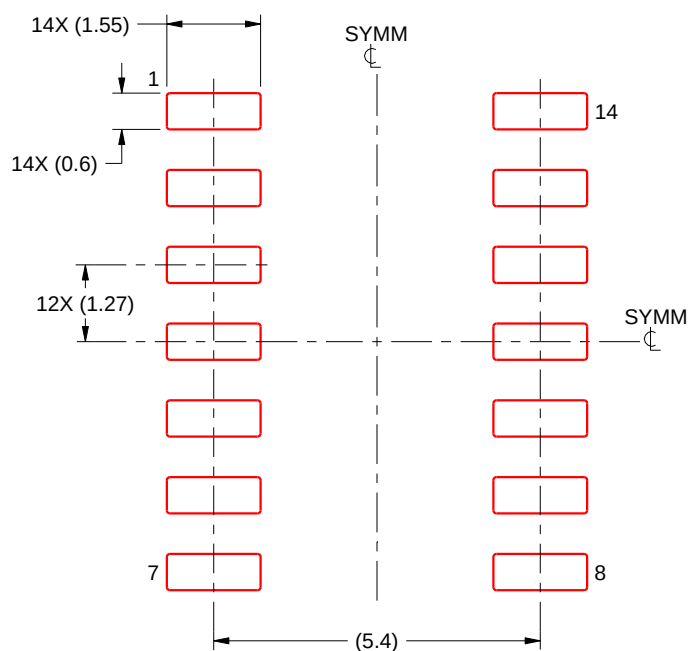
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

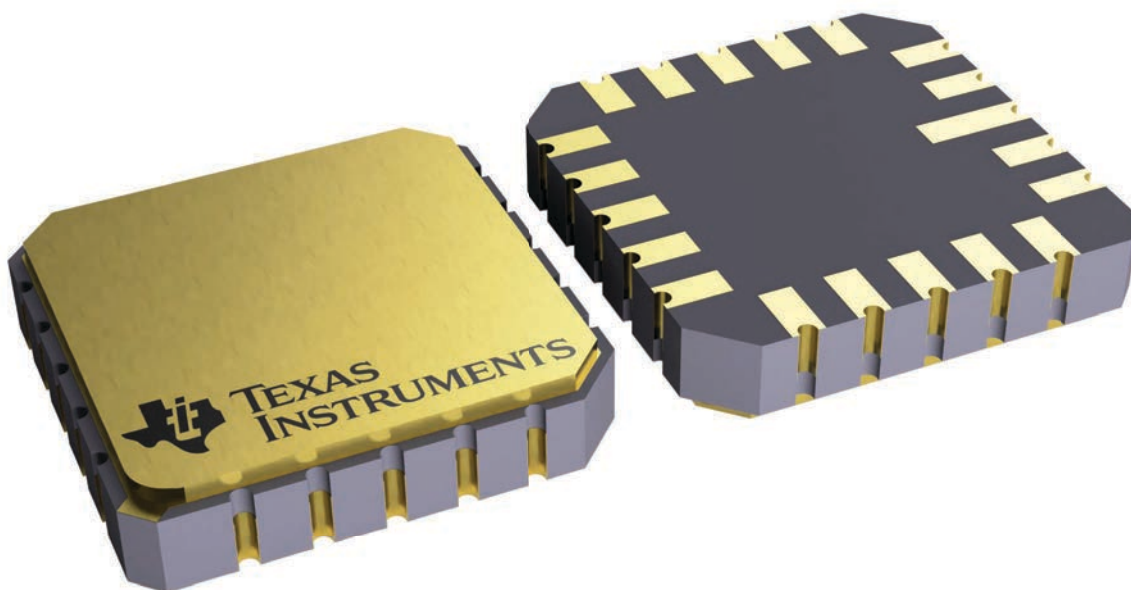
FK 20

LCCC - 2.03 mm max height

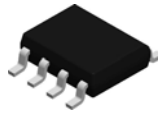
8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

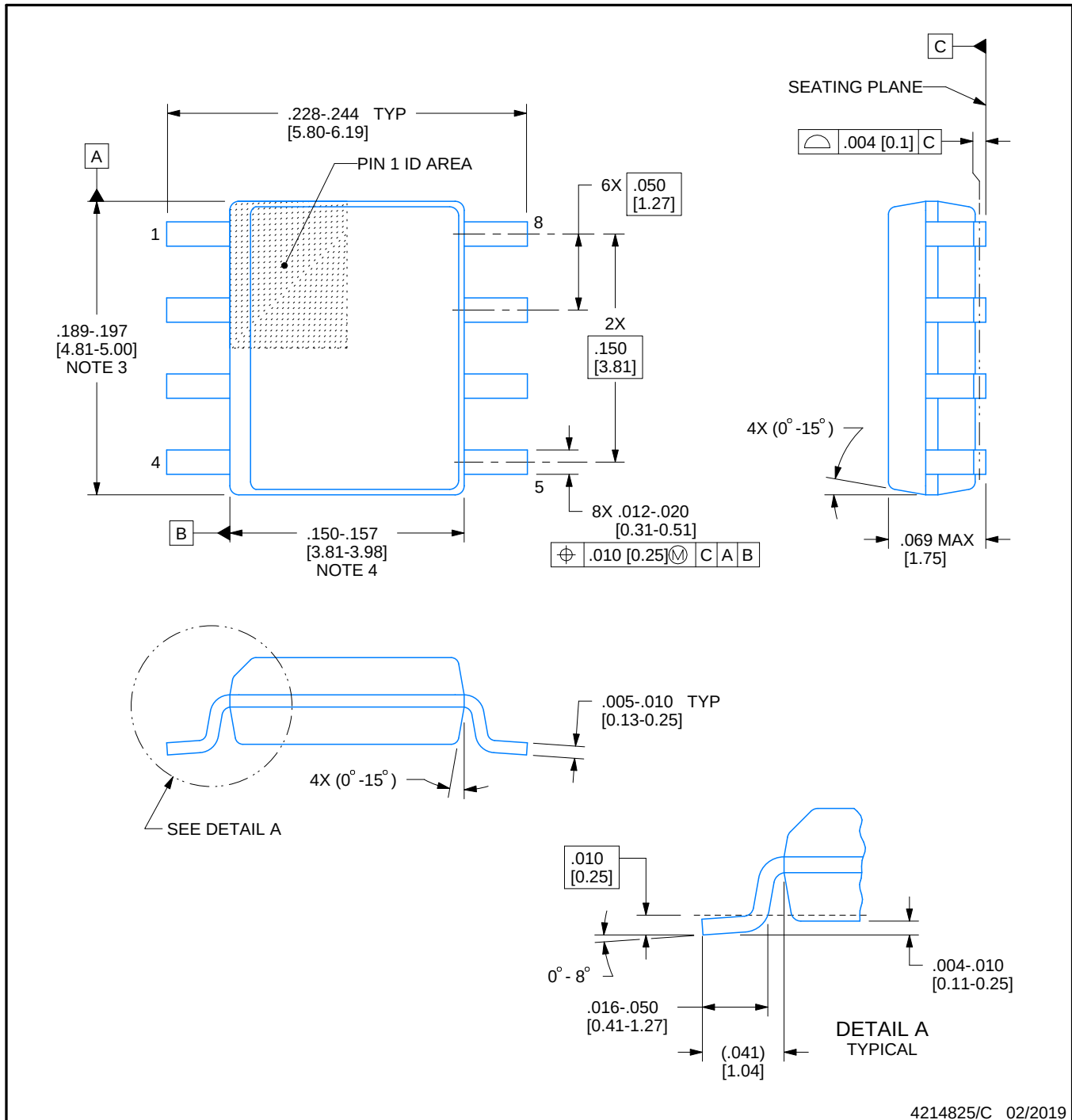
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

D0008A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

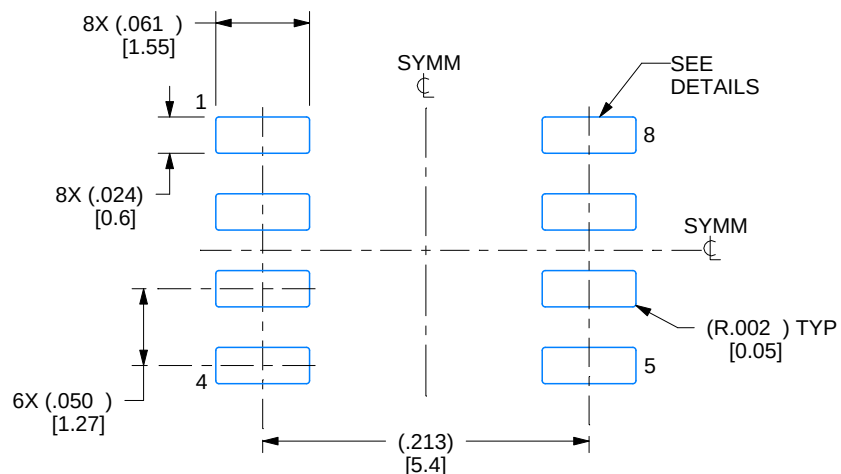
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

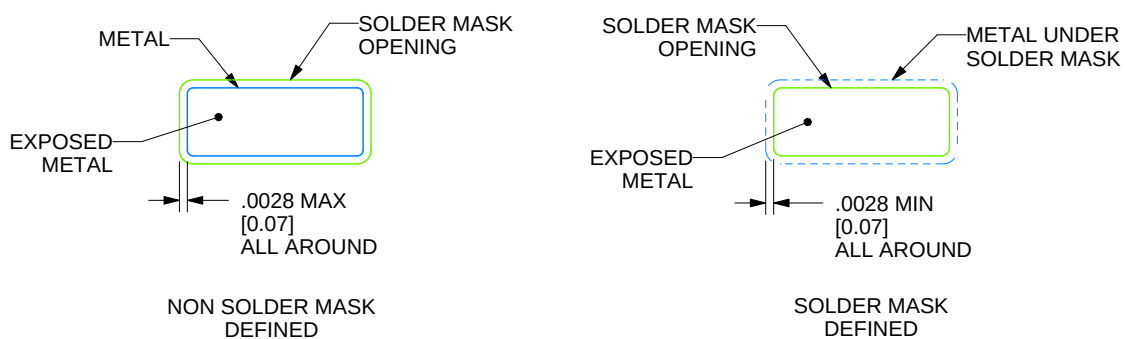
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

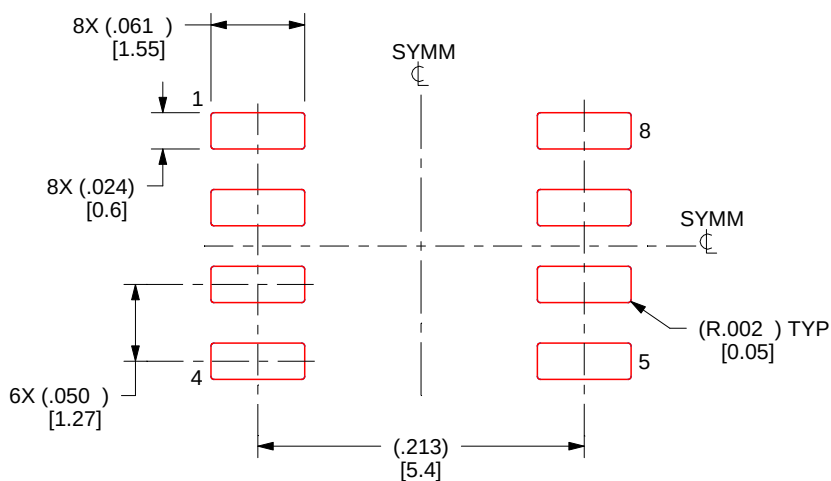
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

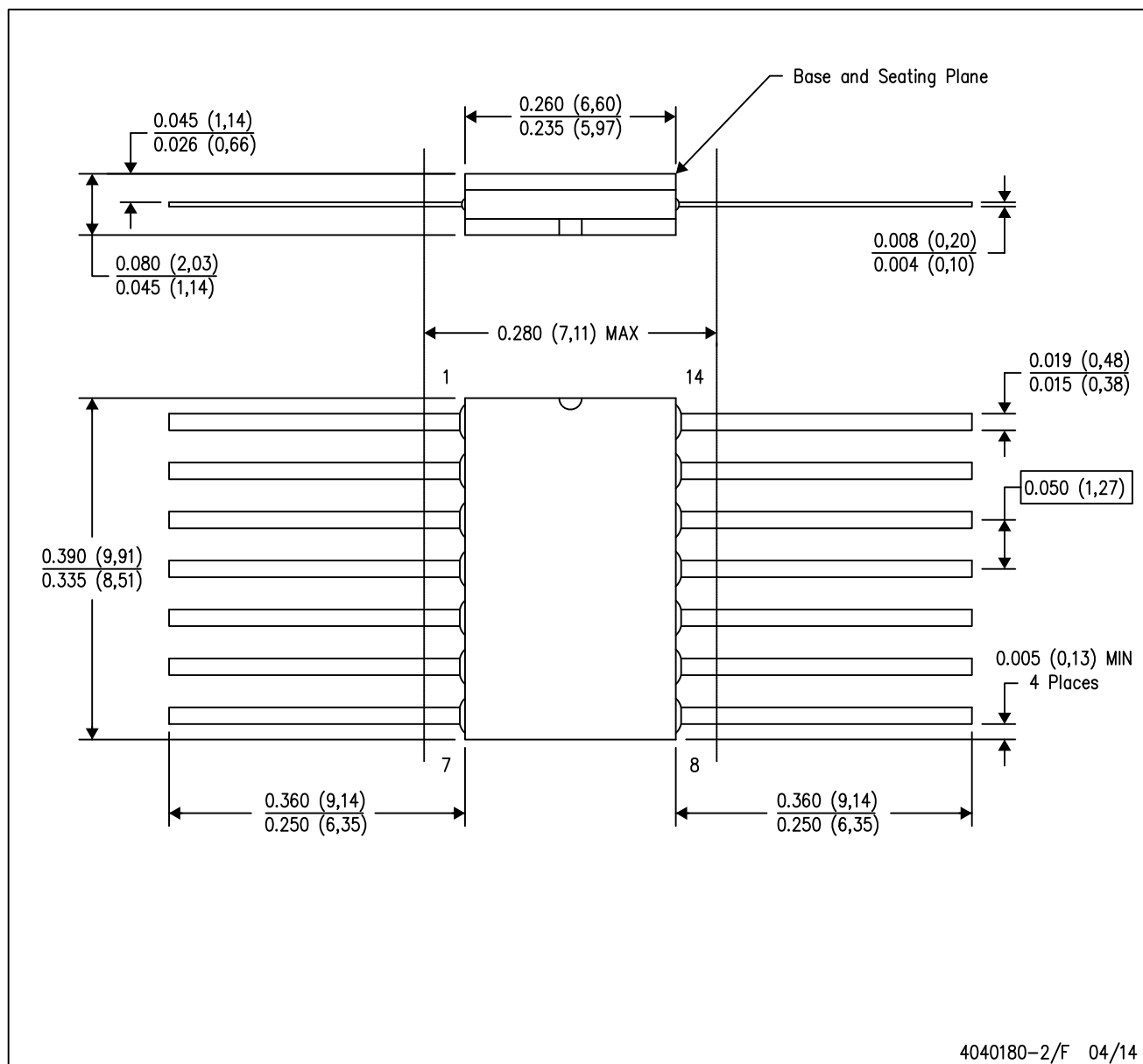
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14

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