Noritake itron

RoHS 2002/95/EC

VACUUM FLUORESCENT DISPLAY

MODULE

SPECIFICATION

MODEL: CU40045-UW1J

REVISION: F-1

SPECIFICATION NO. : DS-1439-0000-01

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This product complies with RoHS Directive 2002/95/EC

1. General Description

1.1 Application: Readout of computer, micro-computer, communication terminal and automatic instruments.

1.2 Construction: Single board display module consists of 160 characters (4 x 40) VFD, two controllers which includes character generator ROM, RAM and DC/DC converter.

1.3 Scope: The module can be connected to the CPU bus directly. +5V single power supply is required.

1.4 Weight: About 140 g

2. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Power Supply Voltage	VCC	0	—	5.5	VDC	—
Logic Input Voltage	VI	0	—	VCC+0.3	VDC	—

3. Electrical Ratings

Measuring Conditions : TA (Ambient temperature)=25 degree

Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Input Voltage	"H"	VIH	2.0	–	VCC	VDC	VCC – VSS = 5.0V
	"L"	VIL	VSS	–	0.8		
Power supply Voltage		VCC-VSS	4.75	5.00	5.25	VDC	–

4. Electrical Characteristics

Measuring Conditions: TA (Ambient temperature)=25degree, Vcc=5.0VDC

Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Output Voltage	"H"	VOH	VCC-0.8	_	–	VDC	IOH = -4 mA
	"L"	VOL	–	_	0.6		IOL = 4 mA
	"H"	VOH	VCC-0.5	_	–	VDC	IOH = -2 mA
	"L"	VOL	–	_	0.5		IOL = 2 mA
Power Supply Current 1		ICC1	–	520	680	mA	Display ON
Power Supply Current 2		ICC2	–	20	30	mA	Display OFF
Power Consumption			–	2.6	3.4	W	Display ON

Note: ICC shows the current, when all dots are turned on.
Slow rise up power supply may cause a failure of Power-on reset which is explained in "10.2 Power-on reset". Less than 50 ms power rising time is recommended.
ICC might be anticipated twice as usual at power on rush.

5. Optical Characteristics

Number of characters	:	160 (4 lines x 40 chars)
Matrix format	:	5 x 7 dot with underline
Display area	:	137.35 x 23.16mm (X x Y)
Character size	:	2.07 x 4.89 mm (X x Y)
Character pitch	:	3.47 mm
Line pitch	:	6.09 mm
Dot size	:	0.29 x 0.48mm (X x Y)
Dot pitch	:	0.44 x 0.63mm (X x Y)
Luminance	:	350 cd/m^2 (100fL) Min. (1000 cd/m^2 Typ.)
Color of illumination	:	Green (Blue-green)

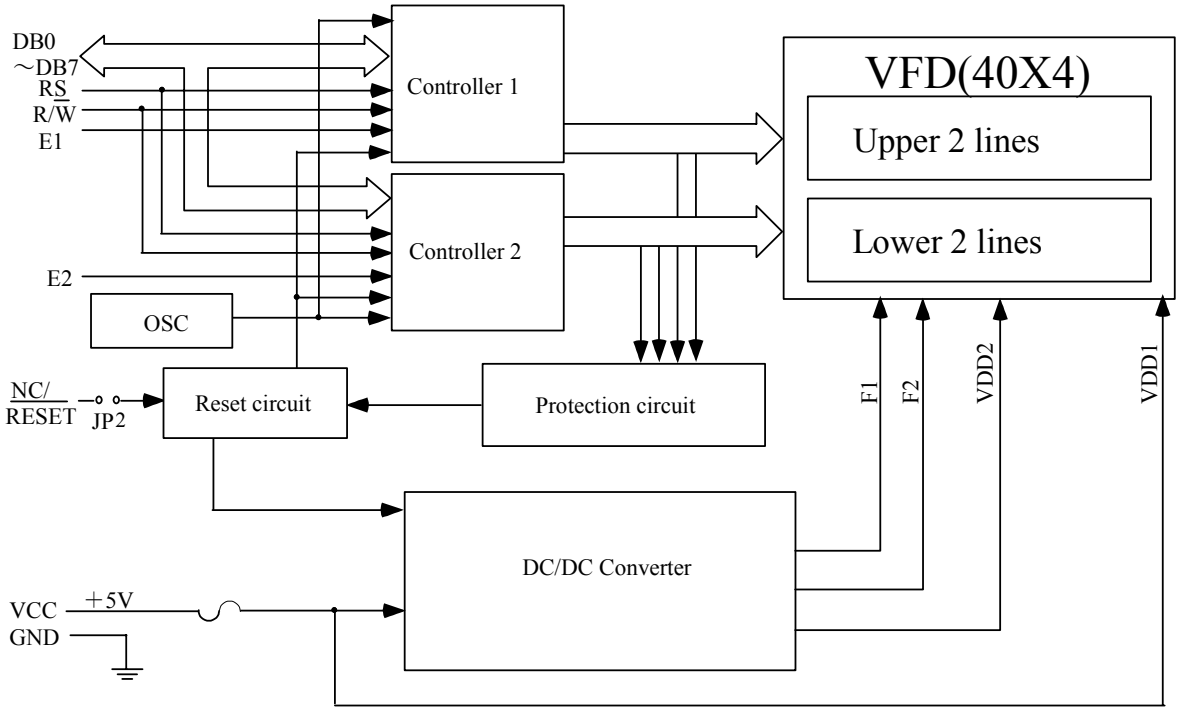
6. Environmental Conditions

Operating temperature	:	-40 to +85 degree
Storage temperature	:	-50 to +85 degree
Operating humidity	:	20 to 80 % RH (Non condensation)
Vibration(Non operation)	:	10 to 55 to 10 Hz (Frequency), 1.0 mm (Total Amplitude) 30 Min. (Duration) X, Y, Z each direction
Shock (Non operation)	:	539 m/S^2, 10mS

7. Terminal function

Signal name	No. of Lines	Input/ Output	Connected to	Function
DB4~DB7	4	Input/ Output	MPU	4 lines of high order data bus. Bi-directional transfer of data between MPU and module is done through these lines. Also DB7 can be used as a busy flag. These lines are used as data in 4 bit operation.
DB0~DB3	4	Input/ Output	MPU	4 lines of low order data bus. Bi-directional transfer of data between MPU and module is done through these lines. In 4 bit operation, these are not used and should be grounded.
E1	1	Input	MPU	Enable1-Operation start signal for data Read/Write of upper 2 lines.(Controller 1)
E2	1	Input	MPU	Enable2-Operation start signal for data Read/Write of lower 2 lines.(Controller 2)
R/$\overline{W}$	1	Input	MPU	Signal to select Read or Write. "0": Write "1": Read
RS	1	Input	MPU	Register Select. "0": Instruction register (Write) : Busy flag; Address counter (Read) "1": Data register (Write, Read)
VCC	1	-	Power Supply	+5V
GND	1	-	Power Supply	0V(GND)

8. Block Diagram



Upper 2 lines are controlled by Controller 1 with E1 signal, and Lower 2 lines are controlled by Controller 2 with E2 signal.

9. Functional Descriptions

9.1 Instruction table

Instruction	CODE										Cycle Time	Description
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display clear	0	0	0	0	0	0	0	0	0	1	100 μs Max.	Clears all display and sets DD RAM address 0 in the address counter.
Cursor home	0	0	0	0	0	0	0	0	1	*	666 ns	Sets DD RAM address 0 in the address counter. Also returns the display being shifted to the original position. DD RAM contents remain unchanged.
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	666 ns	Sets the cursor direction and specifies display shift. These operations are performed during writing/reading data.
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	666 ns	Sets all display ON/OFF(D),cursor ON/OFF(C),cursor blink of character position (B).
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	*	*	666 ns	Shifts display or cursor, keeping DD RAM contents.
Function set	0	0	0	0	1	IF	*	*	*	*	666 ns	Sets data length (IF).
Bright-ness control	1	0	*	*	*	*	*	*	BR1	BR0	666 ns	Accepts 1 byte data of just after "Function set" as brightness control data.

Instruction	CODE										Cycle Time	Description
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
CG RAM address setting	0	0	0	1	ACG						666 ns	Sets the CG RAM address.
DD RAM address setting	0	0	1	ADD							666 ns	Sets the DD RAM address.
Busy flag & address reading	0	1	BF	ACC							666 ns	Reads busy flag (BF) and address counter.
Data writing to CG or DD RAM	1	0	Data writing								666 ns	Writes data into CG RAM or DD RAM.
Data reading from CG or DD RAM	1	1	Data reading								666 ns	Reads data from CG RAM or DD RAM.
	I/D = 1 : Increment I/D = 0 : Decrement S = 1 : Display shift enabled S = 0 : Cursor shift enabled S/C = 1 : Display shift S/C = 0 : Cursor move R/L = 1 : Shift to the right R/L = 0 : Shift to the left BR1,BR0 = 00 : 100% 01 : 75% 10 : 50% 11 : 25% IF = 1 : 8-bits IF = 0 : 4-bits BF = 1 : Busy BF = 0 : Not busy												DD RAM: Display Data RAM CG RAM: Character Generator RAM ACG: CG RAM Address ADD: DD RAM Address ACC: Address Counter

Note:

* : don't care

9.2 Display Clear

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	01H

RS=0

This instruction
1. Fills all locations in the display data (DD) RAM with 20H (Blank character).
2. Clears the contents of the address counter to 0H.
3. Sets the display for zero character shift.
4. Sets the address counter to point to the DD RAM.
5. If the cursor is displayed, the cursor moves to the left most character in the top line (line 1).
6. Sets the address counter to increment on each access of DD RAM or CG RAM.

9.3 Cursor Home

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	1	*	02H to 03H

RS=0

*: don't care

This instruction
1. Clears the contents of the address counter to 0H.
2. Sets the address counter to point to the DDRAM.
3. Sets the display for zero character shift.
4. If the cursor is displayed, moves the left most character in the top line (line 1).

9.4 Entry Mode Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	1	I/D	S	04H to 07H

RS=0

The I/D bit selects the way in which the contents of the address counter are modified after every access to DDRAM or CGRAM.
I/D=1: The address counter is increment.
I/D=0: The address counter is decrement.

The S bit enables display shifts instead of cursor shift, after each write or read to the DDRAM.
S=1: Display shift enabled.
S=0: Cursor shift enabled.

The direction in which the display is shifted is opposite in sense to that of the cursor. For example if S=0 and I/D=1, the cursor would shift one character to the right after a CPU writes to DD RAM. However if S=1 and I/D=1, the display would shift one character to the left and the cursor would maintain its position on the panel.

The cursor will already be shifted in the direction selected by I/D during reads of the DD RAM, irrespective of the value of S. Similarly reading and writing the CG RAM always shifts the cursor. Also both lines are shifted simultaneously.

Cursor move and Display shift by the "Entry Mode Set"

I/D	S	After writing DD RAM data	After reading DD RAM data
0	0	The cursor moves one character to the left.	The cursor moves one character to the left.
1	0	The cursor moves one character to the right.	The cursor moves one character to the right.
0	1	The display shifts one character to the right without cursor's move.	The cursor moves one character to the left.
1	1	The display shifts one character to the left without cursor's move.	The cursor moves one character to the right.

9.5 Display ON/OFF

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	D	C	B	08H to 0FH

RS=0

This instruction controls various features of the display.
The D bit turns the entire display on or off.
D＝1: Display on
D＝0: Display off

Note: Power supply can be OFF as for power saving by using this command. Display ON or OFF and Power Supply OFF are applied by combinations of command for Controller 1 and 2 as follows.

Display ON/OFF		Display	Power Supply
Controller1	Controller2		
0	1	Upper 2lines OFF	ON
1	0	All Dot OFF	ON
0	0	All Dot OFF	OFF

The C bit turns the cursor on or off.
C=1: Cursor on
C=0: Cursor off

The B bit enables blinking of the character the cursor coincides with.
B=1: Blinking on
B=0: Blinking off

Blinking is achieved by alternating between a normal and all on display of a character.
The cursor blinks with a frequency of about 0.6 Hz and DUTY 50%.

9.6 Cursor/Display Shift

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	S/C	R/L	*	*	10H to 1FH

RS=0

*: don't care

This instruction shifts the display and/or moves the cursor, on character to either left or right, without neither reading nor writing DD RAM.
The S/C bit selects movement of the cursor or movement of both the cursor and the display.
S/C=1: Shift both cursor and display.
S/C=0: Shift cursor only.

The R/L bit selects left ward or right ward movement of the display and/or cursor.
R/L=1: Shift one character right.
R/L=0: Shift one character left.

Cursor move and Display shift by the "Cursor/Display Shift"

S/C	R/L	Cursor shift	Display shift
0	0	Move one character to the left	No shift
0	1	Move one character to the right	No shift
1	0	Shift one character to left with display	Shift one character to the left
1	1	Shift one character to right with display	Shift one character to the right

9.7 Function Set

This command sets width of data bus line by itself, and sets screen brightness by following one byte data.

9.7.1 Function Set Command

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	IF	*	*	*	*	20H to 3FH

RS=0

*: don't care

This instruction initializes the system, and must be the first instruction executed after power-on.
The IF bit selects between an 8-bit or a 4-bit bus width interface.

IF=1: 8-bit CPU interface using DB7 to DB0
IF=0: 4-bit CPU interface using DB7 to DB4

9.7.2 Brightness Control

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	*	*	*	*	*	BR1	BR0	00H to 03H

RS=1

*: don't care

One byte data (RS=1) which follows the "Function Set Command" is considered as brightness data. When a command (RS=0) is written after the "Function Set Command", the brightness control function is not initiated. Screen brightness is as follows.

BR1	BR0	Brightness
0	0	100 % (Default)
0	1	75 %
1	0	50 %
1	1	25 %

Note: Brightness level of upper and lower 2lines will be different depending on combinations of command for Controller 1 and 2.

Example:

Brightness Set		Brightness level	
Controller 1	Controller 2	Upper 2lines	Lower 2lines
75%	75%	75%	75%
75%	50%	50%	50%
50%	75%	50%	75%

9.8 Set CG RAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	ACG						40H to 7FH

RS=0

This instruction

1. Loads a new 6-bit address into the address counter.
2. Sets the address counter to address CG RAM.

Once "Set CG RAM Address" has been executed, the contents of the address counter will be automatically modified after every access of CG RAM, as determined by the "9.4 Entry Mode Set" instruction. The active width of the address counter, when it is addressing CG RAM, is 6-bits so the counter will wrap around to 00H from 3FH if more than 64 bytes of data are written to CG RAM.

9.9 Set DD RAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	ADD						

RS=0

80H to A7H (1 line), C0H to E7H (2 line)

This instruction
1. Loads a new 7-bit address into the address counter.
2. Sets the address counter to point to the DD RAM.

Once the "Set DD RAM Address" instruction has been executed, the contents of the address counter will be automatically modified after each access of DD RAM, as selected by the "9.4 Entry Mode Set" instruction.
Displays operate as two separate 40 character x 2 line displays.

Valid DD RAM Address Ranges

	Number of Characters	ADR	
1st line	40	00H to 27H	Upper half Display
2nd line	40	40H to 67H	
3rd line	40	00H to 27H	Lower half Display
4th line	40	40H to 67H	

9.10 Write Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
DATA WRITE								00H to FFH

RS=1

This instruction writes the data in DB7 to DB0 into either the CG RAM or the DD RAM. The RAM space (CG or DD), and the address in that space, that is accessed depends on whether a "Set CG RAM Address" or a "Set DD RAM Address" instruction was last executed, and on the parameters of that instruction. The contents of the address counter will be automatically modified after each "Write Data", as determined by the "9.4 Entry Mode Set". When data is written to the CG RAM, the DB7, DB6 and DB5 bits are not displayed as characters.

9.11 Read Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DATA READ							

RS=1

This instruction reads data from either CG RAM or DD RAM, depending on the type of "Set RAM Address" instructions last sent. The address in that space depends on the "Set RAM Address" instruction parameters. Immediately before executing "Read Data", "Set CG RAM Address" or "Set DD RAM Address" must be executed. The contents of the address counter are modified after each "Read Data". As determined by the "9.4 Entry Mode Set". Display shift is not executed, as described at of the "9.4 Entry Mode Set".

9.12 Read Busy Flag/Address Counter

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BF	ACC						

RS=0

Reading the instruction register yields the current value of the address counter and the busy flag. This instruction must be executed prior to any other instructions. ACC, the address counter value, will point to a location in either CG RAM or DD RAM, depending on the type of "Set RAM Address" instruction last sent.
In "Busy Flag Check" immediately after executing "Write Data" instruction, a valid address counter value can be ready as soon as BF goes low. The BF bit shows the status of the busy flag.

BF=1: busy.
BF=0: ready for next instruction, command receivable.

10.Other features

10.1 CG RAM

The display module equips CG RAM as user's are 320 bit = (5x8 bit /char) x 8 chars of store user definable character fonts. The character fonts consists of 5 x 7 dots with underline. The number 1~36 corresponds to character fonts.

Character code	CG RAM address						CG RAM data (character pattern)							
	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
00H or (08H)	0	0	0	0	0	0	*	*	*	1	2	3	4	5
	0	0	0	0	0	1	*	*	*	6	7	8	9	10
	0	0	0	0	1	0	*	*	*	11	12	13	14	15
	0	0	0	0	1	1	*	*	*	16	17	18	19	20
	0	0	0	1	0	0	*	*	*	21	22	23	24	25
	0	0	0	1	0	1	*	*	*	26	27	28	29	30
	0	0	0	1	1	0	*	*	*	31	32	33	34	35
	0	0	0	1	1	1	*	*	*	0	0	36	0	0
01H or (09H)	0	0	1	0	0	0	*	*	*	1	2	3	4	5
	0	0	1	0	0	1	*	*	*	6	7	8	9	10
	0	0	1	0	1	0	*	*	*	11	12	13	14	15
	0	0	1	0	1	1	*	*	*	16	17	18	19	20
	0	0	1	1	0	0	*	*	*	21	22	23	24	25
	0	0	1	1	0	1	*	*	*	26	27	28	29	30
	0	0	1	1	1	0	*	*	*	31	32	33	34	35
	0	0	1	1	1	1	*	*	*	0	0	36	0	0

REMARKS; "*": Don't care "0": Turned off "1": Turned on.

Dot assignment

1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25
26	27	28	29	30
31	32	33	34	35
36				

Dot 36 is for underline.

10.2 Power-on reset

Internal status of the module is initialized, when the controller detects the rising of power supply up. The status are as follows:

1. Display clear
   Fills the DD RAM with 20Hex (Space code).
   During executing of "Display Clear" (Max 100 μs), the busy flag(BF) is "1".

2. Sets the address counter to 0H.
   Sets the address counter to point the DD RAM.

3. Display ON/OFF
   D=0: Display OFF
   C=0: Cursor OFF
   B=0: Blink OFF

4. Entry Mode Set
   I/D=1 : Increment(+1)
   S=0 : No display shift

5. Function Set
   IF=1: 8-bit interface

6. Brightness Control
   BR0=BR1=0: 100%

Remarks
There is a possibility that reset doesn't work by slow start power supply causes.
Therefore the initializing by commands needed.

10.3 CPU interface

The display module is capable to communicate with M68 bus systems such as 8-bit or 4-bit data. The module is able to connected to bus of M68 type CPU.

10.3.1 4-Bit CPU interface

If 4-bit interface is used, the 8-bit instruction is written nibble by nibble: the high-order nibble being written first, followed by low-order nibble. It is not necessary to check the busy flag between writing separate nibbles of individual instructions.

See "9.7.1 Function Set Command" for more information.

10.4 Jumper

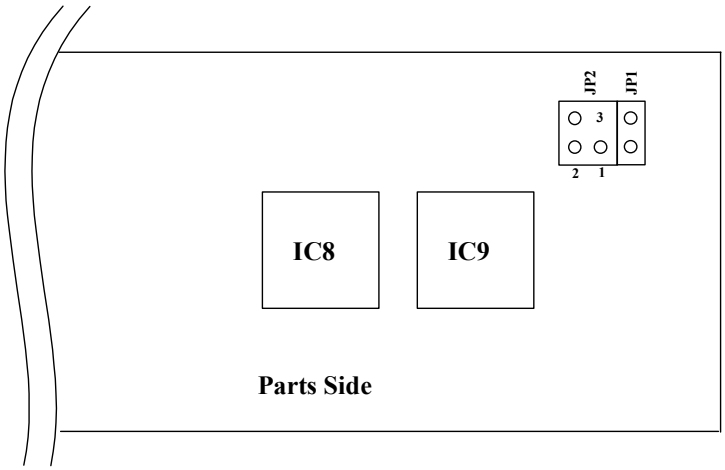
Some jumpers are prepared on the PCB board, to set operating mode of the display module. A soldering iron is required to short jumper.

No2 and No3 of jumper 'JP2' is used to reset of module.

You can reset the module by shorting No2 and No3 of the jumper 'JP2' for some interval which is longer than 10us.

The following figure shows the location of each jumper.

Location



The following table shows the function of No 1 and No 2 of JP2.

CU40045-UW1J is no reset inputs from 12th hole of 16 through holes and M68 CPU bus interface. Reset input signal is active when it is low.

Table of No 1 and No 2 of JP2 setting

No 1 and No 2 of JP2	No 12 of CN1
Open	NC
short	$\overline{\text{RESET}}$

NC: no connection

JP1 is for factory use only.

11.Character Font

D3 D2 D1 D0	D7 D6 D5 D4	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 0 0	0																
0 0 0 1	1																
0 0 1 0	2																
0 0 1 1	3																
0 1 0 0	4																
0 1 0 1	5																
0 1 1 0	6																
0 1 1 1	7																
1 0 0 0	8																
1 0 0 1	9																
1 0 1 0	A																
1 0 1 1	B																
1 1 0 0	C																
1 1 0 1	D																
1 1 1 0	E																
1 1 1 1	F																

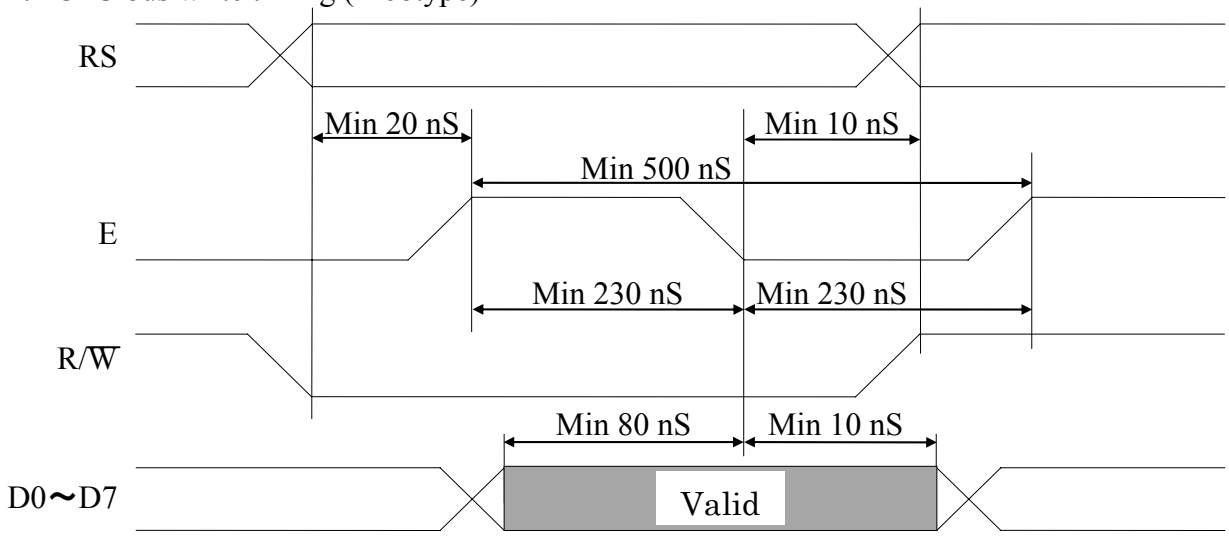
Font: G57131.cg

Note: Font number 00-07Hex (08-0FHex) is User Definable Character Fonts.

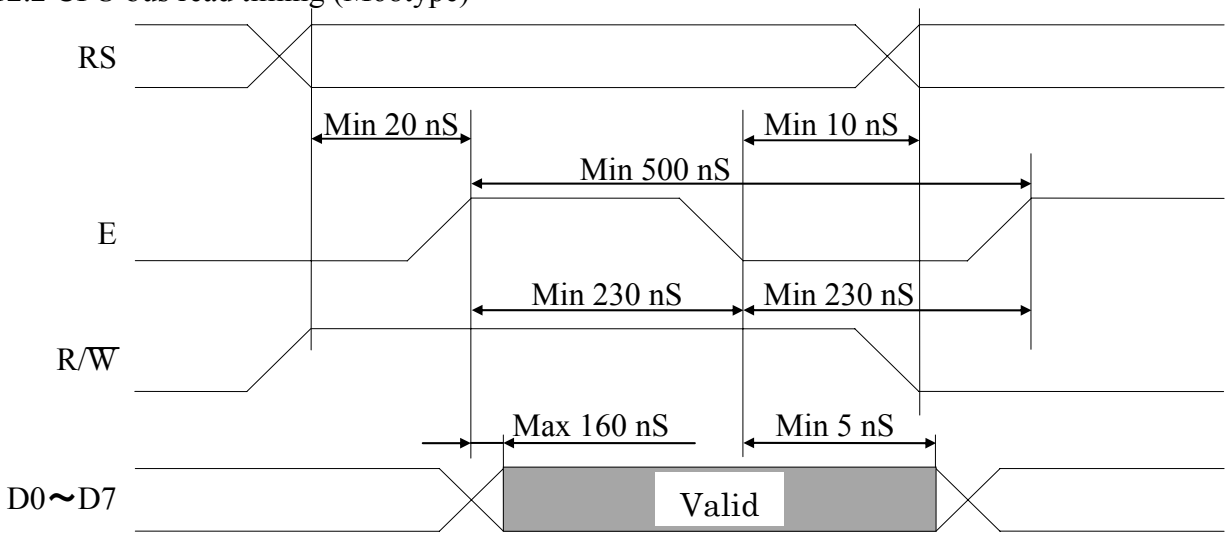
12.Timing

Input signal rise time and fall time < 15 ns.

12.1 CPU bus write timing (M68type)



12.2 CPU bus read timing (M68type)



13. Connector Pin assignment

13.1 16pin Connector (CN1)

Sixteen (16) of through holes (CN1) are prepared for power supply and data communications.
A connector or pins may be able to solder to the holes.

No.	Terminal	No.	Terminal
1	DB7	9	E1
2	DB6	10	R/W
3	DB5	11	RS
4	DB4	12	NC *)
5	DB3	13	GND
6	DB2	14	Vcc
7	DB1	15	E2
8	DB0	16	NC

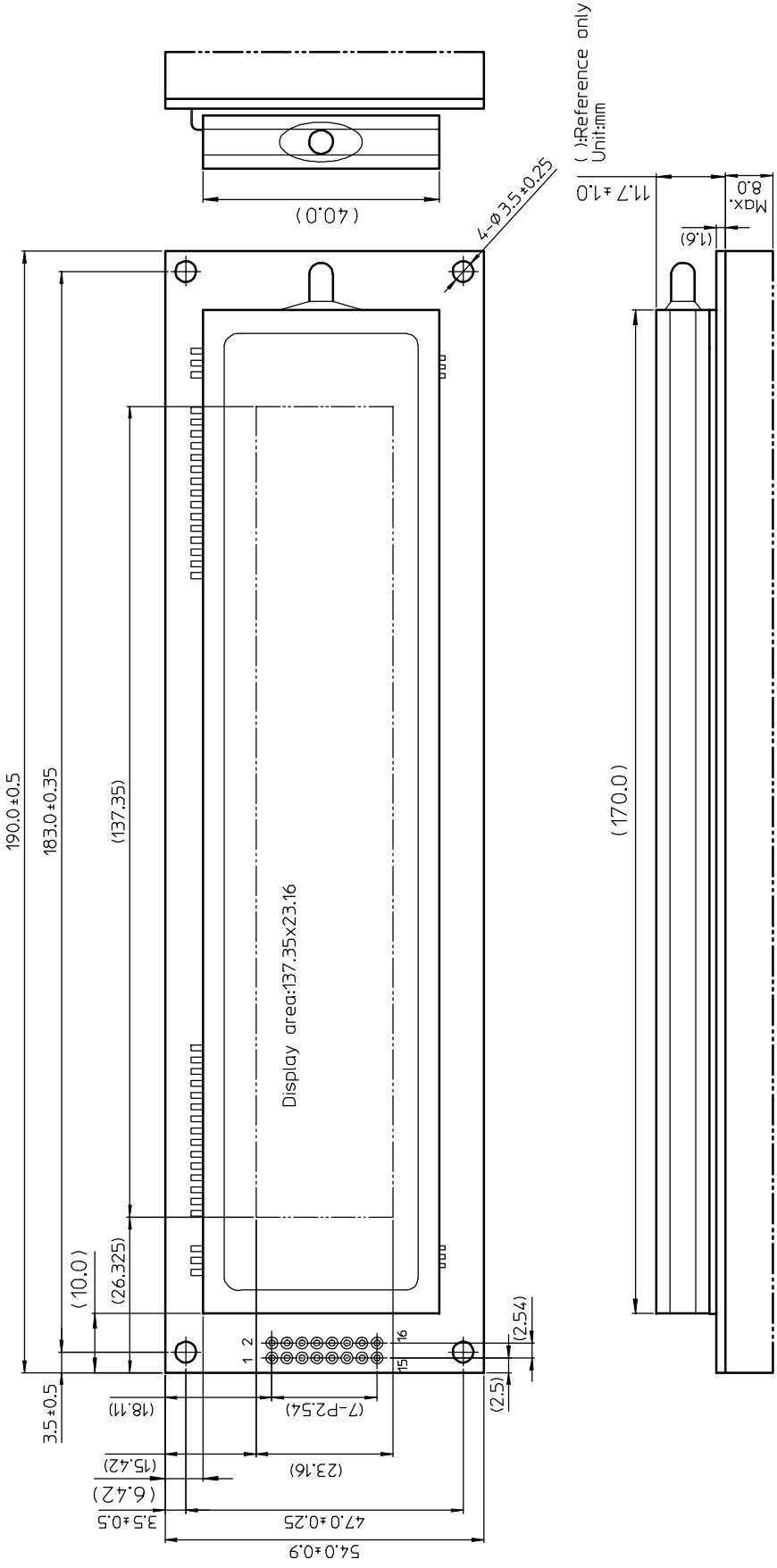
NC: no connection

Location and dimensions (Diameter of holes is 1.0mm)
The No.12 through hole is for reset input when No 1 and No 2 of JP2 are short.

13.2 3pin Connector (CN2)

A three (3) pin connector on the board is factory use only, and may be removed in future.

14. Outline dimension



Notice for the Cautious Handling VFD Modules

Handling and Usage Precautions:
Please carefully follow the appropriate product application notes for proper usage, safety handling, and operation standards for maximum performance.

[VFD tubes are made of glass]
- Because the edges of the VFD glass-envelop are not smooth, it is necessary to handle carefully to avoid injuries to your hands
- Please avoid breaking the VFD glass-envelop to prevent injury from sharp glass particles.
- The tip of the exhaust pipe is fragile so avoid shock from impact.
- It is recommended to allow sufficient open space surrounding the exhaust pipe to avoid possible damage.
- Please design the PCB for the VFD-module within 0.3 mm warping tolerance to avoid any forces that may damage the display due to PCB distortion causing a breakdown of the electrical circuit leading to VFD failure.

[High voltage]
- Avoid touching conductive electrical parts, because the VFD-module uses high voltage exceeding 30～100 volts.
- Even when electric power is turned off, it may take more than one minute for the electrical current to discharge.

[Cable connection]
- Do not unplug the power and/or data cables of VFD-modules during operating condition because unrecoverable damage may result.
- Sending input signals to the VFD-module during a power off condition sometimes causes I/O port damage.
- It is recommended to use a 30 cm or shorter signal cable to prevent functional failures.

[Electrostatic charge]
- VFD-modules needs electrostatic free packaging and protection from electrostatic charges during handling and usage.

[Structure]
- During operation, VFD and VFD-modules generate heat. Please consider sufficient heat radiation dissipation using heat sink solutions.
- We prefer to use UL grade materials or components in conjunction with VFD-modules.
- Wrap and twist motion causes stress and may break VFDs & VFD modules. Please adhere to allowances within 0.3mm at the point of attachment.

[Power]
- Apply regulated power to the VFD-module within specified voltages to protect from failures.
- Because some VFD-modules may consume in rush current equal to twice the typical current at power-on timing, we recommend using a sufficient power capability and quick starting of the power regulator.
- VFD-module needs a specified voltage at the point of connection. Please use an adequate power cable to avoid a decrease in voltage. We also recommend inserting a power fuse for extra protection.

[Operating consideration]
- Illuminating phosphor will decrease in brightness during extended operation. If a fixed pattern illuminates for an extended period,(several hours), the phosphor efficiency will decrease compared to the non operating phosphor causing a non uniform brightness among pixels. Please consider programming the display patterns to use all phosphor segments evenly. Scrolling may be a consideration for a period of time to refresh the phosphor condition and improve even illumination to the pixels.
- We recommend using a signal cable 30cm or less to avoid some possible disturbances to the signal.

[Storage and operating environment]
- Please use VFD-modules under the recommended specified environmental conditions. Salty, sulfur and dusty environments may damage the VFD-module even during storage.

[Discard]
- Some VFDs contain a small amount of cadmium in the phosphor and lead in the solder. When discarding VFDs or VFD-modules, please adhere to governmental related laws or regulations.

[Others]
- Although the VFD-module is designed to be protected from electrical noise, please plan your circuitry to exclude as much noise as possible.
- Do not reconstruct or repair the VFD-module without our authorization. We cannot assure the quality or reliability of unauthorized reconstructed VFD-modules.

Notice:
- We do not authorize the use of any patents that may be inherent in these specifications.
- Neither whole nor partial copying of these specifications are permitted without our approval. If necessary , please ask for assistance from our sales consultant.
- This product is not designed for military, aerospace, medical or other life-critical applications. If you choose to use this product for these applications, please ask us for prior consultation or we cannot take responsibility for problems that may occur.