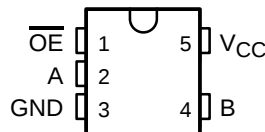


- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DBV OR DCK PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT1G125 features a single high-speed line switch. The switch is disabled when the output-enable ($\overline{OE}$) input is high.

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING [‡]
–40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74CBT1G125DBVR	S25_
		Reel of 250	SN74CBT1G125DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74CBT1G125DCKR	SM_
		Reel of 250	SN74CBT1G125DCKT	

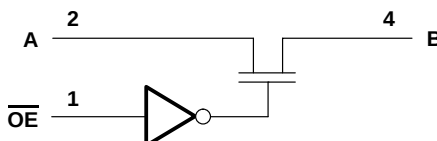
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

[‡] The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN74CBT1G125

SINGLE FET BUS SWITCH

SCDS046G – FEBRUARY 1998 – REVISED JANUARY 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4	5.5	V
V_{IH} High-level control input voltage	2		V
V_{IL} Low-level control input voltage		0.8	V
T_A Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
I_I	$V_{CC} = 5.5$ V, $V_I = 5.5$ V or GND			±1	µA
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND			1	µA
C_i Control input	$V_I = 3$ V or 0			3	pF
$C_{io(OFF)}$	$V_O = 3$ V or 0, $\overline{OE} = V_{CC}$			4	pF
r_{on}^S	$V_{CC} = 4$ V, TYP at $V_{CC} = 4$ V, $V_I = 2.4$ V, $I_I = 15$ mA			14	20
	$V_{CC} = 4.5$ V	$V_I = 0$	$I_I = 64$ mA	5	7
			$I_I = 30$ mA	5	7
		$V_I = 2.4$ V, $I_I = 15$ mA		10	15

[‡] All typical values are at $V_{CC} = 5$ V (unless otherwise noted), $T_A = 25^\circ\text{C}$.

^S Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

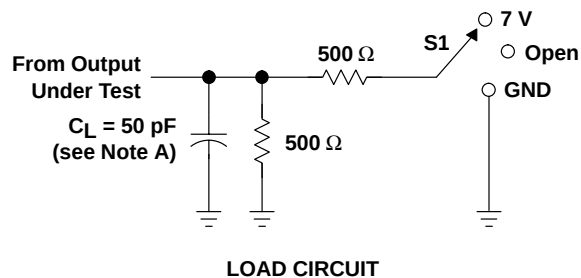
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4$ V		$V_{CC} = 5$ V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^{\dagger\dagger}$	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		5.5	1.6	4.9	ns
t_{dis}	$\overline{OE}$	A or B		4.5	1	4.2	ns

^{††} The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

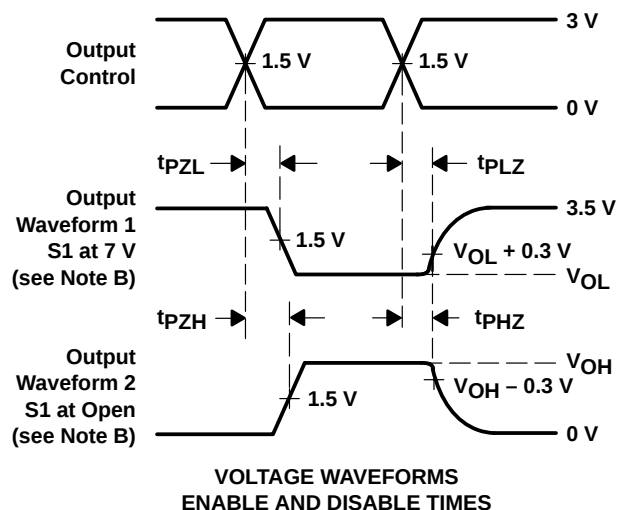
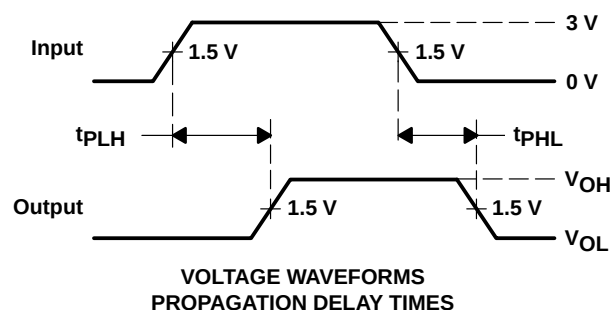


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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74CBT1G125DBVRE4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(S25G, S25S)
74CBT1G125DBVRE4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(S25G, S25S)
74CBT1G125DCKRG4	Active	Production	SC70 (DCK) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(SM3, SMS, SMU)
74CBT1G125DCKRG4.A	Active	Production	SC70 (DCK) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(SM3, SMS, SMU)
SN74CBT1G125DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(S25G, S25J, S25S)
SN74CBT1G125DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(S25G, S25J, S25S)
SN74CBT1G125DBVT	NRND	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(S25J, S25S)
SN74CBT1G125DBVT.A	NRND	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(S25J, S25S)
SN74CBT1G125DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(SM3, SMJ, SMS, SM T, SMU)
SN74CBT1G125DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(SM3, SMJ, SMS, SM T, SMU)
SN74CBT1G125DCKT	NRND	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(SM3, SMJ, SMS)
SN74CBT1G125DCKT.A	NRND	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(SM3, SMJ, SMS)

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CBT1G125DBVRE4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74CBT1G125DBVRE4	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74CBT1G125DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74CBT1G125DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74CBT1G125DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74CBT1G125DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
SN74CBT1G125DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74CBT1G125DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74CBT1G125DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74CBT1G125DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74CBT1G125DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CBT1G125DBVRE4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74CBT1G125DBVRE4	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74CBT1G125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74CBT1G125DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74CBT1G125DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74CBT1G125DCKR	SC70	DCK	5	3000	203.0	203.0	35.0
SN74CBT1G125DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74CBT1G125DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74CBT1G125DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74CBT1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74CBT1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0



SOT-23 - 1.45 mm max height

Front View:

- Overall dimensions: 3.0 x 2.6
- Pin locations: 1, 2, 3, 4, 5
- Dimensions: 1.75, 1.45, 1.9, 3.05, 2.75
- Feature table:

$\oplus$	0.2	$\odot$	C	A	B
----------	-----	---------	---	---	---
- Note: PIN 1 INDEX AREA
- Note: NOTE 5

Side View:

- Chamfer: 4X 0°-15°
- Dimension: 0.15 TYP

End View:

- Chamfer: 4X 4°-15°
- Dimension: 0.22 TYP

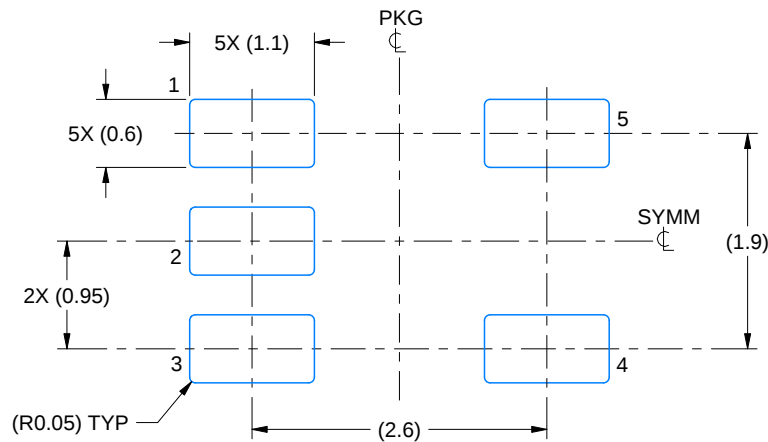
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

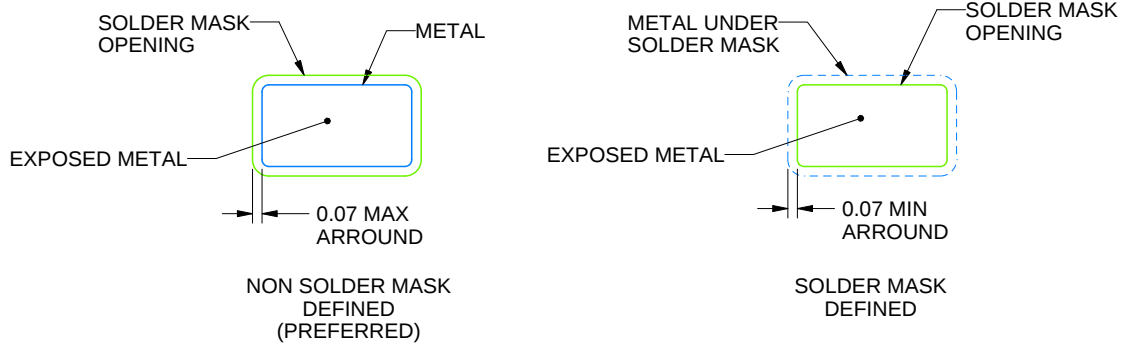
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

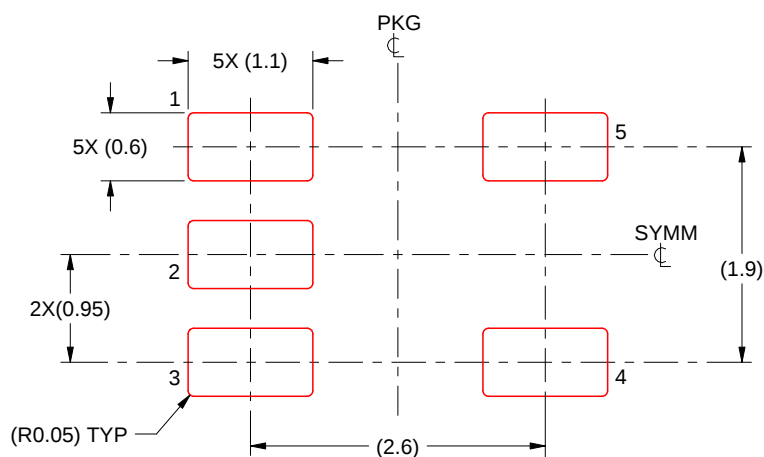
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

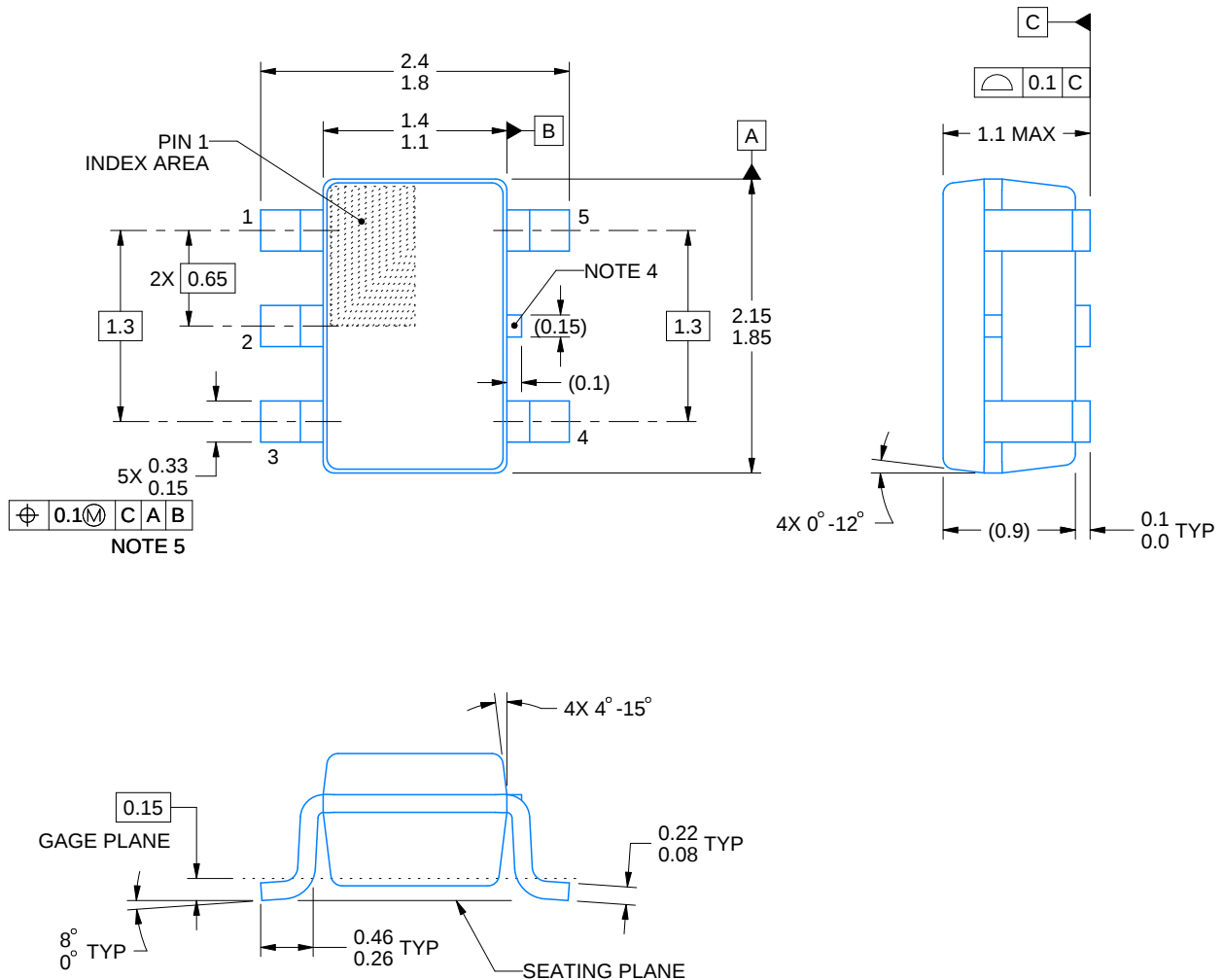


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

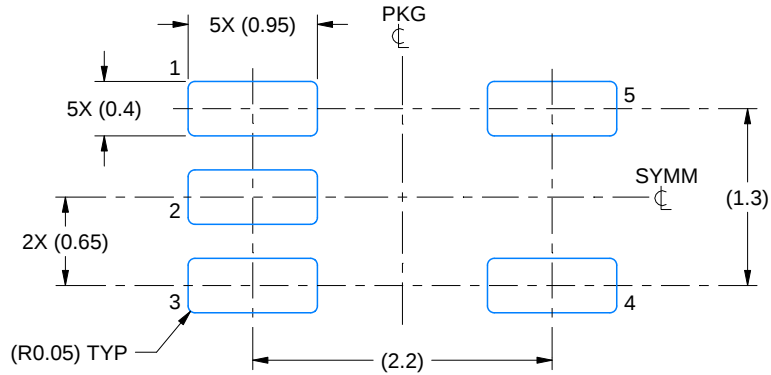
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



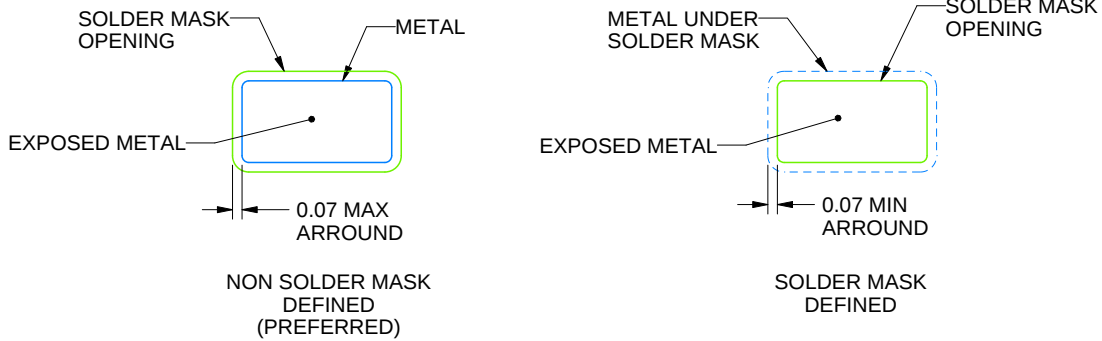
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

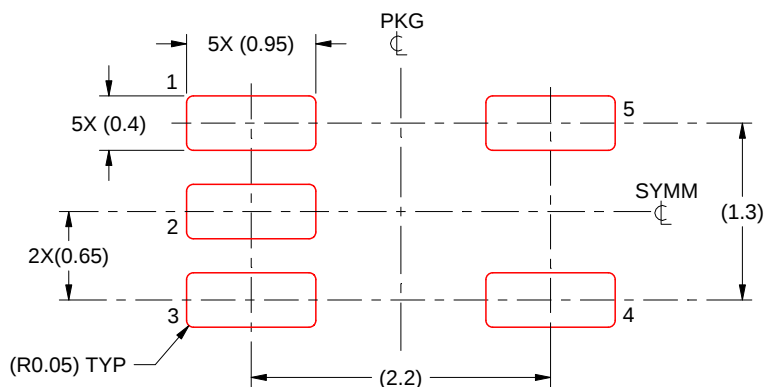


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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