SIEMENS

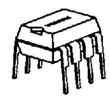
8/16 Kbit (1024/2048 × 8 bit) Serial CMOS EEPROMs, I²C Synchronous 2-Wire Bus

SLx 24C08/16

Preliminary

Features

- **Data EEPROM internally organized as 1024/2048 bytes and 64/128 pages × 16 bytes**
- **Low power CMOS**
- **V_{CC} = 2.7 to 5.5 V operation**
- **Two wire serial interface bus, I²C-Bus compatible**
- **Filtered inputs for noise suppression with Schmitt trigger**
- **Clock frequency up to 400 kHz**
- **High programming flexibility**
  - Internal programming voltage
  - Self timed programming cycle including erase
  - Byte-write and page-write programming, between 1 and 16 bytes
  - Typical programming time 6 ms (< 10 ms) for up to 16 bytes
- **High reliability**
  - Endurance 10^6 cycles[1)]
  - Data retention 40 years[1)]
  - ESD protection 4000 V on all pins
- **8 pin DIP/DSO packages**
- **Available for extended temperature ranges**
  - Industrial: – 40 °C to + 85 °C
  - Automotive: – 40°C to + 125 °C



P-DIP-8-4

P-DSO-8-3

1) Values are temperature dependent, for further information please refer to your Siemens Sales office.

Ordering Information

Type	Ordering Code	Package	Temperature	Voltage
SLA 24C08-D	Q67100-H3572	P-DIP-8-4	– 40 °C ... + 85 °C	4.5 V...5.5 V
SLA 24C08-S	Q67100-H3518	P-DSO-8-3	– 40 °C ... + 85 °C	4.5 V...5.5 V
SLA 24C08-D-3	Q67100-H3435	P-DIP-8-4	– 40 °C ... + 85 °C	2.7 V...5.5 V
SLA 24C08-S-3	Q67100-H3517	P-DSO-8-3	– 40 °C ... + 85 °C	2.7 V...5.5 V
SLE 24C08-D	Q67100-H3226	P-DIP-8-4	– 40°C ... + 125 °C	4.5 V...5.5 V
SLE 24C08-S	Q67100-H3227	P-DSO-8-3	– 40°C ... + 125 °C	4.5 V...5.5 V
SLA 24C16-D	Q67100-H3513	P-DIP-8-4	– 40 °C ... + 85 °C	4.5 V...5.5 V
SLA 24C16-S	Q67100-H3508	P-DSO-8-3	– 40 °C ... + 85 °C	4.5 V...5.5 V
SLA 24C16-D-3	Q67100-H3512	P-DIP-8-4	– 40 °C ... + 85 °C	2.7 V...5.5 V
SLA 24C16-S-3	Q67100-H3507	P-DSO-8-3	– 40 °C ... + 85 °C	2.7 V...5.5 V
SLE 24C16-D	Q67100-H3229	P-DIP-8-4	– 40°C ... + 125 °C	4.5 V...5.5 V
SLE 24C16-S	Q67100-H3230	P-DSO-8-3	– 40°C ... + 125 °C	4.5 V...5.5 V

Other types are available on request

- Temperature range (– 55 °C ... + 150 °C)
- Package (die, wafer delivery)

1 Pin Configuration

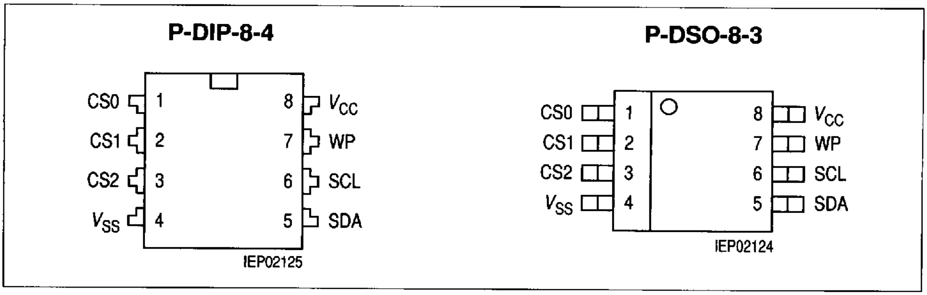


Figure 1
Pin Configuration (top view)

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Pin Definitions and Functions

Table 1

Pin No.	Symbol	Function
1, 2, 3	CS0, CS1, CS2	Chip select inputs
4	V_{SS}	Ground
5	SDA	Serial bidirectional data bus
6	SCL	Serial clock input
7	WP	Write protection input
8	V_{CC}	Supply voltage

Pin Description

Serial Clock (SCL)

The SCL input is used to clock data into the device on the rising edge and to clock data out of the device on the falling edge.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer addresses, data or control information into the device or to transfer data out of the device. The output is open drain, performing a wired AND function with any number of other open drain or open collector devices. The SDA bus requires a pull-up resistor to V_{CC}.

Chip Select (CS0, CS1, CS2)

The CS0, CS1 and CS2 pins are chip select inputs. They are not connected for this device. It is recommended to connect CS0, CS1 and CS2 either to V_{CC} or V_{SS}.

Write Protection (WP)

WP switched to V_{SS} allows normal read/write operations.

WP switched to V_{CC} protects the upper half of the EEPROM against changes (hardware write protection).

2 Description

The SLx 24C08/16 device is a serial electrically erasable and programmable read only memory (EEPROM), organized as 1024/2048 × 8 bit. The data memory is divided into 64/128 pages. The 16 bytes of a page can be programmed simultaneously.

The device conforms to the specification of the 2-wire serial I²C-Bus. Low voltage design permits operation down to 2.7 V with low active and standby currents.

The device operates at 5.0 V ± 10% with a maximum clock frequency of 400 kHz and at 2.7 ... 4.5 V with a maximum clock frequency of 100 kHz. The device is available as 5 V type (V_{CC} = 4.5 ... 5.5 V) with two temperature ranges for industrial and automotive applications and as 3 V type (V_{CC} = 2.7 ... 5.5 V) for industrial applications. The EEPROMs are mounted in eight-pin DIP and DSO packages or are also supplied as chips.

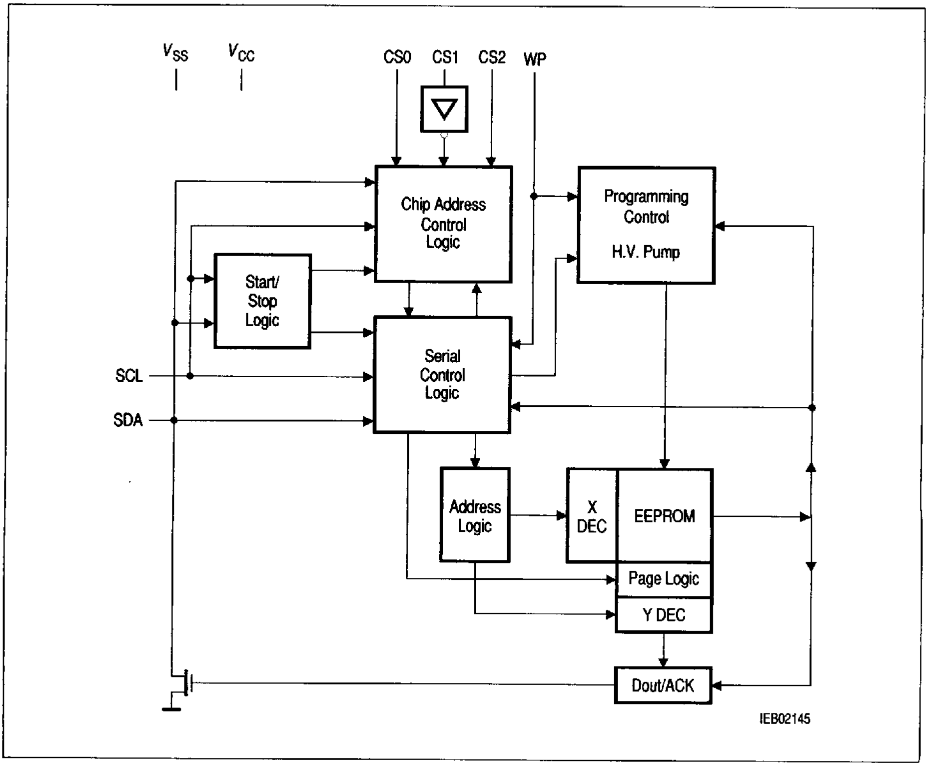

Figure 2
Block Diagram

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3 I²C-Bus Characteristics

The SLx 24C08/16 devices support a master/slave bidirectional bus oriented protocol in which the EEPROM always takes the role of a slave.

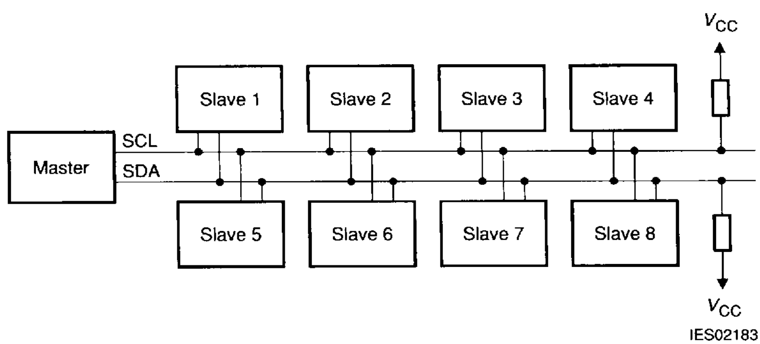

Figure 3
Bus Configuration

Master	Device that initiates the transfer of data and provides the clock for both transmit and receive operations.
Slave	Device addressed by the master, capable of receiving and transmitting data.
Transmitter	The device with the SDA as output is defined as the transmitter. Due to the open drain characteristic of the SDA output the device applying a low level wins.
Receiver	The device with the SDA as input is defined as the receiver.

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The conventions for the serial clock line and the bidirectional data line are shown in **figure 4**.

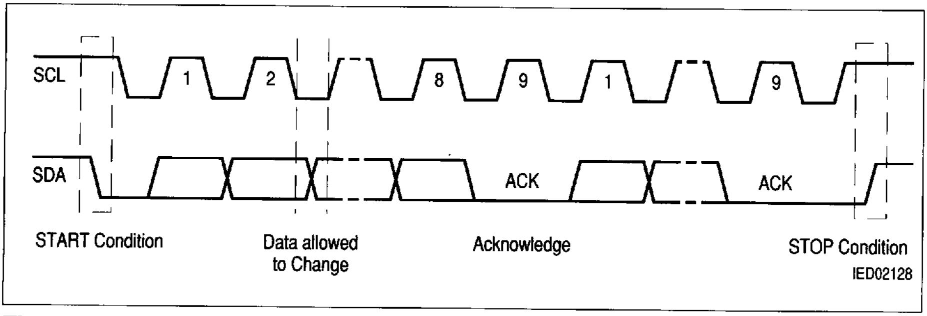

Figure 4
I²C-Bus Timing Conventions for START Condition, STOP Condition, Data Validation and Transfer of Acknowledge ACK

Standby Mode in which the bus is not busy (no serial transmission, no programming): both clock (SCL) and data line (SDA) are in high state. The device enters the standby mode after a STOP condition or after a programming cycle.

START Condition High to low transition of SDA when SCL is high, preceding all commands.

STOP Condition Low to high transition of SDA when SCL is high, terminating all communications. A STOP condition initiates an EEPROM programming cycle. A STOP condition after reading a data byte from the EEPROM initiates the Standby mode.

Acknowledge A successful reception of eight data bits is indicated by the receiver by pulling down the SDA line during the following clock cycle of SCL (ACK). The transmitter on the other hand has to release the SDA line after the transmission of eight data bits.
The EEPROM as the receiving device responds with an acknowledge, when addressed. The master, on the other side, acknowledges each data byte transmitted by the EEPROM and can at any time end a read operation by releasing the SDA line (no ACK) followed by a STOP condition.

Data Transfer Data must change only during low SCL state, data remains valid on the SDA bus during high SCL state. Nine clock pulses are required to transfer one data byte, the most significant bit (MSB) is transmitted first.

4 Device Addressing and EEPROM Addressing

After a START condition, the master always transmits a Command Byte CSW or CSR. After the acknowledge of the EEPROM a Control Byte follows, its content and the transmitter depend on the previous Command Byte. The description of the Command and Control Bytes is shown in **table 2**.

Command Byte **Selects operation:** the least significant bit b0 is low for a write operation (Chip Select Write Command Byte CSW) or set high for a read operation (Chip Select Read Command Byte CSR).

Contains address information: in the CSW Command Byte, the bit positions b2 or b3 to b1 are decoded for the two or three uppermost EEPROM address bits A9 or A10 to A8 (in the CSR Command Byte, the bit positions b3 to b1 are left undefined).

Control Byte **Following CSW (b0 = 0):** contains the eight lower bits of the EEPROM address (EEA) bit A7 to A0.

Following CSR (b0 = 1): contains the data read out, transmitted by the EEPROM. The EEPROM data are read as long as the master pulls down SDA after each byte in order to acknowledge the transfer. The read operation is stopped by the master by releasing SDA (no acknowledge is applied) followed by a STOP condition.

Table 2
Command and Control Byte for I²C-Bus Addressing of Chip and EEPROM

	Definition								Function
	b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**	
CSW	1	0	1	0	A10	A9	A8	0	Chip Select for Write
CSR	1	0	1	0	x	x	x	1	Chip Select for Read
EEA	A7	A6	A5	A4	A3	A2	A1	A0	EEPROM address

The device has an internal address counter which points to the current EEPROM address.

The address counter is incremented
- after a data byte to be written has been acknowledged, during entry of further data byte
- during a byte read, thus the address counter points to the following address after reading a data byte.

The timing conventions for read and write operations are described in **figures 5** and **6**.

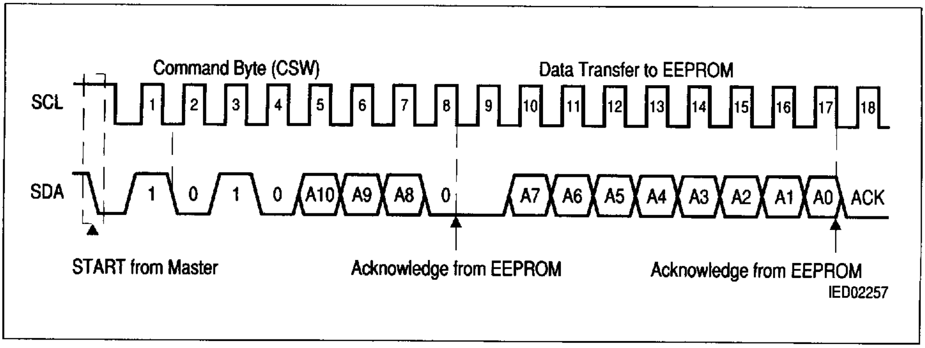

Figure 5
Timing of the Command Byte CSW

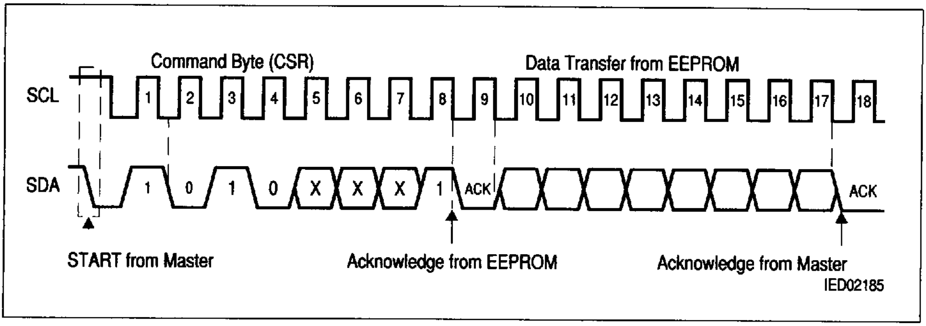

Figure 6
Timing of the Command Byte CSR

5 Write Operations

Changing of the EEPROM data is initiated by the master with the command byte CSW. Depending on the state of the Write Protection pin WP either one byte (Byte Write) or up to 16 bytes (Page Write) are modified in one programming procedure.

5.1 Byte Write

Address Setting After a START condition the master transmits the Chip Select Write byte CSW. The EEPROM acknowledges the CSW byte during the ninth clock cycle. The following byte with the EEPROM address (A0 to A7) is loaded into the address counter of the EEPROM and acknowledged by the EEPROM.

Transmission of Data Finally the master transmits the data byte which is also acknowledged by the EEPROM into the internal buffer.

Programming Cycle Then the master applies a STOP condition which starts the internal programming procedure. The data bytes are written in the memory location addressed in the EEA byte (A0 to A7) and the CSW byte (A8 to A9 or A10). The programming procedure consists of an internally timed erase/write cycle. In the first step, the selected byte is erased to “1”. With the next internal step, the addressed byte is written according to the contents of the buffer.

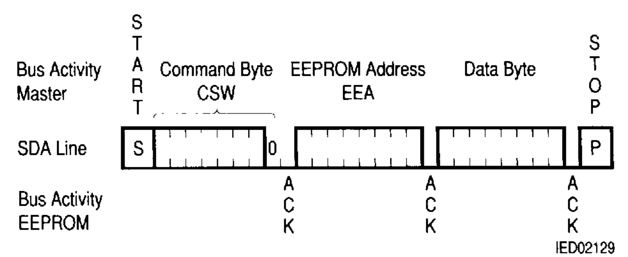

Figure 7
Byte Write Sequence

The erase/write cycle is finished latest after 10 ms. Acknowledge polling may be used for speed enhancement in order to indicate the end of the erase/write cycle (refer to **chapter 5.3** Acknowledge Polling).

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5.2 Page Write

Address Setting

The page write procedure is the same as the byte write procedure up to the first data byte. In a page write instruction however, entry of the EEPROM address byte EEA is followed by a sequence of one to maximum sixteen data bytes with the new data to be programmed. These bytes are transferred to the internal page buffer of the EEPROM.

Transmission of Data

The first entered data byte will be stored according to the EEPROM address n given by EEA (A0 to A7) and CSW (A8 to A9 or A10). The internal address counter is incremented automatically after the entered data byte has been acknowledged. The next data byte is then stored at the next higher EEPROM address. EEPROM addresses within the same page have common page address bits A4 through A10. Only the respective four least significant address bits A0 through A3 are incremented, as all data bytes to be programmed simultaneously have to be within the same page.

Programming Cycle

The master stops data entry by applying a STOP condition, which also starts the internally timed erase/write cycle. In the first step, all selected bytes are erased to “1”. With the next internal step, the addressed bytes are written according to the contents of the page buffer.

Those bytes of the page that have not been addressed are not included in the programming.

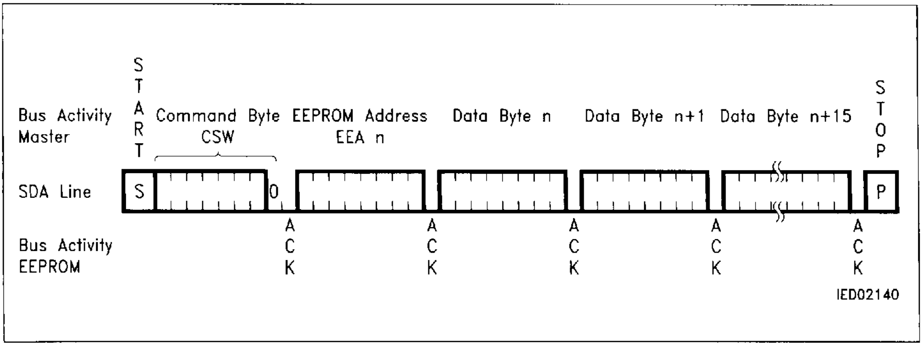

Figure 8
Page Write Sequence

The erase/write cycle is finished latest after 10 ms. Acknowledge polling may be used for speed enhancement in order to indicate the end of the erase/write cycle (refer to **chapter 5.3** Acknowledge Polling).

5.3 Acknowledge Polling

During the erase/write cycle the EEPROM will not respond to a new command byte until the internal write procedure is completed. At the end of active programming the chip returns to the standby mode and the last entered EEPROM byte remains addressed by the address counter. To determine the end of the internal erase/write cycle acknowledge polling can be initiated by the master by sending a START condition followed by a command byte CSR or CSW (read with b0 = 1 or write with b0 = 0). If the internal erase/write cycle is not completed, the device will not acknowledge the transmission. If the internal erase/write cycle is completed, the device acknowledges the received command byte and the protocol activities can continue.

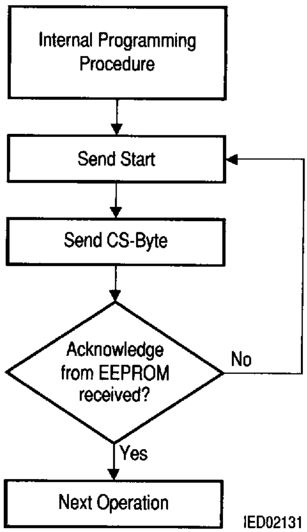

Figure 9
Flow Chart "Acknowledge Polling"

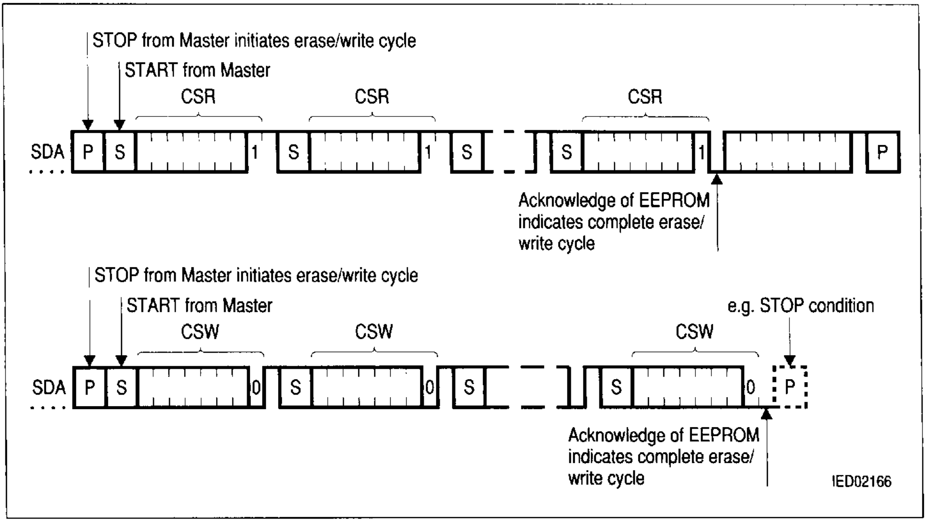

Figure 10
Principle of Acknowledge Polling

6 Read Operations

Reading of the EEPROM data is initiated by the Master with the command byte CSR.

6.1 Random Read

Random read operations allow the master to access any memory location.

Address Setting The master generates a START condition followed by the command byte CSW. The receipt of the CSW-byte is acknowledged by the EEPROM with a low on the SDA line. Now the master transmits the EEPROM address (EEA) to the EEPROM and the internal address counter is loaded with the desired address.

Transmission of CSR After the acknowledge for the EEPROM address is received, the master generates a START condition, which terminates the initiated write operation. Then the master transmits the command byte CSR for read, which is acknowledged by the EEPROM.

Transmission of EEPROM Data During the next eight clock pulses the EEPROM transmits the data byte and increments the internal address counter.

STOP Condition from Master During the following clock cycle the masters releases the bus and then transmits the STOP condition.

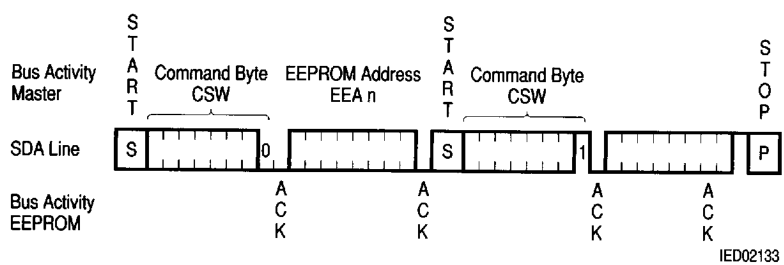

Figure 11
Random Read

6.2 Current Address Read

The EEPROM content is read without setting an EEPROM address, in this case the current content of the address counter will be used (e.g. to continue a previous read operation after the Master has served an interrupt).

Transmission of CSR For a current address read the master generates a START condition, which is followed by the command byte CSR (chip select read). The receipt of the CSR-byte is acknowledged by the EEPROM with a low on the SDA line.

Transmission of EEPROM Data During the next eight clock pulses the EEPROM transmits the data byte and increments the internal address counter.

STOP Condition from Master During the following clock cycle the masters releases the bus and then transmits the STOP condition.

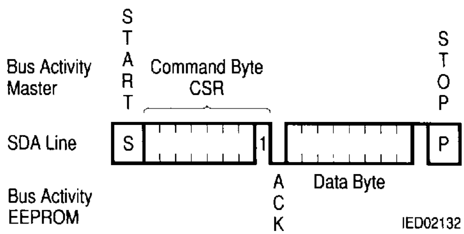

Figure 12
Current Address Read

6.3 Sequential Read

A sequential read is initiated in the same way as a current read or a random read except that the master acknowledges the data byte transmitted by the EEPROM. The EEPROM then continues the data transmission. The internal address counter is incremented by one during each data byte transmission.

A sequential read allows the entire memory to be read during one read operation. After the highest addressable memory location is reached, the internal address pointer “rolls over” to the address 0 and the sequential read continues.

The transmission is terminated by the master by releasing the SDA line (no acknowledge) and generating a STOP condition (see **figure 13**).

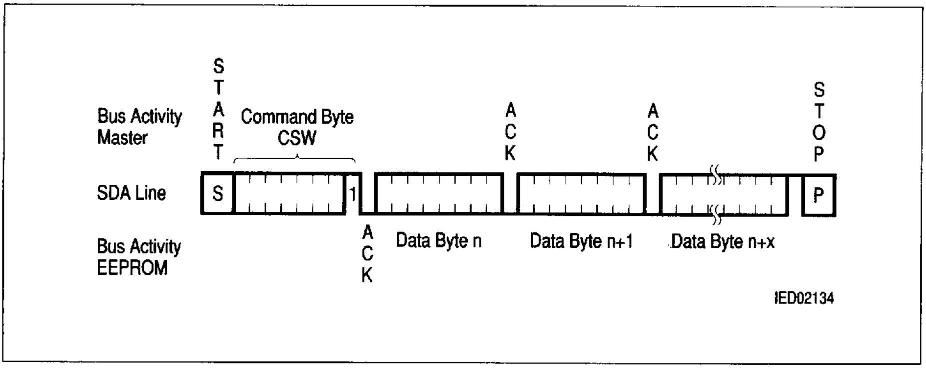

Figure 13
Sequential Read

7 Electrical Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

7.1 Absolute Maximum Ratings

Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this data sheet is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Parameter		Limit Values	Units
Operating temperature	range 1 (industrial) range 2 (automotive)	– 40 to + 85 – 40 to + 125	°C °C
Storage temperature		– 65 to + 150	°C
Supply voltage		– 0.3 to + 7.0	V
All inputs and outputs with respect to ground		– 0.3 to V_{CC} + 0.5	V
ESD protection (human body model)		4000	V

7.2 DC Characteristics

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Supply voltage	V_{CC}	4.5		5.5	V	5 V type
	V_{CC}	2.7		5.5	V	3 V type
Supply current[1)](write)	I_{CC}		1	3	mA	V_{CC} = 5 V; f_c = 100 kHz
Standby current[2)]	I_{SB}			50	µA	Inputs at V_{CC} or V_{SS}
Input leakage current	I_{LI}		0.1	10	µA	$V_{IN} = V_{CC}$ or V_{SS}
Output leakage current	I_{LO}		0.1	10	µA	$V_{OUT} = V_{CC}$ or V_{SS}
Input low voltage	V_{IL}	– 0.3		$0.3 \times V_{CC}$	V	

7.2 DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Input high voltage	V_{IH}	$0.7 \times V_{CC}$		$V_{CC} + 0.5$	V	
Output low voltage	V_{OL}			0.4	V	$I_{OL} = 3$ mA; $V_{CC} = 5$ V $I_{OL} = 2.1$ mA; $V_{CC} = 3$ V
Input/output capacitance (SDA)	$C_{I/O}$			8[3]	pF	$V_{IN} = 0$ V; $V_{CC} = 5$ V
Input capacitance (other pins)	C_{IN}			6[3]	pF	$V_{IN} = 0$ V; $V_{CC} = 5$ V

[1] The values for I_{cc} are maximum peak values
[2] Valid over the whole temperature range
[3] This parameter is characterized only

7.3 AC Characteristics

Parameter	Symbol	Limit Values V_{CC} = 2.7-5.5 V		Limit Values V_{CC} = 4.5-5.5 V		Units
		min.	max.	min.	max.	
SCL clock frequency	f_{SCL}		100		400	kHz
Clock pulse width low	t_{low}	4.7		1.2		µs
Clock pulse width high	t_{high}	4.0		0.8		µs
SDA and SCL rise time	t_R		1.0		0.25	µs
SDA and SCL fall time	t_F		0.3		0.25	µs
Start set-up time	$t_{SU.STA}$	4.7		0.6		µs
Start hold time	$t_{HD.STA}$	4.0		0.6		µs
Data in set-up time	$t_{SU.DAT}$	200		100		µs
Data in hold time	$t_{HD.DAT}$	0		0		µs
SCL low to SDA data out valid	t_{AA}	0.1	4.5	0.1	0.9	µs
Data out hold time	t_{DH}	100		50		ns
Stop set-up time	$t_{SU.STO}$	4.7		0.6		µs
Time the bus must be free before a new transmission can start	t_{BUF}	4.7		1.2		µs
SDA and SCL spike suppression time at constant inputs	t_I	50	100	50	100	ns
Erase/write cycle	t_{WR}		10		10	ms

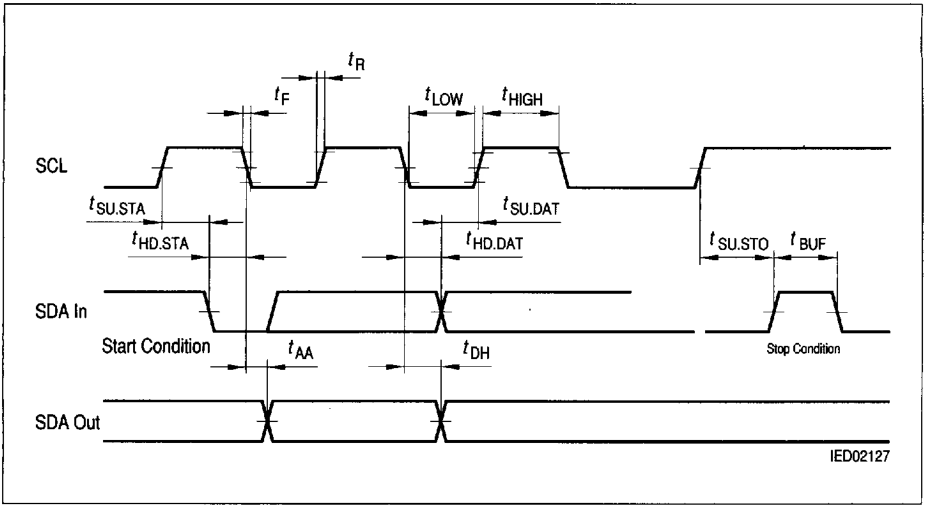

Figure 14
Bus Timing Data