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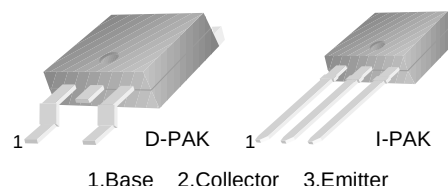
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KSH117

D-PAK for Surface Mount Applications

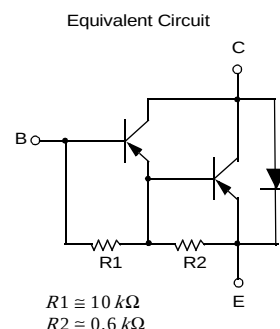
- High DC Current Gain
- Built-in a Damper Diode at E-C
- Lead Formed for Surface Mount Applications (No Suffix)
- Straight Lead (I-PAK, " - I " Suffix)
- Electrically Similar to Popular TIP117



PNP Silicon Darlington Transistor

Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	- 100	V
V_{CEO}	Collector-Emitter Voltage	- 100	V
V_{EBO}	Emitter-Base Voltage	- 5	V
I_C	Collector Current (DC)	- 2	A
I_{CP}	Collector Current (Pulse)	- 4	A
I_B	Base Current	- 50	mA
P_C	Collector Dissipation ($T_C=25^\circ\text{C}$)	20	W
	Collector Dissipation ($T_a=25^\circ\text{C}$)	1.75	W
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature	- 65 ~ 150	$^\circ\text{C}$



Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
$V_{CEO}(\text{sus})$	*Collector-Emitter Sustaining Voltage	$I_C = -30\text{mA}, I_B = 0$	- 100		V
I_{CEO}	Collector Cut-off Current	$V_{CE} = -50\text{V}, I_B = 0$		- 20	μA
I_{CBO}	Collector Cut-off Current	$V_{CB} = -100\text{V}, I_E = 0$		- 20	μA
I_{EBO}	Emitter Cut-off Current	$V_{EB} = -5\text{V}, I_C = 0$		- 2	mA
h_{FE}	*DC Current Gain	$V_{CE} = -3\text{V}, V_{EB} = -0.5\text{A}$ $V_{CE} = -3\text{V}, V_{EB} = -2\text{A}$ $V_{CE} = -3\text{V}, I_C = -4\text{A}$	500 1000 200	12K	
$V_{CE}(\text{sat})$	*Collector-Emitter Saturation Voltage	$I_C = -2\text{A}, I_B = -8\text{mA}$ $I_C = -4\text{A}, I_B = -40\text{mA}$		- 2 - 3	V V
$V_{BE}(\text{sat})$	*Base-Emitter Saturation Voltage	$I_C = -4\text{A}, I_B = -40\text{mA}$		- 4	V
$V_{BE}(\text{on})$	*Base-Emitter On Voltage	$V_{CE} = -3\text{A}, I_C = -2\text{A}$		- 2.8	V
f_T	Current Gain Bandwidth Product	$V_{CE} = -10\text{V}, I_C = -0.75\text{A}$	25		MHz
C_{ob}	Output Capacitance	$V_{CB} = -10\text{V}, I_E = 0$ $f = 0.1\text{MHz}$		200	pF

* Pulse Test: $PW \leq 300\mu\text{s}$, Duty Cycles $\leq 2\%$

Typical Characteristics

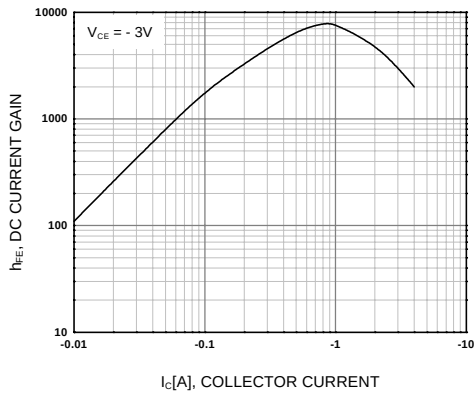


Figure 1. DC current Gain

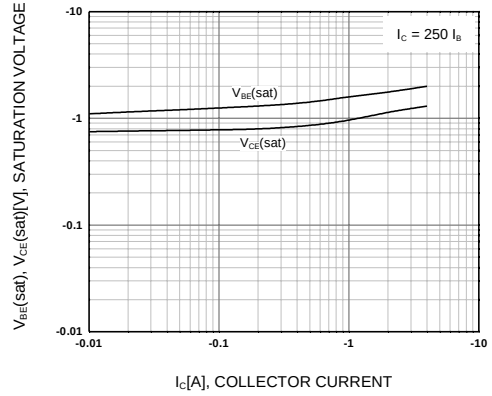


Figure 2. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

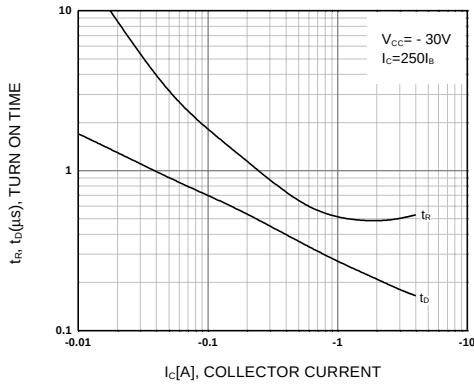


Figure 3. Collector Output Capacitance

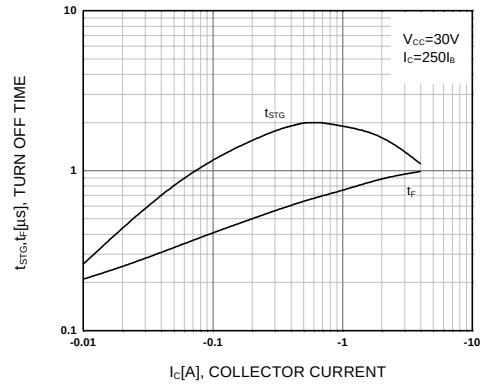


Figure 4. Turn On Time

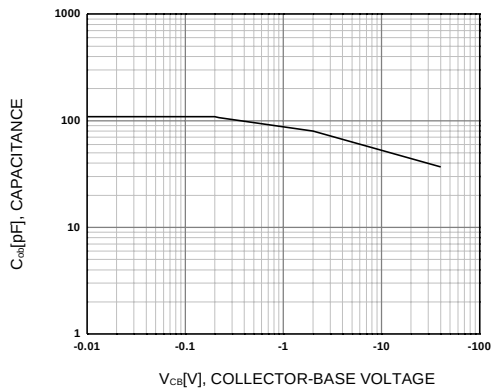


Figure 5. Turn Off Time

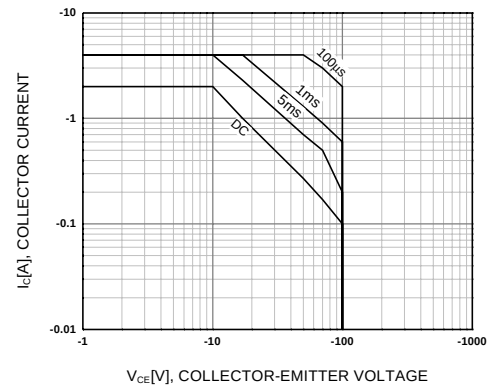
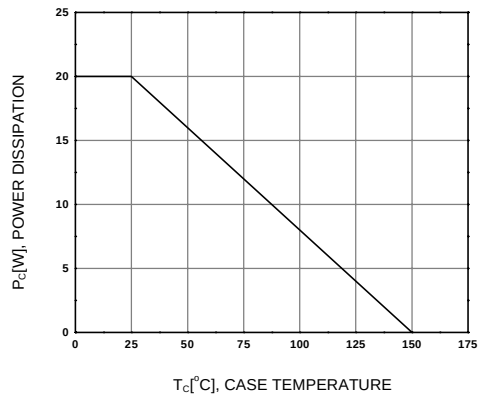
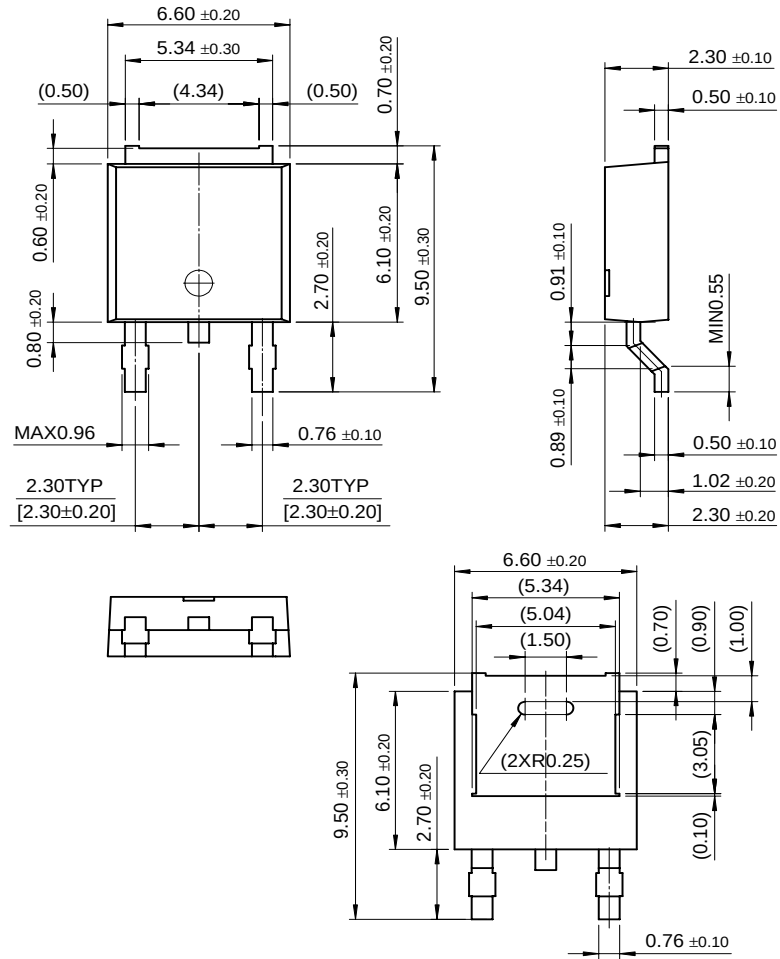


Figure 6. Safe Operating Area

Typical Characteristics (Continued)**Figure 7. Power Derating**

Package Dimensions

D-PAK



Dimensions in Millimeters

Technical drawing of the 2.30TYP connector showing three views: front, side, and top.

Front View Dimensions:

- Overall width: 6.60 ± 0.20
- Inner width: 5.34 ± 0.20
- Flange thickness: 0.60 ± 0.20
- Body height: 6.10 ± 0.20
- Pin height: 1.80 ± 0.20
- Pin length: 9.30 ± 0.30
- Pin diameter: 0.76 ± 0.10
- Pin tip radius: $MAX 0.96$
- Pin spacing: $2.30TYP$ [2.30 ± 0.20]

Side View Dimensions:

- Overall height: 16.10 ± 0.30
- Top flange thickness: 0.50 ± 0.10
- Pin diameter: 0.50 ± 0.10

Top View:

- Shows the layout of the three pins and the central body.

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