

Features

- High speed
 - 15 ns
- Fast t_{DOE}
- CMOS for optimum speed/power
- Low active power
 - 550 mW (max, 15 ns “L” version)
- Low standby power
 - 0.275 mW (max, “L” version)
- 2 V data retention (“L” version only)
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

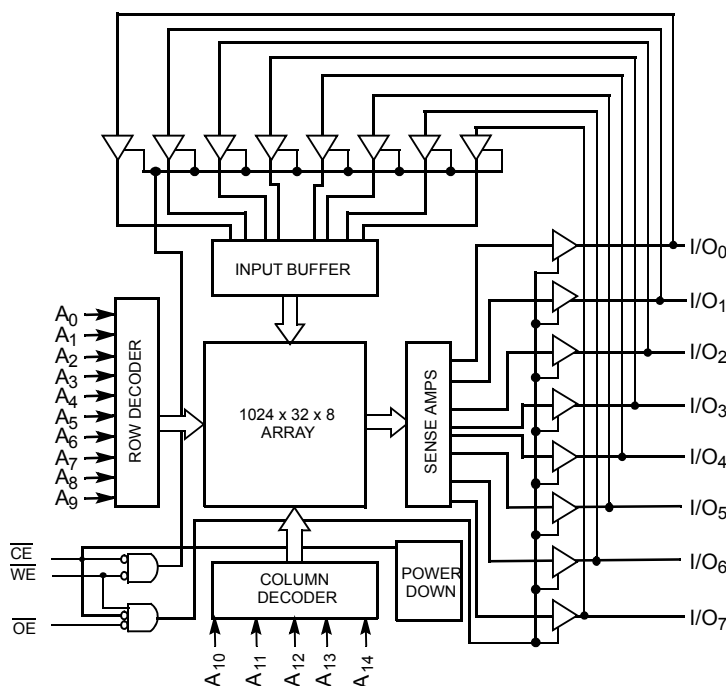
The CY7C199N is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and active LOW Output Enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199N is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW Write Enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable ($\overline{WE}$) is HIGH. A die coat is used to improve alpha immunity.

For a complete list of related documentation, [click here](#).

Logic Block Diagram

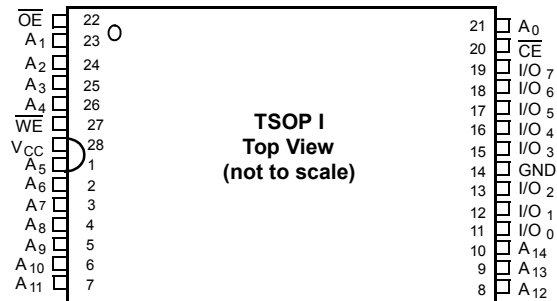


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Pin Configuration

Figure 1. 28-pin TSOP 1 pinout



Selection Guide

Description		-15	Unit
Maximum Access Time		15	ns
Maximum Operating Current	L	100	mA
Maximum CMOS Standby Current	L	0.05	mA

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65 °C to +150 °C

Ambient Temperature with
Power Applied -55 °C to +125 °C

Supply Voltage to Ground Potential
(Pin 28 to Pin 14) -0.5 V to +7.0 V

DC Voltage Applied to Outputs
in High Z State ^[1] -0.5 V to $V_{CC} + 0.5$ V

DC Input Voltage ^[1] -0.5 V to $V_{CC} + 0.5$ V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage
(per MIL-STD-883, Method 3015) > 2001 V

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0 °C to +70 °C	5 V $\pm$ 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-15		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	–	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$	–	0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-5	+5	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	–	100	mA
I_{SB1}	Automatic CE Power-down Current – TTL Inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	–	5	mA
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$, $V_{IN} \geq V_{CC} - 0.3 \text{ V}$, or $V_{IN} \leq 0.3 \text{ V}$, $f = 0$	–	0.05	mA

Notes

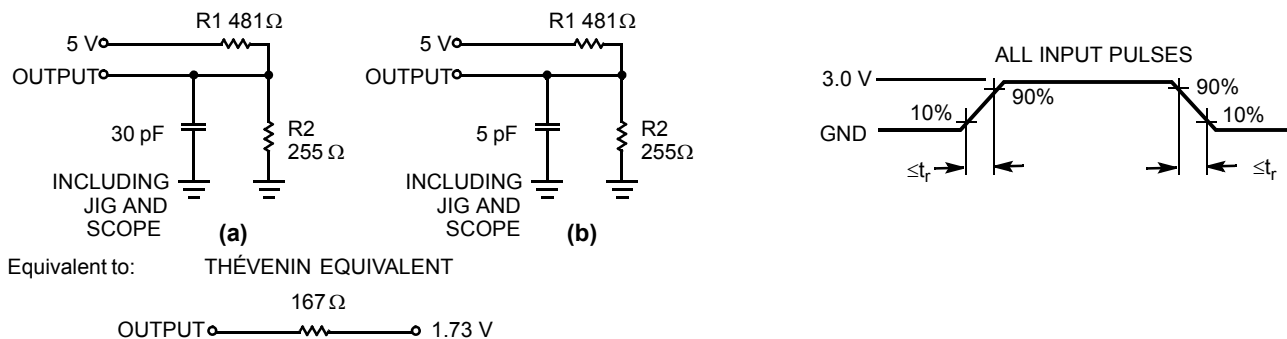
- $V_{IL}(\text{min}) = -2.0 \text{ V}$ for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.

Capacitance

Parameter ^[3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{ V}$	8	pF
C_{OUT}	Output capacitance		8	pF

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[4]



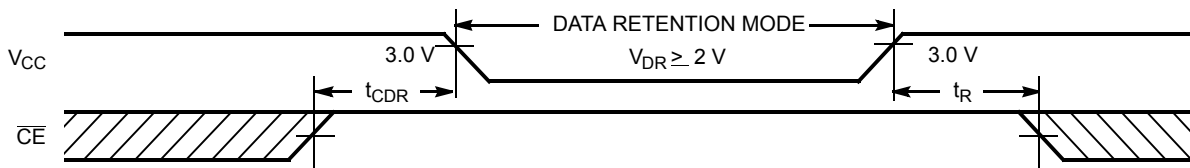
Data Retention Characteristics

Over the Operating Range (L-version only)

Parameter	Description	Conditions ^[5]	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention	$V_{CC} = V_{DR} = 2.0\text{ V}$, $CE \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	2.0	—	V
I_{CCDR}	Data Retention Current		—	10	μA
t_{CDR} ^[3]	Chip Deselect to Data Retention Time		0	—	ns
t_R ^[4]	Operation Recovery Time		200	—	μs

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- $t_R \leq 3\text{ ns}$ for -15 speed.
- No input may exceed $V_{CC} + 0.5\text{ V}$.

Switching Characteristics

Over the Operating Range

Parameter ^[6]	Description	7C199-15		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read Cycle Time	15	–	ns
t _{AA}	Address to Data Valid	–	15	ns
t _{OHA}	Data Hold from Address Change	3	–	ns
t _{ACE}	CE LOW to Data Valid	–	15	ns
t _{DOE}	OE LOW to Data Valid	–	7	ns
t _{LZOE}	OE LOW to Low Z ^[7]	0	–	ns
t _{HZOE}	OE HIGH to High Z ^[7, 8]	–	7	ns
t _{LZCE}	CE LOW to Low Z ^[7]	3	–	ns
t _{HZCE}	CE HIGH to High Z ^[7, 8]	–	7	ns
t _{PU}	CE LOW to Power-up	0	–	ns
t _{PD}	CE HIGH to Power-down	–	15	ns
Write Cycle ^[9, 10]				
t _{WC}	Write Cycle Time	15	–	ns
t _{SCE}	CE LOW to Write End	10	–	ns
t _{AW}	Address Set-up to Write End	10	–	ns
t _{HA}	Address Hold from Write End	0	–	ns
t _{SA}	Address Set-up to Write Start	0	–	ns
t _{PWE}	WE Pulse Width	9	–	ns
t _{SD}	Data Set-up to Write End	9	–	ns
t _{HD}	Data Hold from Write End	0	–	ns
t _{HZWE}	WE LOW to High Z ^[8]	–	7	ns
t _{LZWE}	WE HIGH to Low Z ^[7]	3	–	ns

Notes

- Test conditions assume signal transition time of 3 ns or less for -15 speed, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of [Figure 2 on page 5](#). Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 4. Read Cycle No. 1 [11, 12]

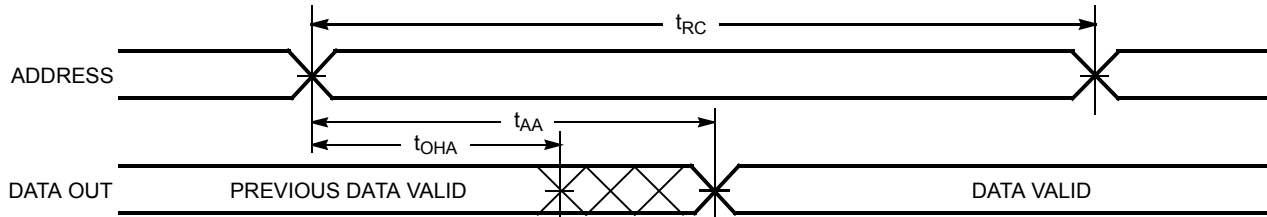


Figure 5. Read Cycle No. 2 [12, 13]

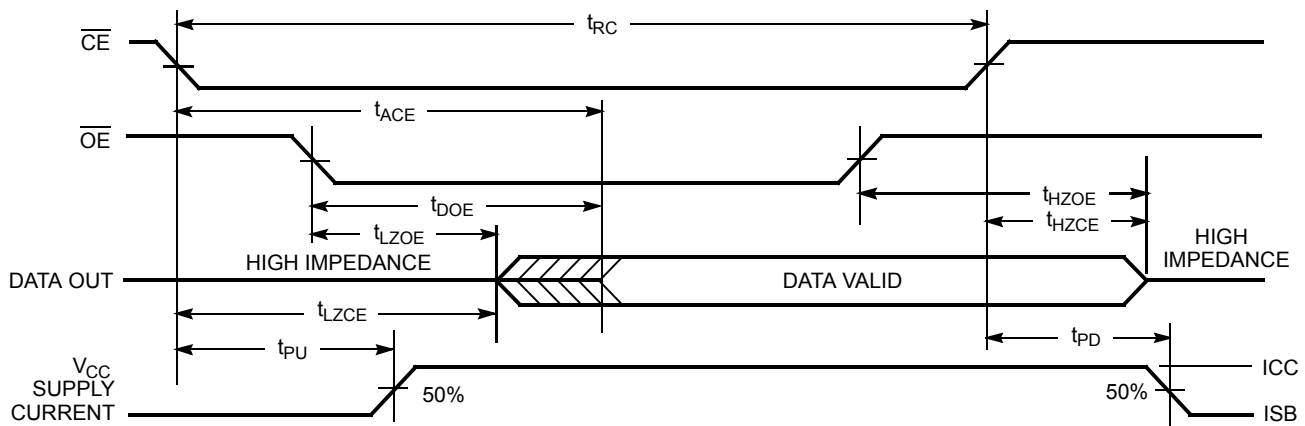
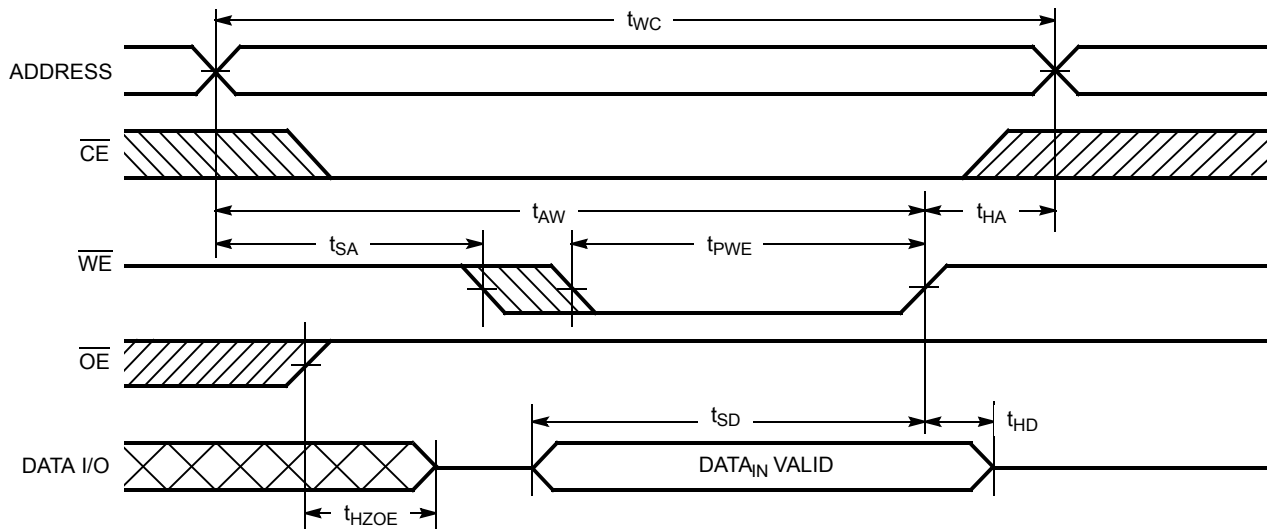


Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [14, 15, 16]



Notes

11. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
15. Data I/O is high impedance if $\overline{OE} = V_{IL}$.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [17, 18, 19]

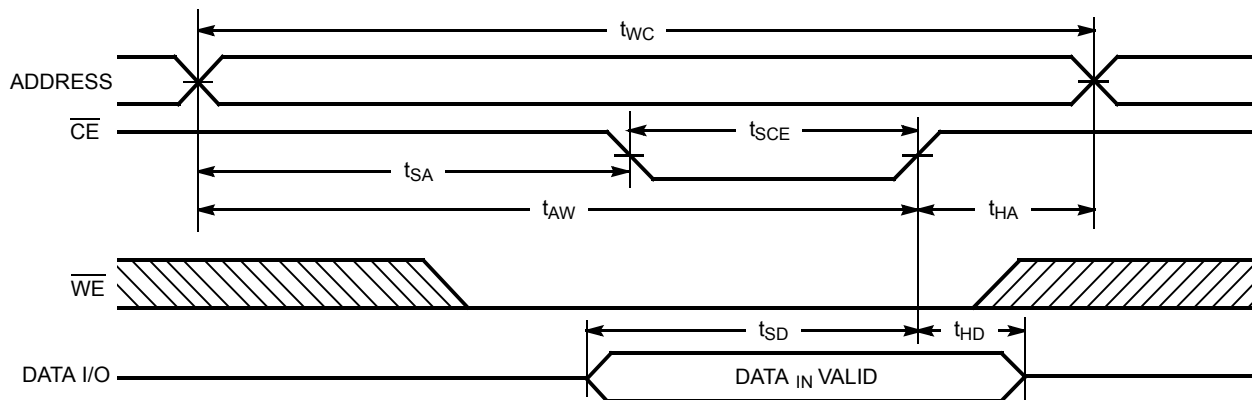
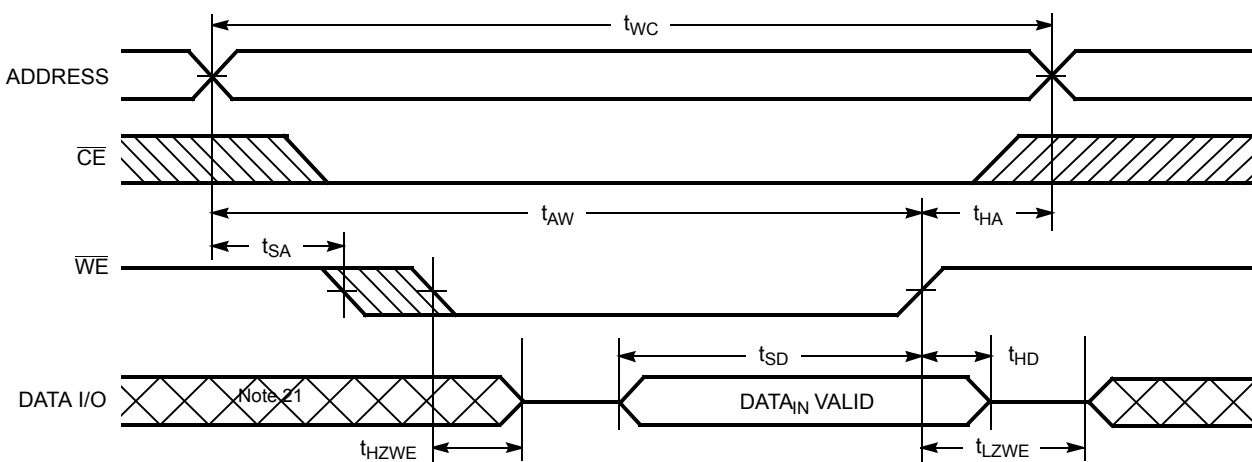


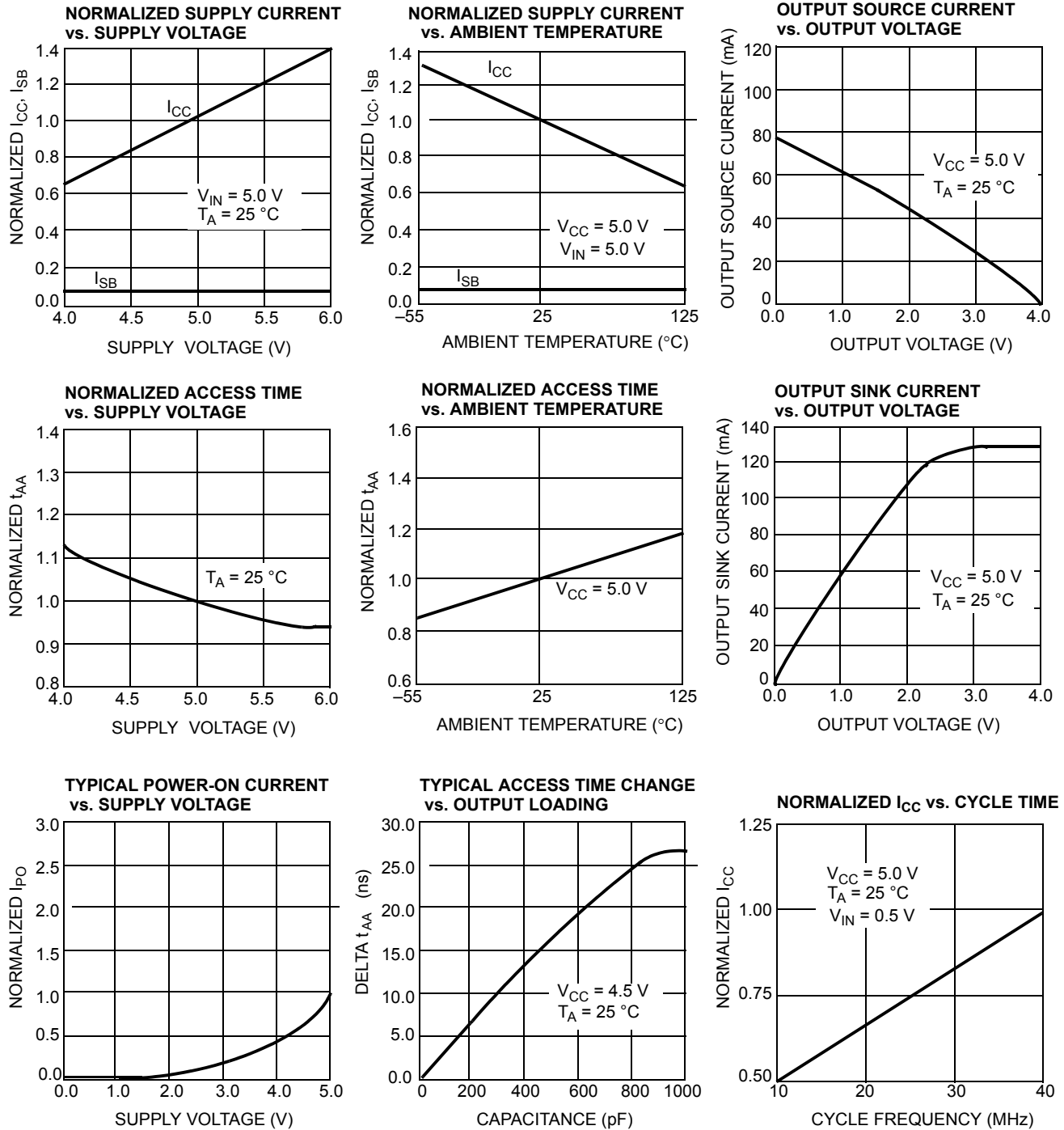
Figure 8. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [19, 20]



Notes

17. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5 \text{ pF}$ as in part (b) of Figure 2 on page 5. Transition is measured $\pm 500 \text{ mV}$ from steady-state voltage.
18. Data I/O is high impedance if $\overline{\text{OE}} = V_{\text{IH}}$.
19. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.
20. The minimum write cycle time for Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD} .
21. During this period, the I/Os are in the output state. Do not apply input signals.

Typical DC and AC Characteristics



Truth Table

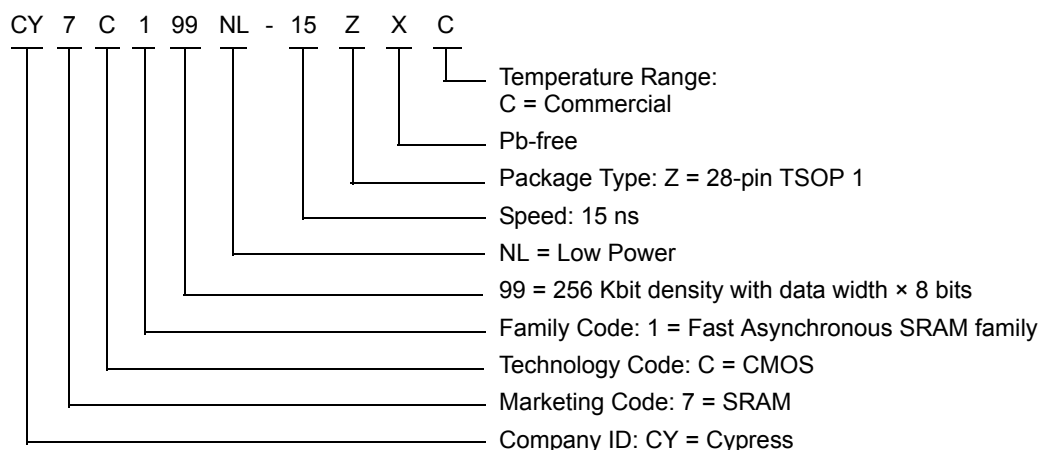
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Output disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C199NL-15ZXC	51-85071	28-pin TSOP 1 (Pb-free)	Commercial

Contact your Local Cypress sales representative for availability of these parts

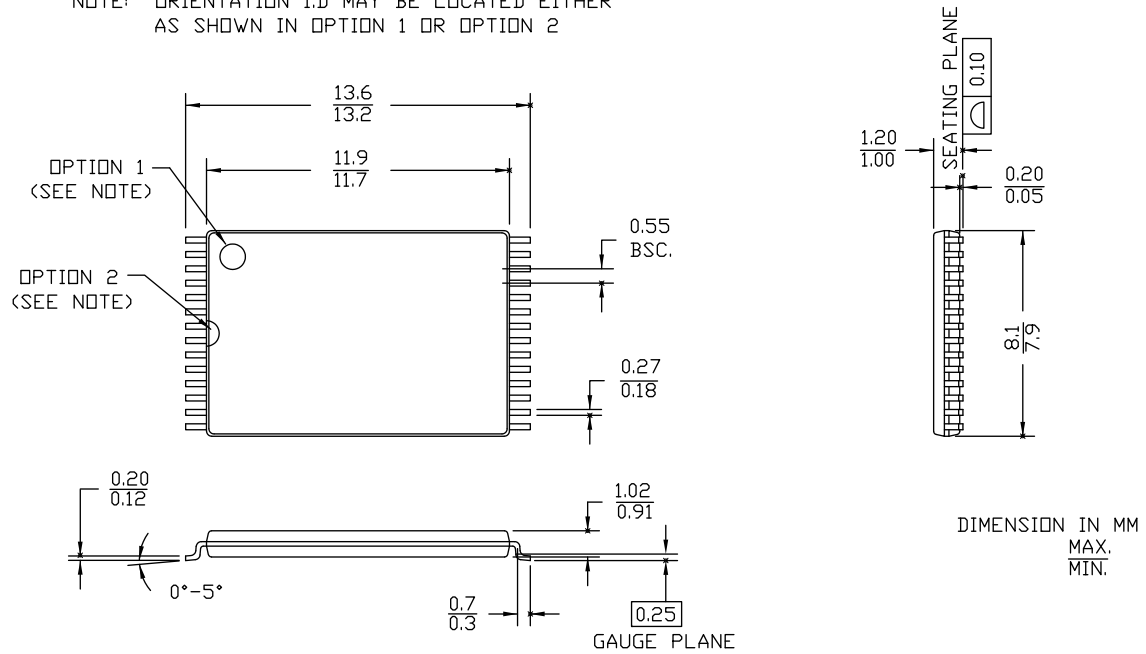
Ordering Code Definitions



Package Diagrams

Figure 9. 28-pin TSOP 1 (8 × 13.4 × 1.2 mm) Package Outline, 51-85071

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



51-85071 *J

Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal-Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C199N, 32 K × 8 Static RAM Document Number: 001-06493				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	423877	See ECN	NXR	New data sheet.
*A	2892510	03/18/2010	VKN	Removed speed bins from the data sheet: 12 ns, 20 ns, 25 ns, 35 ns, and 55 ns. Removed Industrial and Military product information Removed 28-pin (300-Mil) PDIP package Updated Ordering Information table Updated Package Diagram
*B	3109199	12/13/2010	AJU	Added Ordering Code Definitions .
*C	3244591	04/29/2011	PRAS	Updated Package Diagrams . Added Acronyms and Units of Measure . Updated in new template.
*D	4379476	05/14/2014	VINI	Updated Switching Waveforms : Added Note 21 and referred the same note in DATA I/O in Figure 8 . Updated Package Diagrams : spec 51-85071 – Changed revision from *I to *J. Updated in new template. Completing Sunset Review.
*E	4573121	11/18/2014	VINI	Added related documentation hyperlink in page 1.

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