

FEATURES

- Ultra Fast (10ns typ)
- Operates Off **Single** +5V Supply, or $\pm 5V$
- Complementary Output to TTL
- Low Offset Voltage
- No Minimum Input Slew Rate Requirement
- No Power Supply Current Spiking
- Output Latch Capability

APPLICATIONS

- High Speed A to D Converters
- High Speed Sampling Circuits
- Line Receiver
- Extended Range V to F Converters
- Fast Pulse Height/Width Discriminators

DESCRIPTION

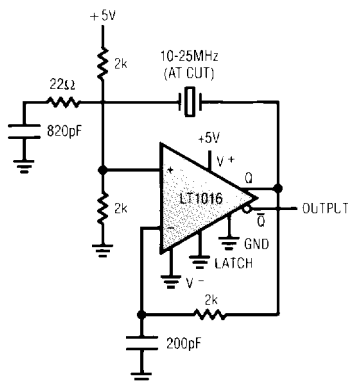
The LT1016 is an ultra fast (10ns) comparator specifically designed to interface directly to TTL logic while operating off either a dual $\pm 5V$ supply or a single +5V supply. Tight offset voltage specifications and high gain allow the LT1016 to be used in precision applications. Matched complementary outputs further extend the versatility of this comparator.

A unique output stage is featured on the LT1016. It provides active drive in both directions for maximum speed into TTL logic or passive loads, yet does not exhibit the large current spikes normally found in "totem pole" output stages. This eliminates the need for a minimum input slew rate typical of other very fast comparators. The ability of the LT1016 to remain stable with the outputs in the active region greatly reduces the problem of output "glitching" when the input signal is slow moving or is low level.

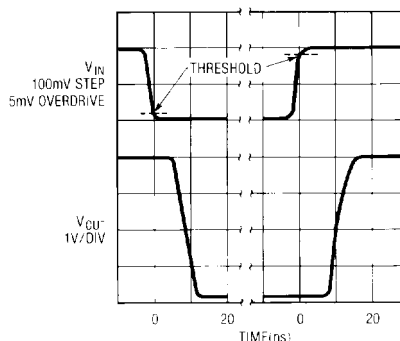
The LT1016 has a true latch pin for retaining input data at the outputs. The outputs will remain latched as long as the latch pin is held high. Quiescent negative power supply current is only 3mA—about ten times lower than competitive units. This reduces die temperature and allows the negative supply pin to be driven from virtually any supply voltage with a simple resistive divider. Device performance is not affected by variations in negative supply voltage.

Note: A companion part to the LT1016 is now available which will sense ground level signals with a single +5V supply. See LT1116.

10-25MHz Crystal Oscillator



Response Time



ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (Note 4)	7V	Operating Temperature Range	
Negative Supply Voltage	7V	LT1016M	-55°C to +125°C
Differential Input Voltage	± 5V	LT1016I	-40°C to +85°C
Input Voltage (Either Input)	Equal to Supplies	LT1016C	0°C to +70°C
Latch Pin Voltage	Equal to Supplies	Storage Temperature Range	-65°C to +150°C
Output Current (Continuous)	± 20mA	Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW H PACKAGE 10-LEAD METAL CAN	TOP VIEW J8 PACKAGE 8-LEAD CERAMIC DIP N8 PACKAGE 8-LEAD PLASTIC DIP	TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SOIC
ORDER PART NUMBER	ORDER PART NUMBER	ORDER PART NUMBER
LT1016MH LT1016CH	LT1016MJ8 LT1016CJ8 LT1016CN8 LT1016IN8	LT1016CS8 LT1016IS8
		PART MARKING
		1016 1016I

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $V^- = 5V$, $V_{OUT}(Q) = 1.4V$, $V_{LATCH} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETERS	CONDITIONS		LT1016M			LT1016C/I			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$ (Note 1),	●		0.8	± 2 3		1.0	± 3 3.5	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift		●		4			4		$\mu V/^\circ C$
I_{OS}	Input Offset Current	(Note 1)	●		0.3	1 1.3		0.3	1 0.3 1.3	μA
I_B	Input Bias Current	(Note 2)	●		5	10 13		5	10 13	μA
	Input Voltage Range	(Note 5)	●	-3.75		+3.5	-3.75		+3.5	V
		Single +5V Supply	●	+1.25		+3.5	+1.25		+3.5	
CMRR	Common-Mode Rejection	$-3.75V \leq V_{CM} \leq +3.5V$	●	80	96		80	96		dB
PSRR	Supply Voltage Rejection	Positive Supply $4.6V \leq V^+ \leq 5.4V$ LT1016M/C	●	54	75		60	75		dB
		Positive Supply $4.6V \leq V^+ \leq 5.4V$ LT1016I	●				54	75		
		Negative Supply $2V \leq V^- \leq 7V$	●	80	100		80	100		
A_V	Small Signal Voltage Gain	$1V \leq V_{OUT} \leq 2V$		1400	3000		1400	3000		V/V
V_{OH}	Output High Voltage	$V^+ \leq 4.6V$	●	2.7	3.4		2.7	3.4		V
		$I_{OUT} = 1mA$ $I_{OUT} = 10mA$	●	2.4	3.0		2.4	3.0		
V_{OL}	Output Low Voltage	$I_{SINK} = 4mA$ $I_{SINK} = 10mA$	●		0.3 0.4	0.5		0.3 0.4	0.5	V
I^+	Positive Supply Current		●		25	35		25	35	mA
I^-	Negative Supply Current		●		3	5		3	5	mA
V_{IH}	Latch Pin Hi Input Voltage		●	2.0			2.0			V
V_{IL}	Latch Pin Lo Input Voltage		●			0.8			0.8	V
I_{IL}	Latch Pin Current	$V_{LATCH} = 0V$	●			500			500	μA
t_{PD}	Propagation Delay (Note 3)	$\Delta V_{IN} = 100mV$, $OD = 5mV$	●		10	14 16		10	14 16	ns
		$\Delta V_{IN} = 100mV$, $OD = 20mV$	●		9	12 15		9	12 15	
			●							
Δt_{PD}	Differential Propagation Delay	(Note 3) $\Delta V_{IN} = 100mV$, $OD = 5mV$				3			3	ns
	Latch Setup Time				2			2		ns

The ● denotes the specifications which apply over the full operating temperature range. For MIL-STD components, please refer to LTC883 data sheet for test listing and parameters.

Note 1: Input offset voltage is defined as the average of the two volages measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

Note 2: Input bias current (I_B) is defined as the average of the two input currents.

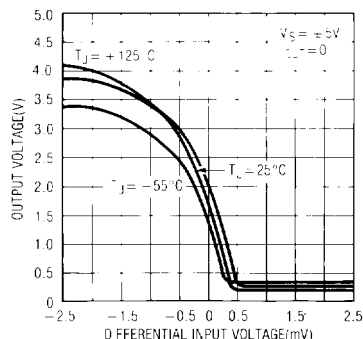
Note 3: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1016 is sample tested with a 1V step and 500mV overdrive at $25^\circ C$ only. Correlation tests have shown that t_{PD} and Δt_{PD} limits shown can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct. For low overdrive conditions V_{OS} is added to overdrive.

Note 4: Electrical specifications apply only up to 5.4V.

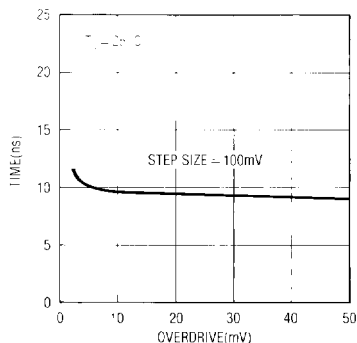
Note 5: See text for discussion of input voltage range for supplies other than $\pm 5V$, or $+5V$.

TYPICAL PERFORMANCE CHARACTERISTICS

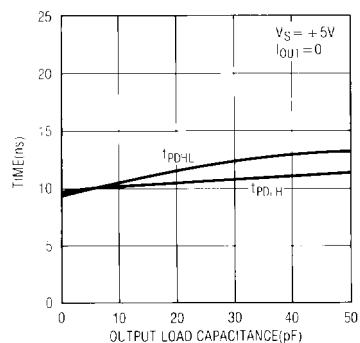
Gain Characteristics



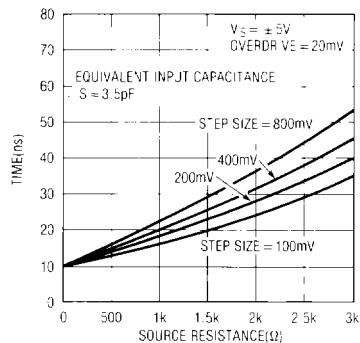
Propagation Delay vs Overdrive



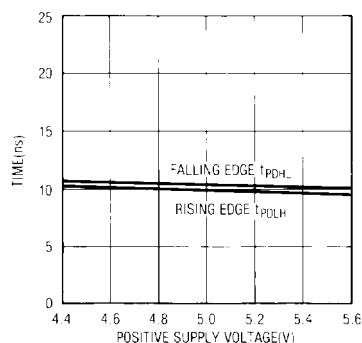
Propagation Delay vs Load Capacitance



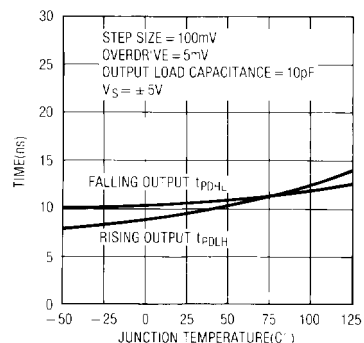
Propagation Delay vs Source Resistance



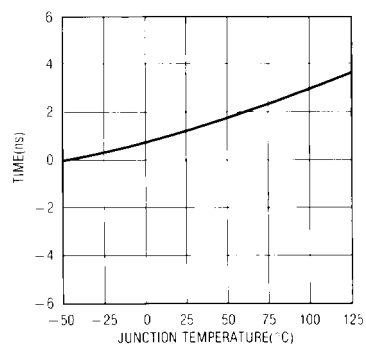
Propagation Delay vs Supply Voltage



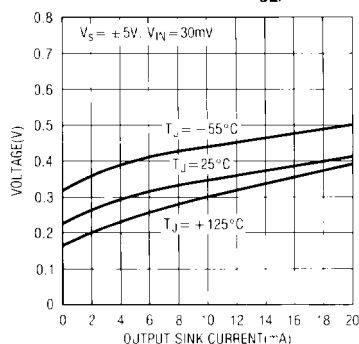
Propagation Delay vs Temperature



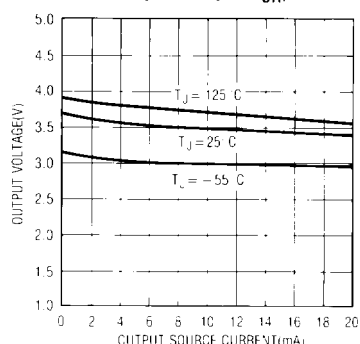
Latch Set-Up Time



Output Low Voltage (V_{OL})

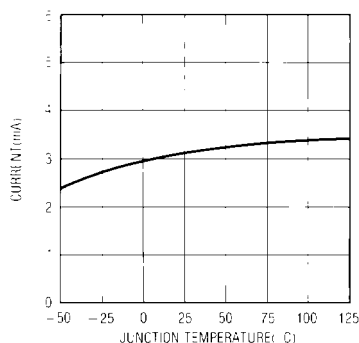


Output High Voltage (V_{OH})

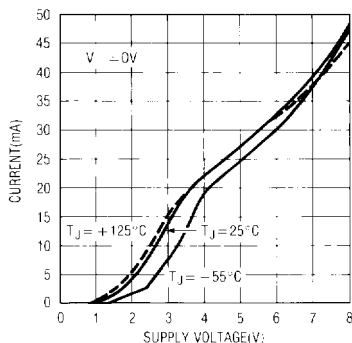


TYPICAL PERFORMANCE CHARACTERISTICS

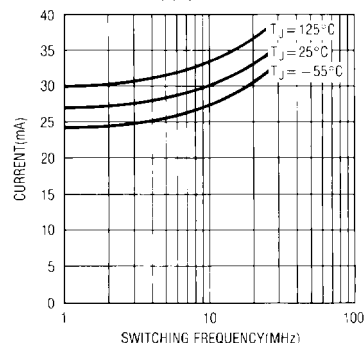
Negative Supply Current



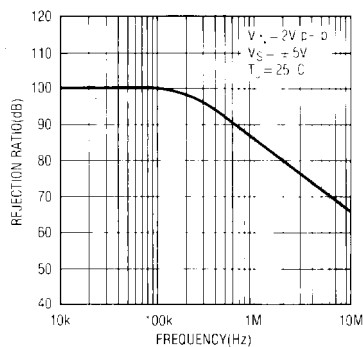
Positive Supply Current



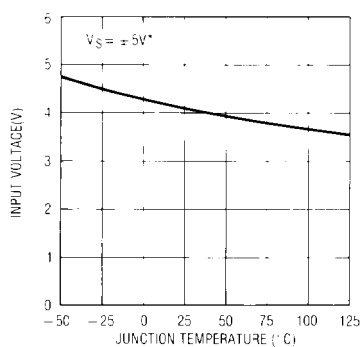
Positive Supply Current



Common-Mode Rejection

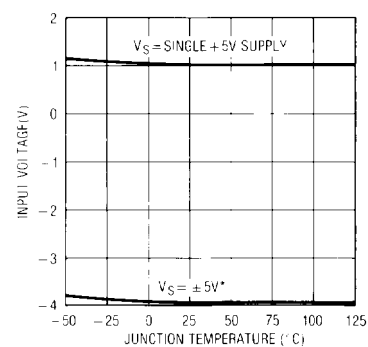


Positive Common-Mode Limit



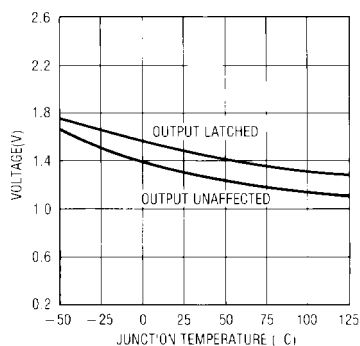
*SEE APPLICATION SECTION FOR COMMON-MODE LIMIT WITH VARYING SUPPLY VOLTAGE.

Negative Common-Mode Limit

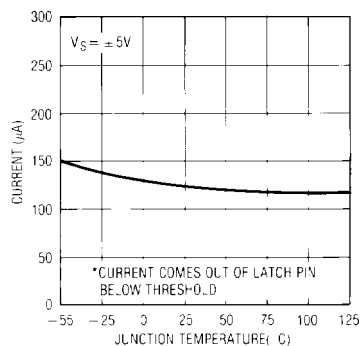


*SEE APPLICATION SECTION FOR COMMON-MODE LIMIT WITH VARYING SUPPLY VOLTAGE.

Latch Pin Threshold



Latch Pin Current*



*CURRENT COMES OUT OF LATCH PIN BELOW THRESHOLD

APPLICATIONS INFORMATION

Common-Mode Considerations

The LT1016 is specified for a common-mode range of -3.75V to $+3.5\text{V}$ with supply voltages of $\pm 5\text{V}$. A more general consideration is that the common-mode range is 1.25V above the negative supply and 1.5V below the positive supply, independent of the actual supply voltage. The criteria for common-mode limit is that the output still responds correctly to a small differential input signal. Either input may be outside the common-mode limit (up to the supply voltage) as long as the remaining input is within the specified limit, and the output will still respond correctly. There is one consideration, however, for inputs which exceed the positive common-mode limit. Propagation delay will be increased by up to 10ns if the signal input is more positive than the upper common-mode limit and then switches back to within the common-mode range. This effect is not seen for signals more negative than the lower common-mode limit.

Input Impedance and Bias Current

Input bias current is measured with the output held at 1.4V . As with any simple NPN differential input stage, the LT1016 bias current will go to zero on an input which is low and double on the input which is high. If both inputs are less than 0.8V above V^- , both input bias currents will go to zero. If either input exceeds the positive common-mode limit, input bias current will increase rapidly, approaching several milliamperes at $V_{IN} = V^+$.

Differential input resistance at zero differential input voltage is about $10\text{k}\Omega$, rapidly increasing as larger DC differential input signals are applied. Common-mode input resistance is about $4\text{M}\Omega$ with zero differential input voltage. With large differential input signals, the high input will have an input resistance of about $2\text{M}\Omega$ and the low input, greater than $20\text{M}\Omega$.

Input capacitance is typically 3.5pF . This is measured by inserting a $1\text{k}\Omega$ resistor in series with the input and measuring the resultant change in propagation delay.

Latch Pin Dynamics

The latch pin is intended to retain input data (output latched) when the latch pin goes high. This pin will float to a high state when disconnected, so a flow-through condition requires that the latch pin be grounded. To guarantee data retention, the input signal must be valid at least 5ns before the latch goes high (set-up time) and must remain valid at least 3ns after the latch goes high (hold time). When the latch goes low, new data will appear at the output in approximately $8\text{--}10\text{ns}$. The latch pin is designed to be driven with TTL or CMOS gates. It has no built-in hysteresis.

Measuring Response Time

The LT1016 is able to respond quickly to fast low level signals because it has a very high gain-bandwidth product ($\approx 50\text{GHz}$), even at very high frequencies. To properly measure the response of the LT1016 requires an input signal source with very fast rise times and exceptionally clean settling characteristics. This last requirement comes about because the standard comparator test calls for an input step size that is large compared to the overdrive amplitude. Typical test conditions are 100mV step size with only 5mV overdrive. This requires an input signal that settles to within 1% (1mV) of final value in only a few nanoseconds with no ringing or "long tailing". Ordinary high speed pulse generators are not capable of generating such a signal, and in any case, no ordinary oscilloscope is capable of displaying the waveform to check its fidelity. Some means must be used to inherently generate a fast, clean edge with known final value.

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response to the pulse generator (Trace A) is as fast as a TTL inverter (Trace C) even when the LT1016 has only millivolts of input signal! Linear circuits operating with this kind of speed make many engineers justifiably wary. Nanosecond domain linear circuits are widely associated with oscillations, mysterious shifts in circuit characteristics, unintended modes of operation and outright failure to function.

Other common problems include different measurement results using various pieces of test equipment, inability to make measurement connections to the circuit without inducing spurious responses and dissimilar operation between two "identical" circuits. If the components used in the circuit are good and the design is sound, all of the above problems can usually be traced to failure to provide a proper circuit "environment." To learn how to do this requires studying the causes of the aforementioned difficulties.

By far the most common error involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move as internal cur-

rent levels of the devices connected to it change. This will almost always cause unruly operation. In addition, several devices connected to an unbypassed supply can "communicate" through the finite supply impedances, causing erratic modes. Bypass capacitors furnish a simple way to eliminate this problem by providing a local reservoir of energy at the device. The bypass capacitor acts like an electrical flywheel to keep supply impedance low at high frequencies. The choice of what type of capacitors to use for bypassing is a critical issue and should be approached carefully. An unbypassed LT1016 is shown responding to a pulse input in Figure 3. The power supply the LT1016 sees at its terminals has high impedance at high frequency. This impedance forms a voltage divider with the LT1016, allowing the supply to move as internal conditions in the comparator change. This causes local feedback and oscillation occurs. Although the LT1016 responds to the input pulse, its output is a blur of 100MHz oscillation. *Always use bypass capacitors.*

In Figure 4 the LT1016's supplies are bypassed, but it still oscillates. In this case, the bypass units are either too far from the device or are lossy capacitors. *Use capacitors with good high frequency characteristics and mount*

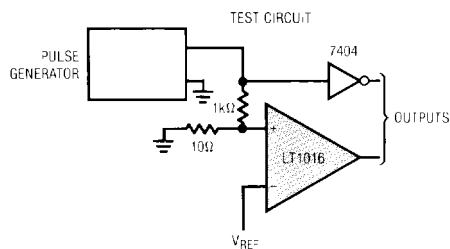


Figure 2. LT1016 vs a TTL Gate

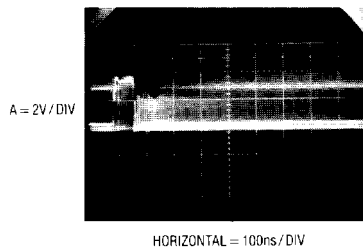
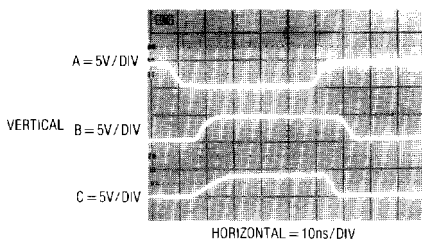


Figure 3. Unbypassed LT1016 Response

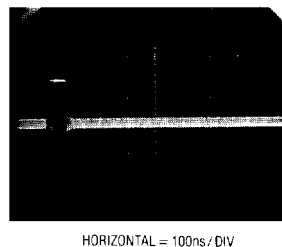


Figure 4. LT1016 Response with Poor Bypassing

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them as close as possible to the LT1016. An inch of wire between the capacitor and the LT1016 can cause problems. If operation in the linear region is desired, the LT1016 must be over a ground plate with good RF bypass capacitors ($\geq 0.01\mu\text{F}$) having lead lengths less than 0.2 inches. Do not use sockets.

In Figure 5 the device is properly bypassed but a new problem pops up. This photo shows both outputs of the comparator. Trace A appears normal, but Trace B shows an excursion of almost 8V — quite a trick for a device running from a +5V supply. This is a commonly reported problem in high speed circuits and can be quite confusing. It is not due to suspension of natural law, but is traceable to a grossly miscompensated or improperly selected oscilloscope probe. *Use probes which match your oscilloscope's input characteristics and compensate them properly.* Figure 6 shows another probe-induced problem. Here, the amplitude seems correct but the 10ns response time LT1016 appears to have 50ns edges! In this case, the

probe used is too heavily compensated or slow for the oscilloscope. Never use 1X or "straight" probes. Their bandwidth is 20MHz or less and capacitive loading is high. *Check probe bandwidth to ensure it is adequate for the measurement. Similarly, use an oscilloscope with adequate bandwidth.*

In Figure 7 the probes are properly selected and applied but the LT1016's output rings and distorts badly. In this case, the probe ground lead is too long. For general purpose work most probes come with ground leads about 6 inches long. At low frequencies this is fine. At high speed, the long ground lead looks inductive, causing the ringing shown. High quality probes are always supplied with some short ground straps to deal with this problem. Some come with very short spring clips which fix directly to the probe tip to facilitate a low impedance ground connection. For fast work, the ground connection to the probe should not exceed 1 inch in length. *Keep the probe ground connection as short as possible.*

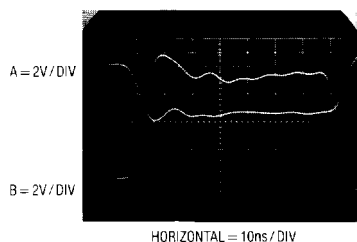


Figure 5. Improper Probe Compensation Causes Seemingly Unexplainable Amplitude Error

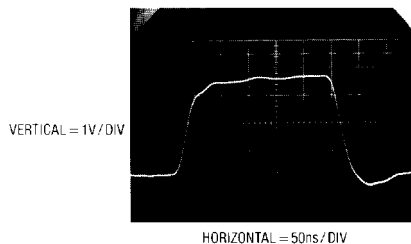


Figure 6. Overcompensated or Slow Probes Make Edges Look Too Slow

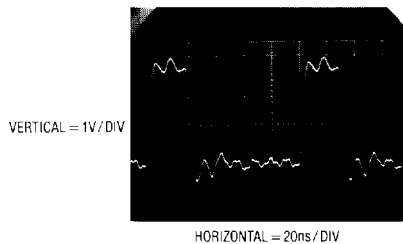


Figure 7. Typical Results Due to Poor Probe Grounding

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Figure 8 shows the LT1016's output (Trace B) oscillating near 40MHz as it responds to an input (Trace A). Note that the input signal shows artifacts of the oscillation. This example is caused by improper grounding of the comparator. In this case, the LT1016's ground pin connection is 1 inch long. The ground lead of the LT1016 must be as short as possible and connected directly to a low impedance ground point. Any substantial impedance in the LT1016's ground path will generate effects like this. The reason for this is related to the necessity of bypassing the power supplies. The inductance created by a long device ground lead permits mixing of ground currents, causing undesired effects in the device. The solution here is simple. *Keep the LT1016's ground pin connection as short (typically 1/4 inch) as possible and run it directly to a low impedance ground. Do not use sockets.*

Figure 9 addresses the issue of the "low impedance ground," referred to previously. In this example, the output is clean except for chattering around the edges. This photograph was generated by running the LT1016 without a "ground plane." A ground plane is formed by using a continuous conductive plane over the surface of the cir-

cuit board. The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (AC currents travel along the surface of a conductor) and covers the entire area of the board, it provides a way to access a low inductance ground from anywhere on the board. Also, it minimizes the effects of stray capacitance in the circuit by referring them to ground. This breaks up potential unintended and harmful feedback paths. *Always use a ground plane with the LT1016, when input signal levels are low or slow moving.*

"Fuzz" on the edges is the difficulty in Figure 10. This condition appears similar to Figure 10, but the oscillation is more stubborn and persists well after the output has gone low. This condition is due to stray capacitive feedback from the outputs to the inputs. A 3k Ω input source impedance and 3pF of stray feedback allowed this oscillation. The solution for this condition is not too difficult. *Keep source impedances as low as possible, preferably 1k Ω or less. Route output and input pins and components away from each other.*

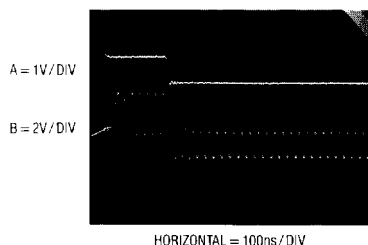


Figure 8. Excessive LT1016 Ground Path Resistance Causes Oscillation

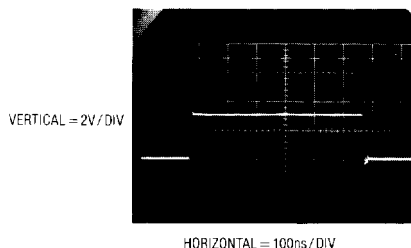


Figure 9. Transition Instabilities Due to No Ground Plane

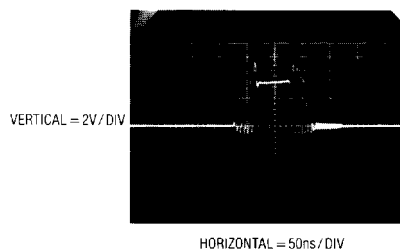


Figure 10. 3pF Stray Capacitive Feedback with 3k Ω Source Can Cause Oscillation

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The opposite of stray-caused oscillations appears in Figure 11. Here, the output response (Trace B) badly lags the input (Trace A). This is due to some combination of high source impedance and stray capacitance to ground at the input. The resulting RC forces a lagged response at the input, and output delay occurs. An RC combination of $2\text{k}\Omega$ source resistance and 10pF to ground gives a 20ns time constant — significantly longer than the LT1016's response time. *Keep source impedances low and minimize stray input capacitance to ground.*

Figure 12 shows another capacitance-related problem. Here the output does not oscillate, but the transitions are discontinuous and relatively slow. The villain of this situation is a large output load capacitance. This could be caused by cable driving, excessive output lead length or the input characteristics of the circuit being driven. In most situations this is undesirable and may be eliminated by buffering heavy capacitive loads. In a few cir-

cumstances it may not affect overall circuit operation and is tolerable. *Consider the comparator's output load characteristics and their potential effect on the circuit. If necessary, buffer the load.*

Another output-caused fault is shown in Figure 13. The output transitions are initially correct but end in a ringing condition. The key to the solution here is the ringing. What is happening is caused by an output lead which is too long. The output lead looks like an unterminated transmission line at high frequencies and reflections occur. This accounts for the abrupt reversal of direction on the leading edge and the ringing. If the comparator is driving TTL this may be acceptable, but other loads may not tolerate it. In this instance, the direction reversal on the leading edge might cause trouble in a fast TTL load. *Keep output lead lengths short. If they get much longer than a few inches, terminate with a resistor (typically 250Ω – 400Ω).*

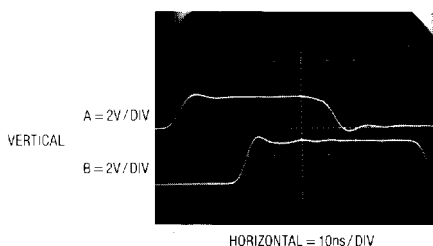


Figure 11. Stray 5pF Capacitance from Input to Ground Causes Delay

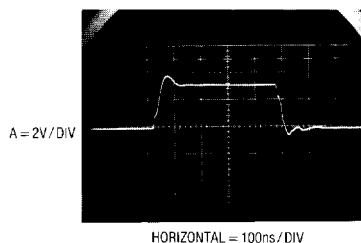


Figure 12. Excessive Load Capacitance Forces Edge Distortion

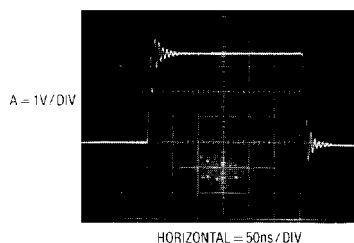


Figure 13. Lengthy, Unterminated Output Lines Ring from Reflections

APPLICATIONS INFORMATION

200ns-0.01% Sample-and-Hold Circuit

Figure 14's circuit uses the LT1016's high speed to improve upon a standard circuit function. The 200ns acquisition time is well beyond monolithic sample-and-hold capabilities. Other specifications exceed the best commercial unit's performance. This circuit also gets around many of the problems associated with standard sample-and-hold approaches, including FET switch errors and amplifier settling time. To achieve this, the LT1016's high speed is used in a circuit which completely abandons traditional sample-and-hold methods.

Important specifications for this circuit include:

Acquisition Time	< 200ns
Common-Mode Input Range	$\pm 3V$
Droop	$1\mu V/\mu s$
Hold Step	2mV
Hold Settling Time	15ns
Feedthrough Rejection	$>> 100dB$

When the sample-hold line goes low, a linear ramp starts just below the input level and ramps upward. When the ramp voltage reaches the input voltage, A1 shuts off the ramp, latches itself off, and sends out a signal indicating sampling is complete.

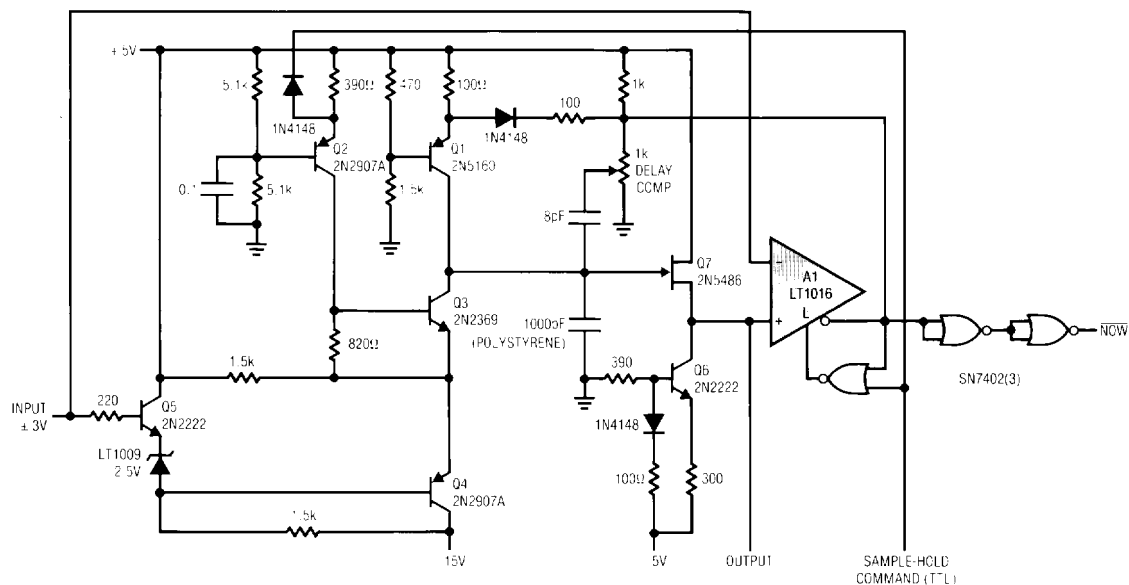


Figure 14. 200ns Sample-and Hold

APPLICATIONS INFORMATION

1.8 μ s, 12-Bit A-D Converter

The LT1016's high speed is used to implement a very fast 12-bit A-D converter in Figure 15. The circuit is a modified form of the standard successive approximation approach and is faster than most commercial SAR 12-bit units. In this arrangement the 2504 successive approximation register (SAR), A1 and C1 test each bit, beginning with the MSB, and produce a digital word representing V_{IN} 's value.

To get faster conversion time, the clock is controlled by the window comparator monitoring the DAC-input summing junction. Additionally, the DMOS FET clamps the DAC output to ground at the beginning of each clock cycle, shortening DAC settling time. After the fifth bit is converted, the clock runs at maximum speed.

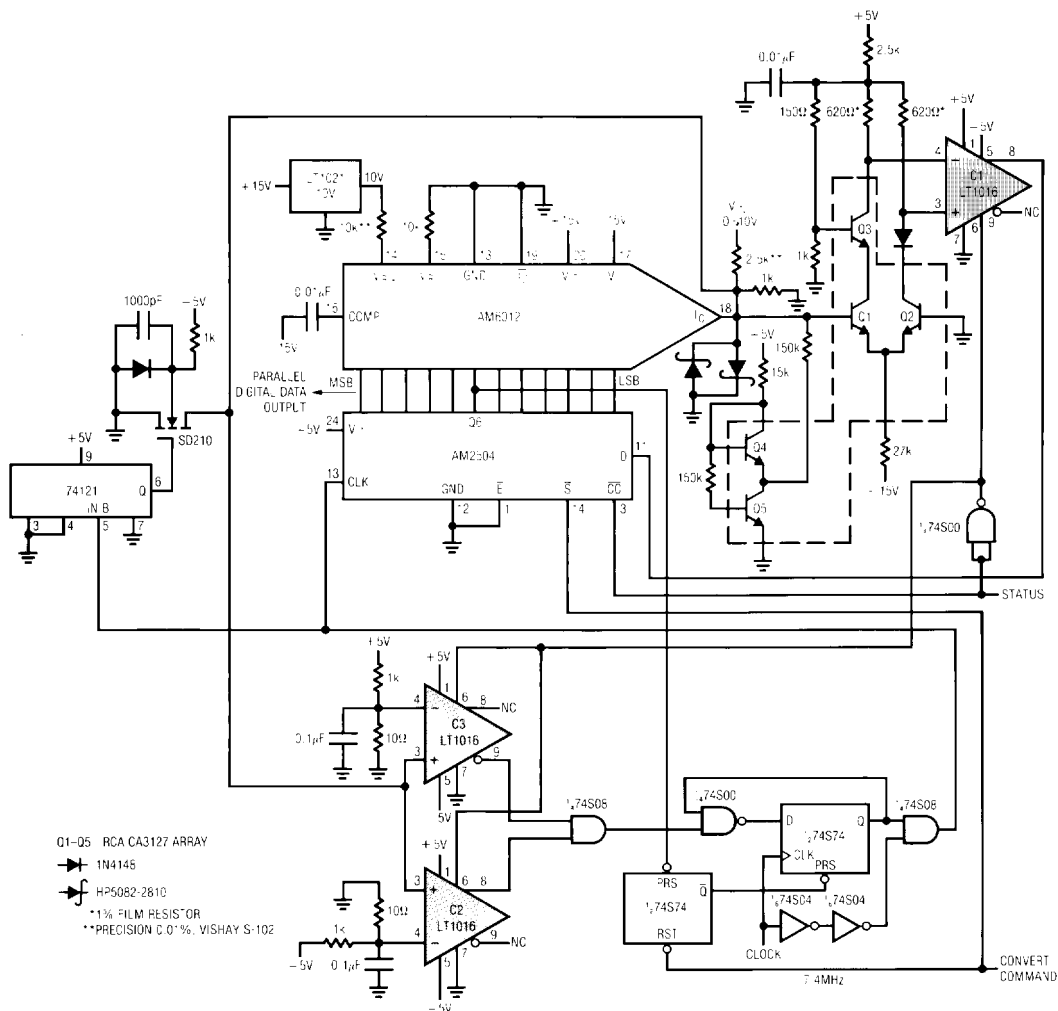
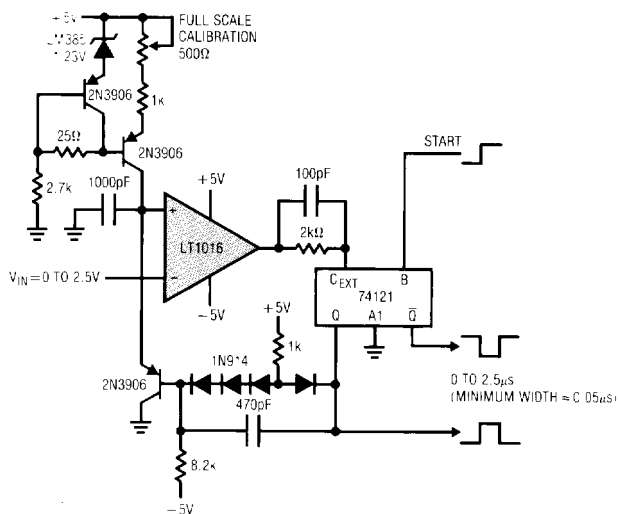


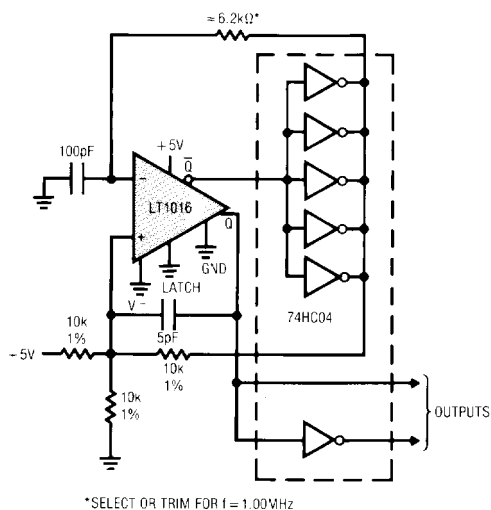
Figure 15. 12-Bit 1.8 μ s SAR A-D

APPLICATIONS INFORMATION

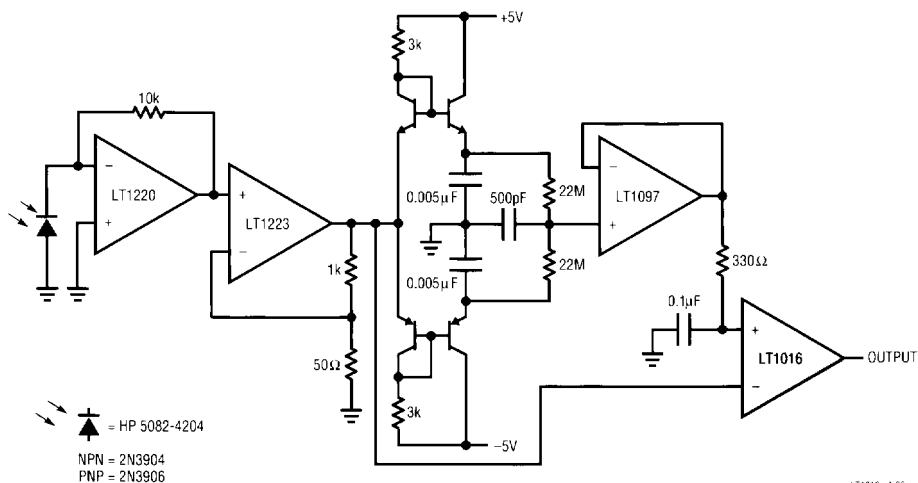
Voltage Controlled Pulse Width Generator



Single Supply Precision RC 1MHz Oscillator

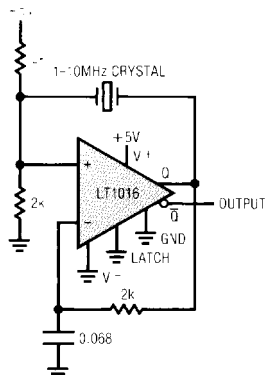


50MHz Fiber Optic Receiver with Adaptive Trigger

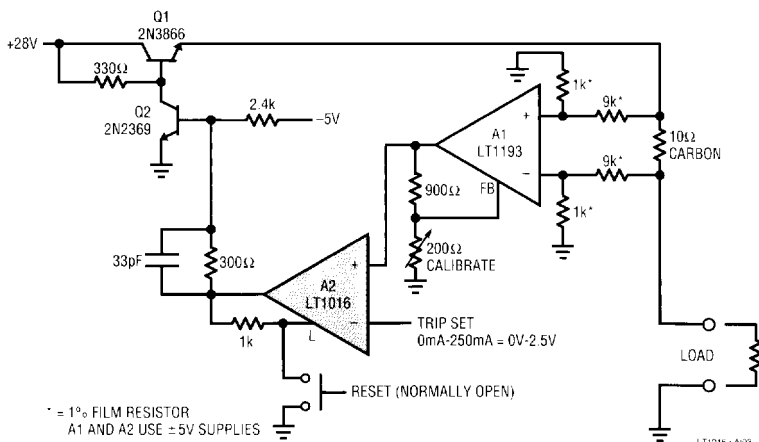


APPLICATIONS INFORMATION

1-10MHz Crystal Oscillator



18ns Fuse with Voltage Programmable Trip Point



APPENDIX A

About Level Shifts

The TTL output of the LT1016 will interface with many circuits directly. Many applications, however, require some form of level shifting of the output swing. With LT1016-based circuits this is not trivial because it is desirable to maintain very low delay in the level shifting stage. When designing level shifters, keep in mind that the TTL output of the LT1016 is a sink-source pair (Figure A1) with good ability to drive capacitance (such as feedforward capacitors).

Figure A2 shows a non-inverting voltage gain stage with a 15V output. When the LT1016 switches, the base-emitter voltages at the 2N2369 reverse, causing it to switch very quickly. The 2N3866 emitter-follower gives a low impedance output and the Schottky diode aids current sink capability.

Figure A3 is a very versatile stage. It features a bipolar swing which may be programmed by varying the output

transistor's supplies. This 3ns delay stage is ideal for driving FET switch gates. Q1, a gated current source, switches the Baker-clamped output transistor, Q2. The heavy feedforward capacitor from the LT1016 is the key to low delay, providing Q2's base with nearly ideal drive. This capacitor loads the LT1016's output transition (Trace A, Figure A4), but Q2's switching is clean (Trace B, Figure A4) with 3ns delay on the rise and fall of the pulse.

Figure A5 is similar to A2 except that a sink transistor has replaced the Schottky diode. The two emitter-followers drive a power MOSFET which switches 1A at 15V. Most of the 7ns–9ns delay in this stage occurs in the MOSFET and the 2N2369.

When designing level shifters, remember to use transistors with fast switching times and high f_T 's. To get the kind of results shown, switching times in the ns range and f_T 's approaching 1GHz are required.

APPENDIX A

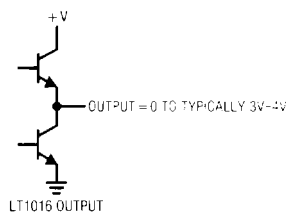


Figure A1

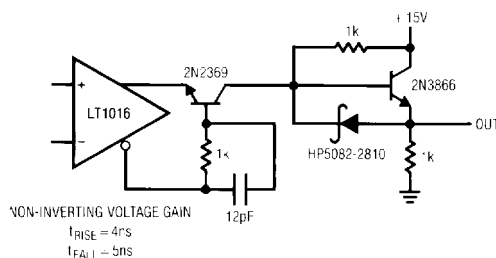


Figure A2

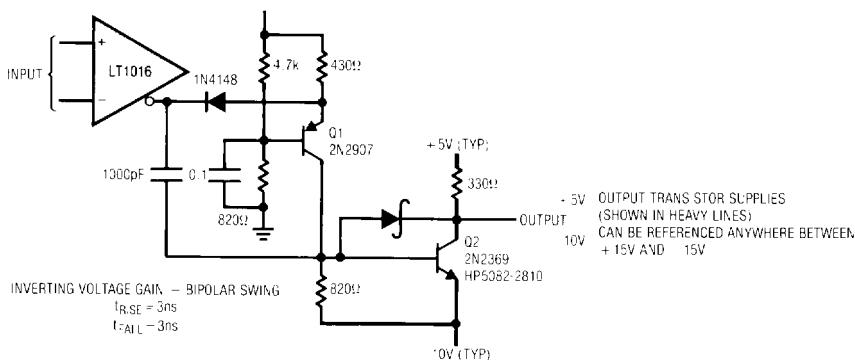


Figure A3

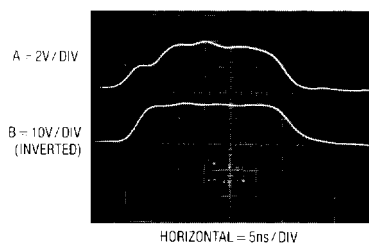


Figure A4. Figure A3's Waveforms

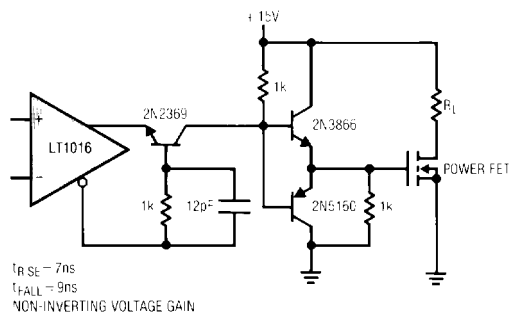
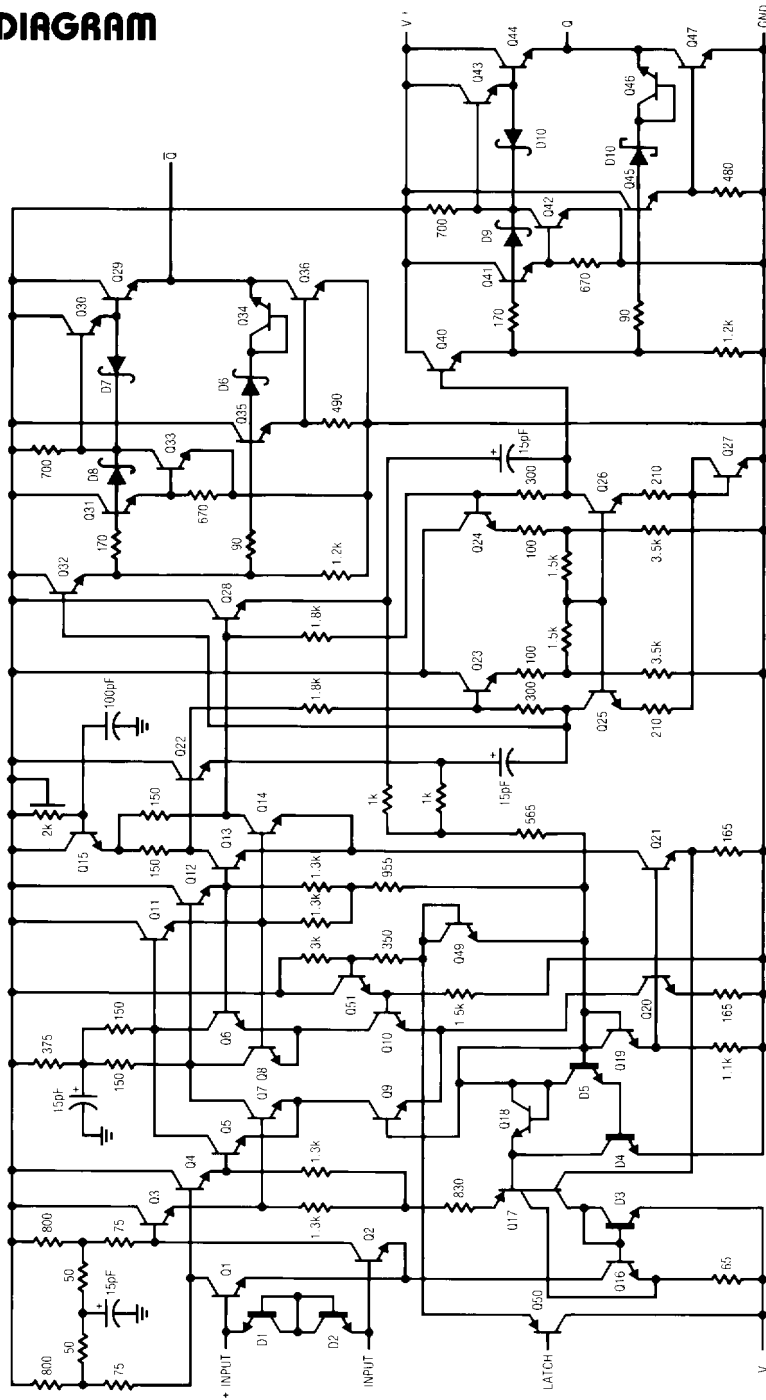


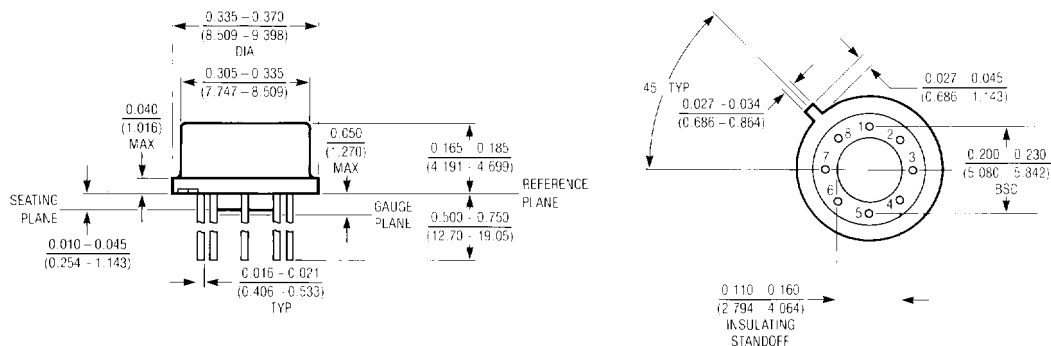
Figure A5

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package **10-Lead TO-5 Metal Can**

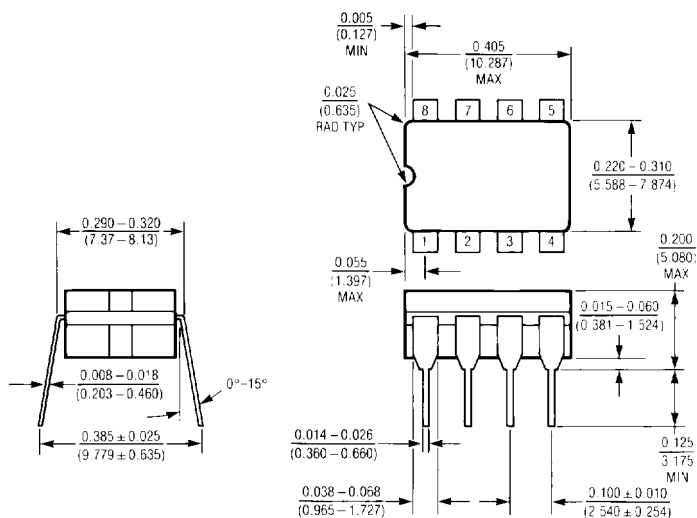


NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE

H8188

T_J max	θ_{JA}	θ_{JC}
150°C	150°C/W	45°C/W

J8 Package **8-Lead Ceramic DIP**



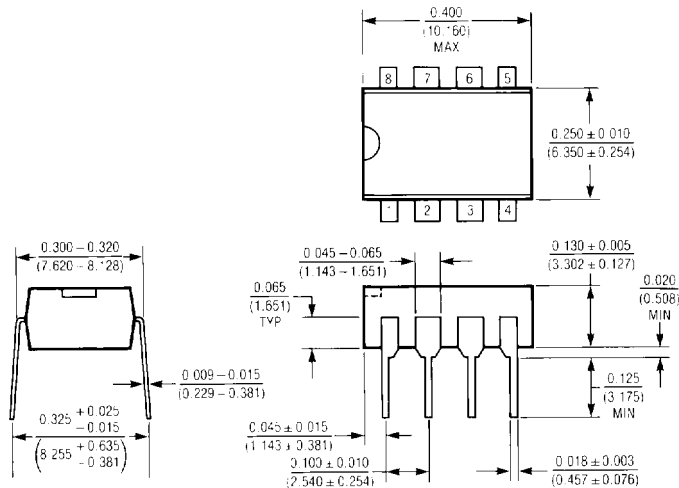
J8168

T_J max	θ_{JA}
150°C	100°C/W

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

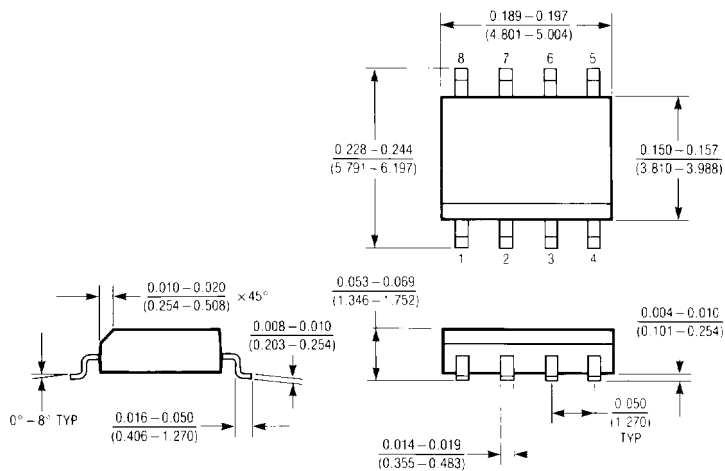
N8 Package 8-Lead Plastic DIP



NB188

T_J MAX	θ_{JA}
100°C	130°C/W

S8 Package 8-Lead Plastic SOIC



T_J MAX	θ_{JA}
100°C	120°C/W

NOTES

1. PKG MATERIAL: PLASTIC
2. LEAD MATERIAL: A-42, TIN PLATED

S8188