

74HC540-Q100; 74HCT540-Q100

Octal buffer/line driver; 3-state; inverting

Rev. 3 — 21 January 2013

Product data sheet

1. General description

The 74HC540-Q100; 74HCT540-Q100 is an 8-bit inverting buffer/line driver with 3-state outputs. The device features two output enables ($\overline{OE}1$ and $\overline{OE}2$). A HIGH on $\overline{OE}n$ causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Inverting outputs
- Complies with JEDEC standard no. 7A
- Input levels:
 - ◆ For 74HC540-Q100: CMOS level
 - ◆ For 74HCT540-Q100: TTL level
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- Multiple package options

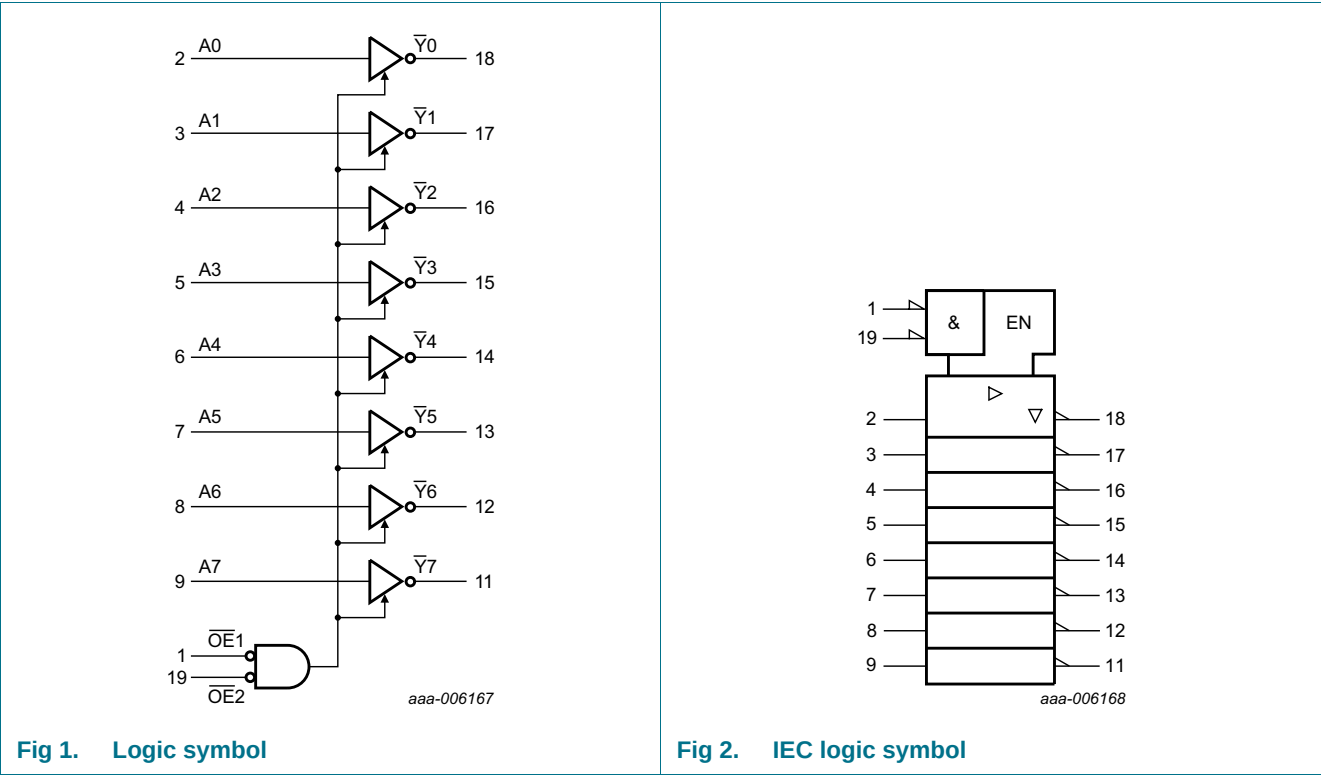
3. Ordering information

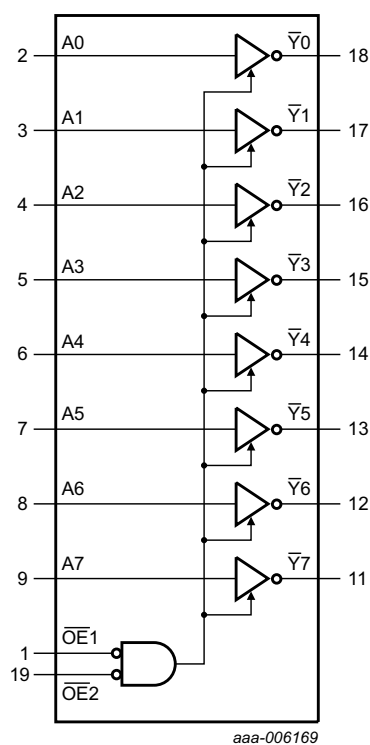
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC540N-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT540N-Q100				
74HC540D-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO20	plastic small outline package; 20 leads;	SOT163-1
74HCT540D-Q100			body width 7.5 mm	



4. Functional diagram



**Fig 3. Functional diagram**

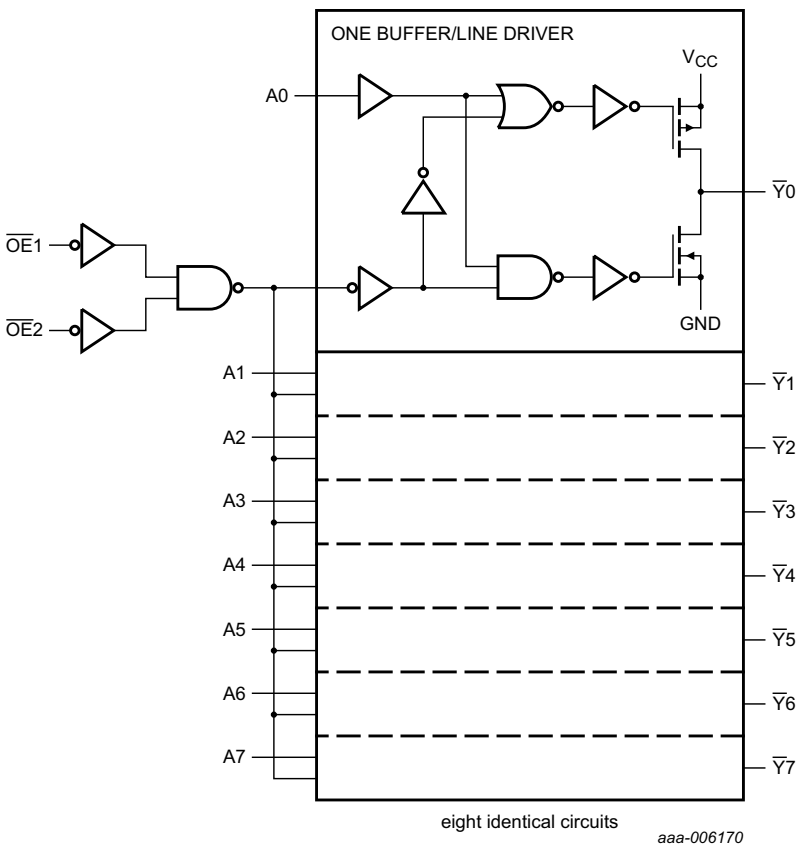
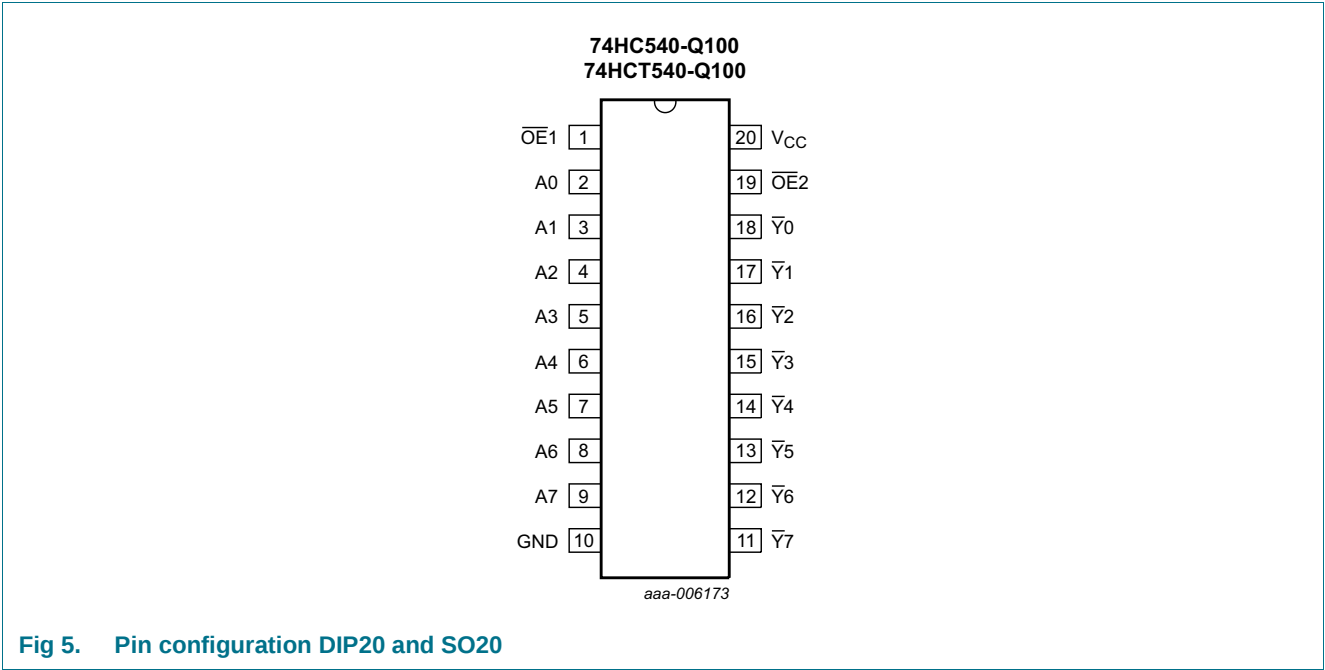


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{\text{OE1}}$	1	output enable input (active LOW)
A0 to A7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
$\overline{\text{Y0}}$ to $\overline{\text{Y7}}$	18, 17, 16, 15, 14, 13, 12, 11	data output
$\overline{\text{OE2}}$	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Functional table^[1]

Control		Input	Output
$\overline{\text{OE1}}$	$\overline{\text{OE2}}$	A _n	$\overline{\text{Yn}}$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	± 20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	± 35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation		[2]		
	DIP20		-	750	mW
	SO20		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP20 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
For SO20 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC540-Q100			74HCT540-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = –40 °C to +85 °C		T _{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC540-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = –20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = –20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = –6.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	I _O = –7.8 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
		V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	I _O = 7.8 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
		V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{OZ}	OFF-state output current	per input pin; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; V _{CC} = 6.0 V; I _O = 0 A	-	±0.5	-	±5.0	-	±10	-	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT540-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = –20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –6.0 mA	3.98	4.32	-	3.84	-	3.7	-	V

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = –40 °C to +85 °C		T _{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA;	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA;	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{OZ}	OFF-state output current	per input pin; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; V _{CC} = 5.5 V; I _O = 0 A	-	-	±0.5	-	±5.0	-	±10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	per input pin; I _O = 0 A; V _I = V _{CC} – 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		An input	-	140	504	-	630	-	686	µA
		$\overline{\text{OE}}1$ input	-	150	540	-	675	-	735	µA
		$\overline{\text{OE}}2$ input	-	100	360	-	450	-	490	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristicsGND = 0 V; C_L = 50 pF; for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	

74HC540-Q100

t _{pd}	propagation delay	An to Y _n ; see Figure 6						
		V _{CC} = 2.0 V	-	30	100	125	150	ns
		V _{CC} = 4.5 V	-	11	20	25	30	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	9	-	-	-	ns
		V _{CC} = 6.0 V	-	9	17	21	26	ns
t _{en}	enable time	$\overline{\text{OE}}n$ to Y _n ; see Figure 7						
		V _{CC} = 2.0 V	-	52	160	200	240	ns
		V _{CC} = 4.5 V	-	19	32	40	48	ns
		V _{CC} = 6.0 V	-	15	27	34	41	ns
t _{dis}	disable time	$\overline{\text{OE}}n$ to Y _n ; see Figure 7						
		V _{CC} = 2.0 V	-	61	160	200	240	ns
		V _{CC} = 4.5 V	-	22	32	40	48	ns
		V _{CC} = 6.0 V	-	18	27	34	41	ns

Table 7. Dynamic characteristicsGND = 0 V; $C_L = 50$ pF; for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	
t _t	transition time	see Figure 6 [2]						
		V _{CC} = 2.0 V	-	14	60	75	90	ns
		V _{CC} = 4.5 V	-	5	12	15	18	ns
		V _{CC} = 6.0 V	-	4	10	13	15	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} [3]	-	39	-	-	-	pF
74HCT540-Q100								
t _{pd}	propagation delay	An to Yn; see Figure 6 [1]						
		V _{CC} = 4.5 V	-	13	24	30	36	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	11	-	-	-	ns
t _{en}	enable time	$\overline{\text{OEn}}$ to Yn; see Figure 7 [1]						
		V _{CC} = 4.5 V	-	22	35	44	53	ns
t _{dis}	disable time	$\overline{\text{OEn}}$ to Yn; see Figure 7 [1]						
		V _{CC} = 4.5 V	-	23	35	44	53	ns
t _t	transition time	V _{CC} = 4.5 V; see Figure 6 [2]	-	5	12	15	18	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} – 1.5 V [3]	-	44	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

- [2] t_t is the same as t_{THL} and t_{TLH}.

- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms

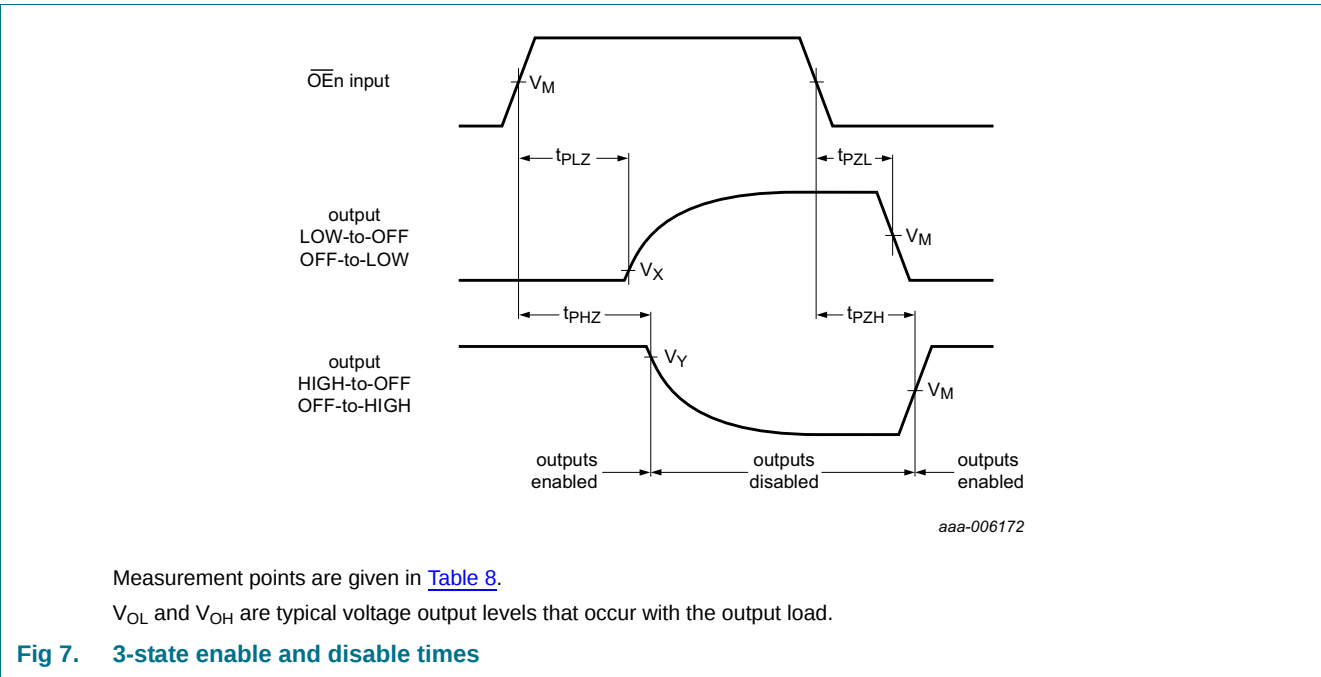
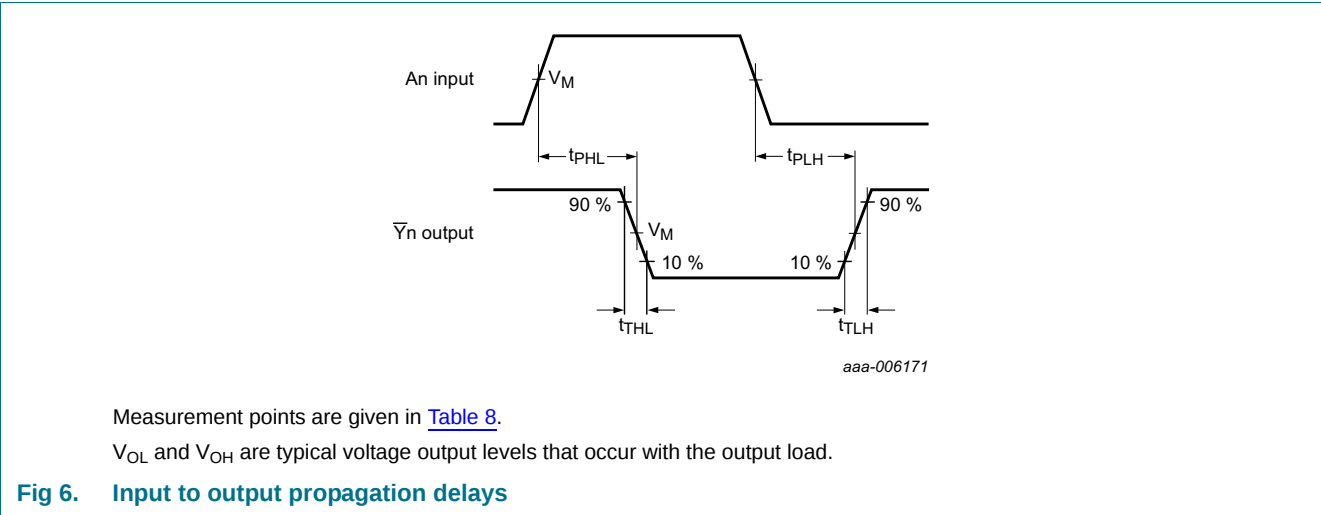


Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC540-Q100	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT540-Q100	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$

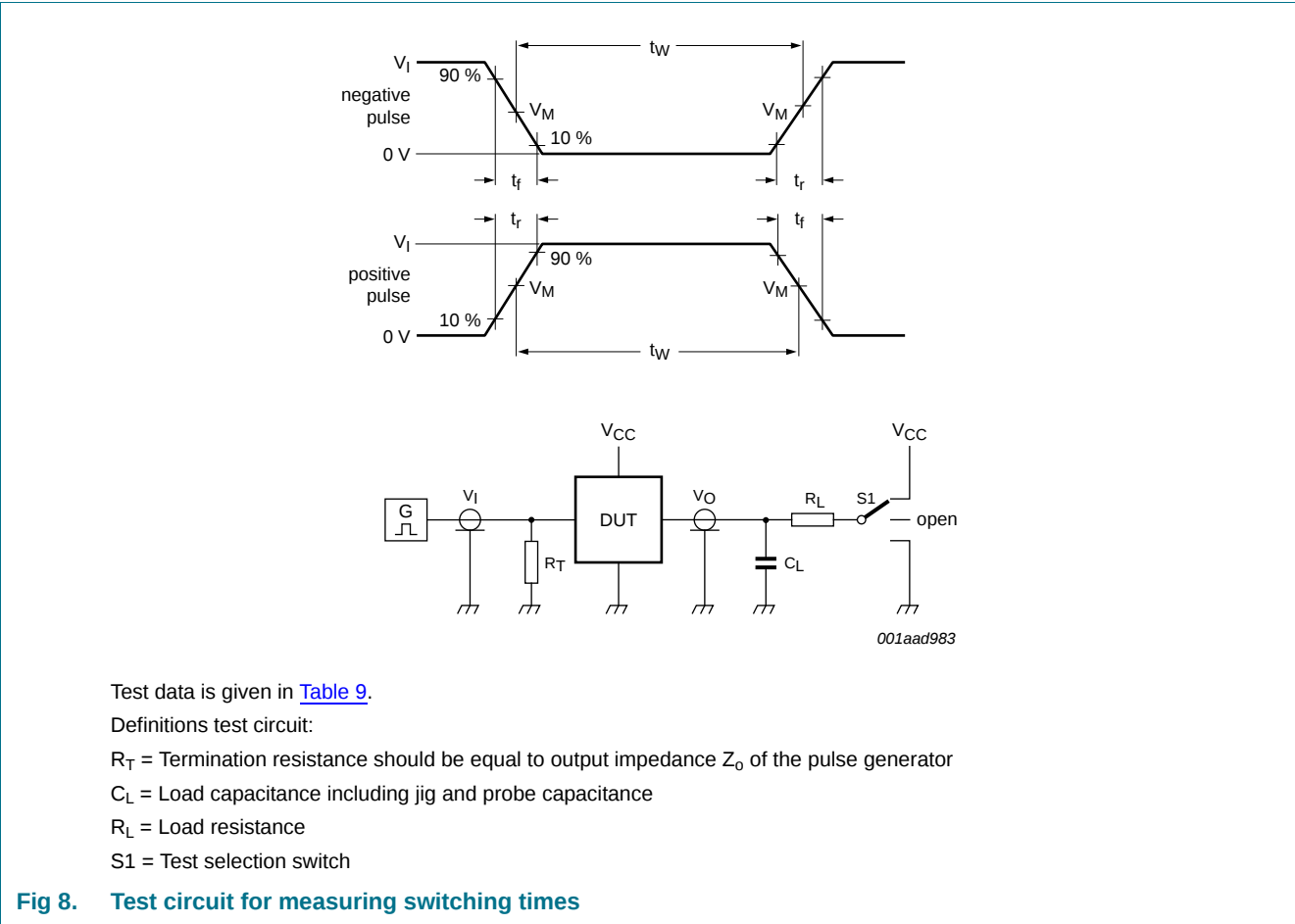


Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC540-Q100	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT540-Q100	3 V	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

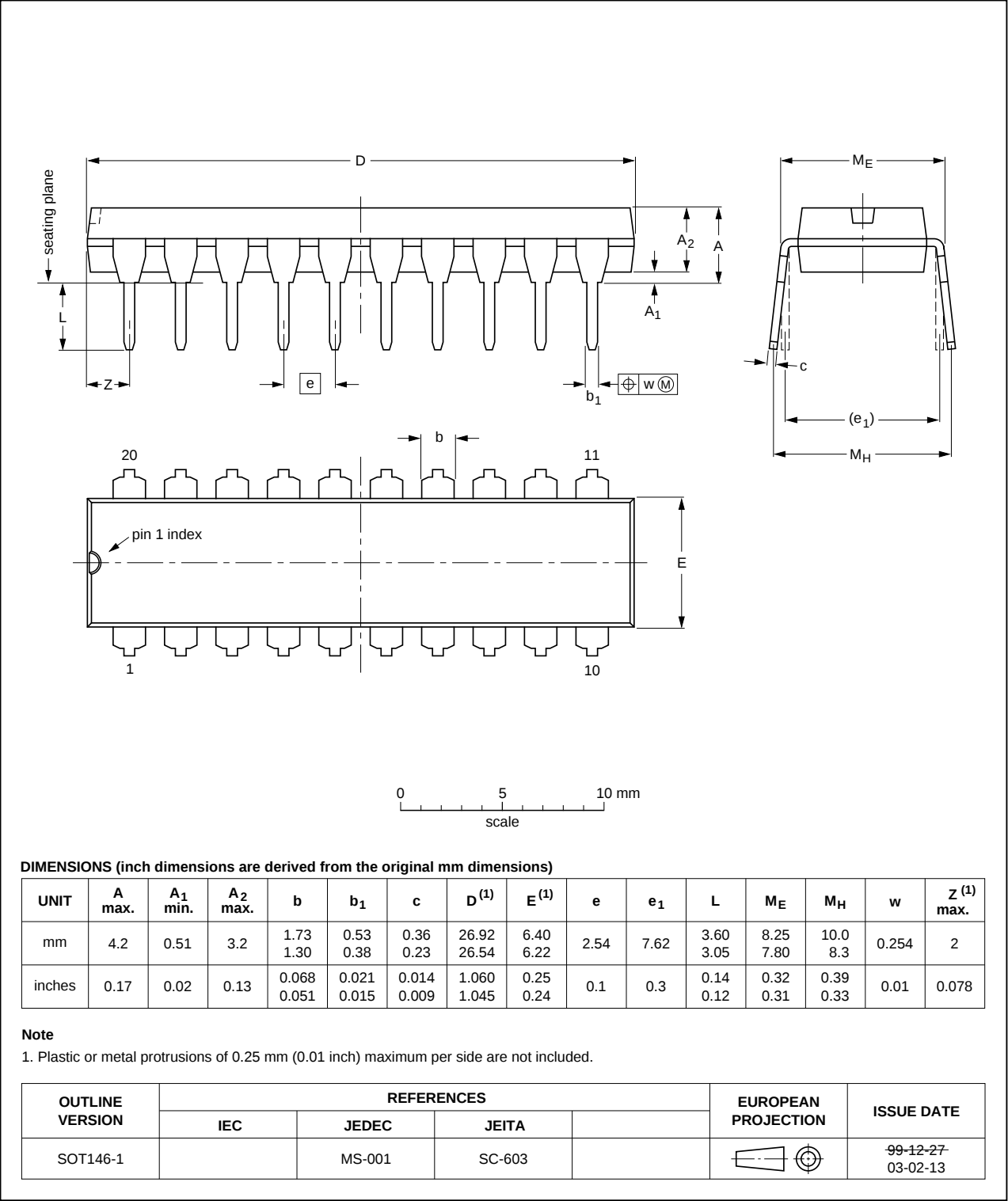


Fig 9. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

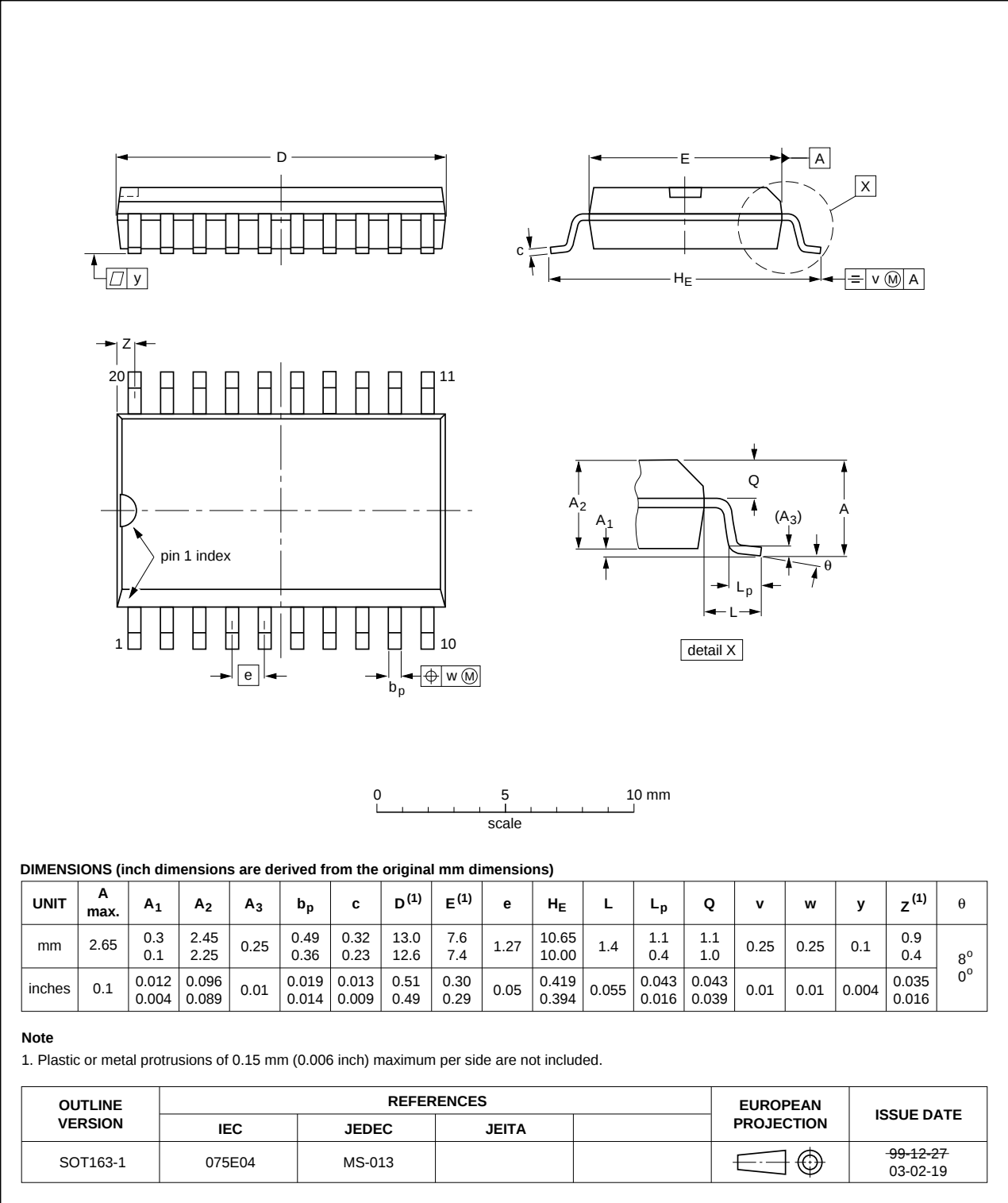


Fig 10. Package outline SOT163-1 (SO20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MIL	Military
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT540_Q100 v.1	20130121	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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