

SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

- Choice of Open-Collector or Active Pullup (Totem-Pole) Outputs
- Single 5-V Supply
- Differential Line Operation
- Dual-Channel Operation
- TTL Compatible
- ± 15 -V Common-Mode Input Voltage Range
- Optional-Use Built-In $130\text{-}\Omega$ Line-Terminating Resistor
- Individual Frequency-Response Controls
- Individual Channel Strobes
- Designed for Use With SN55113, SN75113, SN55114, and SN75114 Drivers
- Designed to Be Interchangeable With National DS9615 Line Receivers

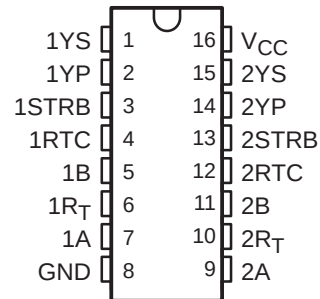
description

The SN55115 and SN75115 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the differential input voltage. The open-collector output configuration permits the wire-ANDing of similar TTL outputs (such as SN5401/SN7401) or other SN55115/SN75115 line receivers. This permits a level of logic to be implemented without extra delay.

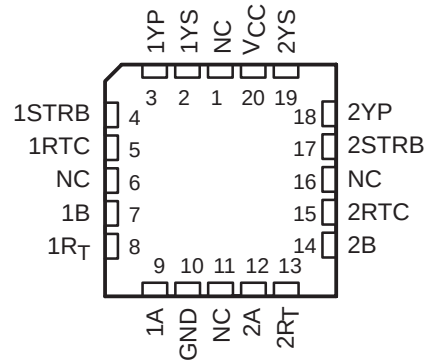
The output stages are similar to TTL totem-pole outputs, but with sink outputs, 1YS and 2YS, and the corresponding active pullup terminals, 1YP and 2YP, available on adjacent package pins. The frequency response and noise immunity may be provided by a single external capacitor. A strobe input is provided for each channel. With the strobe in the low level, the receiver is disabled and the outputs are forced to a high level.

The SN55115 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN75115 is characterized for operation from 0°C to 70°C .

SN55115 . . . J OR W PACKAGE
SN75115 . . . N PACKAGE
(TOP VIEW)



SN55114 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

STRB	DIFF INPUT (A AND B)	OUTPUT (YP AND YS TIED TOGETHER)
L	X	H
H	L	H
H	H	L

H = $V_I \geq V_{IH \text{ min}}$ or V_{ID} more positive than $V_T + \text{max}$

L = $V_I \leq V_{IL \text{ max}}$ or V_{ID} more negative than $V_T - \text{max}$

X = irrelevant



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

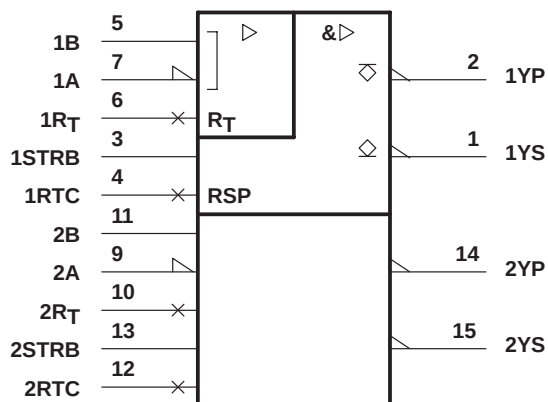
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SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

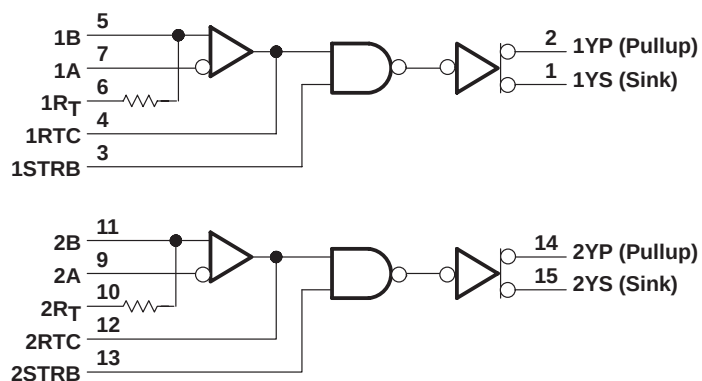
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logic symbol†

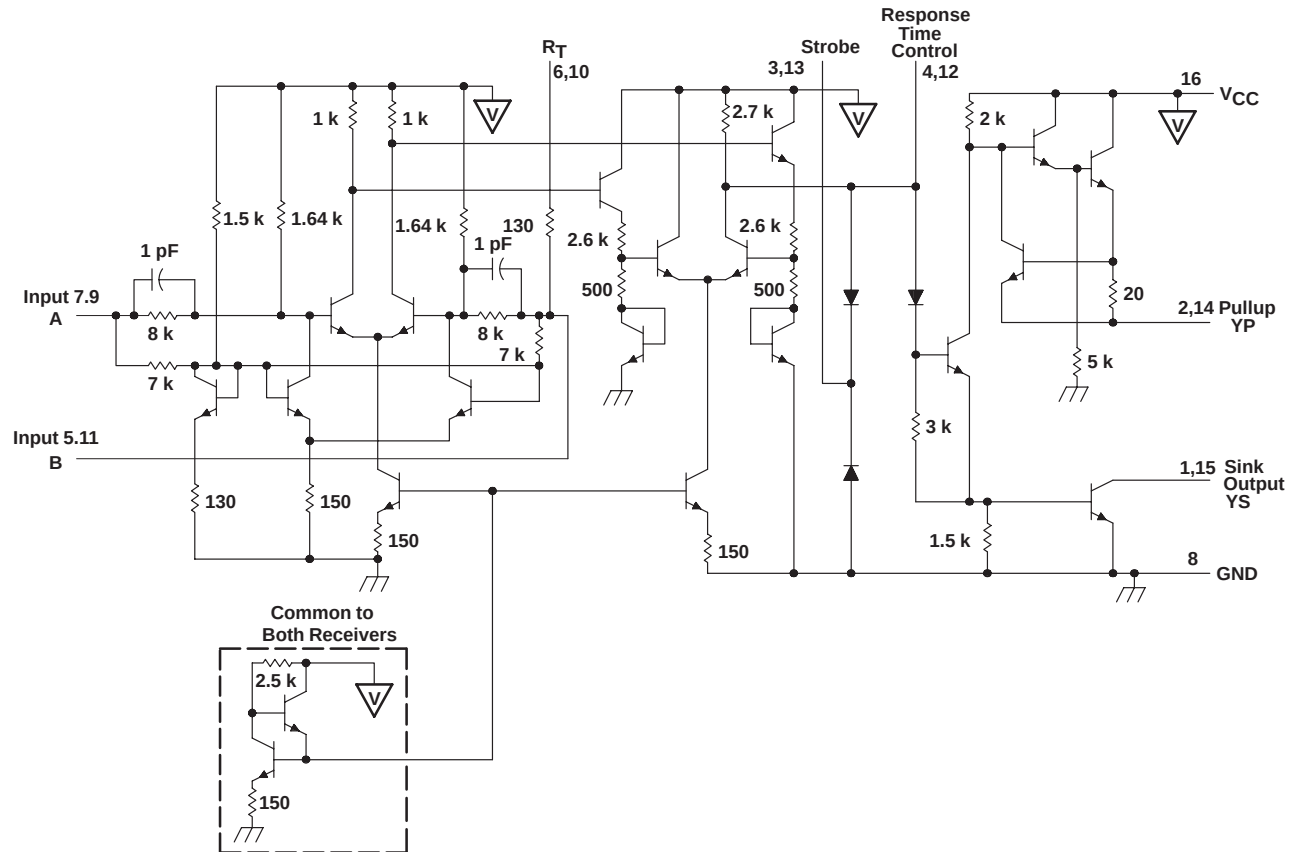


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



Resistor values are nominal and in ohms.
Pin numbers shown are for the J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage V_I (A, B, and R_T)	± 25 V
Input voltage V_I (STRB)	5.5 V
Off-state voltage applied to open-collector outputs	14 V
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T_{Stg}	-65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input voltage, are with respect to network ground terminal.

SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK [†]	1375 mW	11.0 mW/°C	880 mW	275 mW
J [†]	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W [†]	1000 mW	8.0 mW/°C	640 mW	200 mW

[†] In the FK, J, and W packages, SN55115 chips are either silver glass or alloy mounted. SN75115 chips are glass mounted.

recommended operating conditions

	SN55115			SN75115			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage at STRB, V_{IH}	2.4			2.4			V
Low-level input voltage at STRB, V_{IL}			0.4			0.4	V
High-level output current, I_{OH}			–5			–5	mA
Low-level output current, I_{OL}			15			15	mA
Operating free-air temperature, T_A	–55		125	0		70	°C



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SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN55115			SN75115			UNIT		
					MIN	TYP‡	MAX	MIN	TYP‡	MAX			
VIT+	§ Positive-going threshold voltage	VO = 0.4 V,	IOL = 15 mA,	VIC = 0	500			500			mV		
VIT-	§ Negative-going threshold voltage	VO = 2.4 V,	IOH = -5 mA,	VIC = 0	-500¶			-500¶			mV		
VICR	Common-mode input voltage range	VID = ±1 V			+15 to -15	+24 to -19		+15 to -15	+24 to -19		V		
VOH	High-level ouput voltage	VCC = MIN, IOH = -5 mA	VID = -0.5 V,	TA = MIN	2.2		2.4				V		
				TA = 25°C	2.4	3.4	2.4	3.4					
				TA = MAX	2.4		2.4						
VOL	Low-level output voltage	VCC = MIN, IOL = 15 mA	VID = -0.5 V,		0.22		0.4	0.22		0.45	V		
IIL	Low-level input current	VCC = MAX, Other input at 5.5 V	VI = 0.4 V,	TA = MIN	-0.9		-0.9				mA		
				TA = 25°C	-0.5	-0.7	-0.5	-0.7					
				TA = MAX	-0.7		-0.7						
ISH	High-level strobe current	VCC = MIN, Vstrobe = 4.5 V	VID = -0.5 V,	TA = 25°C	2		5				µA		
				TA = MAX	5		10						
ISL	Low-level strobe current	VCC = MAX, Vstrobe = 0.4 V	VID = 0.5 V,		TA = 25°C		-1.15	-2.4	-1.15	-2.4	mA		
I(RTC)	Response-time-control current	VCC = MAX, VRC = 0	VID = 0.5 V,		TA = 25°C		-1.2	-3.4	-1.2	-3.4	mA		
IO(off)	Off-state open-collector output current	VCC = MIN, VID = -4.5 V	VOH = 12 V,	TA = 25°C	100						µA		
				TA = MAX	200								
		VCC = MIN, VID = -4.75 V	VOH = 5.25 V,	TA = 25°C			100						
				TA = MAX			200						
RT	Line-terminating resistance	VCC = 5 V		TA = 25°C	77	130	167	74	130	179	Ω		
IOS	Supply-circuit output current#	VCC = MAX, VO = 0	VID = -0.5 V,		TA = 25°C		-15	-40	-80	-14	-40	-100	mA
ICC	Supply current (both receivers)	VCC = MAX, VIC = 0	VID = 0.5 V,		TA = 25°C		32		50	32		50	mA

[†] Unless otherwise noted, $V_{\text{strobe}} = 2.4 \text{ V}$. All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, and $V_{IC} = 0$.

§ Differential voltages are at the B input terminal with respect to the A input terminal.

[¶] The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

[#] Only one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

SN55115, SN75115

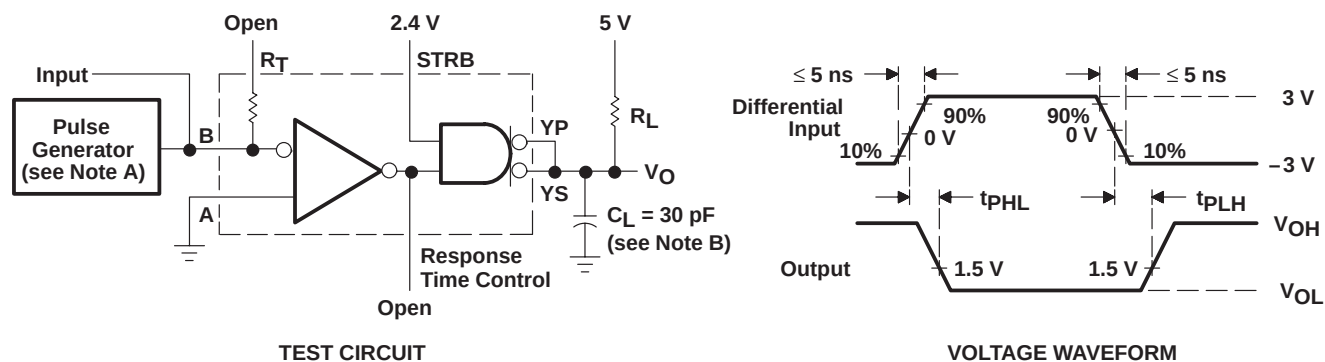
DUAL DIFFERENTIAL RECEIVERS

SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 30\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	SN55115			SN75115			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Propagation delay time, low-to-high level output	R _L = 3.9 kΩ, See Figure 1		18	50		18	75	ns
t _{PHL}	Propagation delay time, high-to-low level output	R _L = 390 Ω, See Figure 1		20	50		20	75	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \, \Omega$, $PRR \leq 500 \, \text{kHz}$, $t_W \leq 100 \, \text{ns}$, duty cycle = 50%.
B. C_l includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

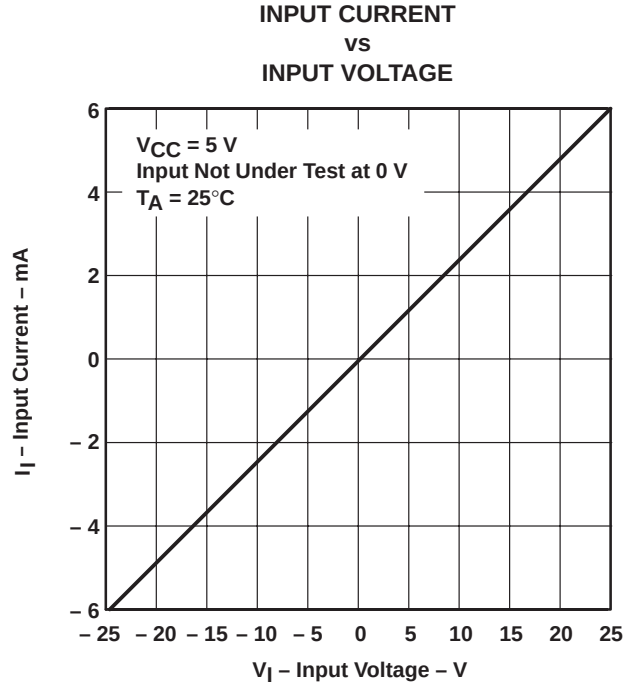


Figure 2

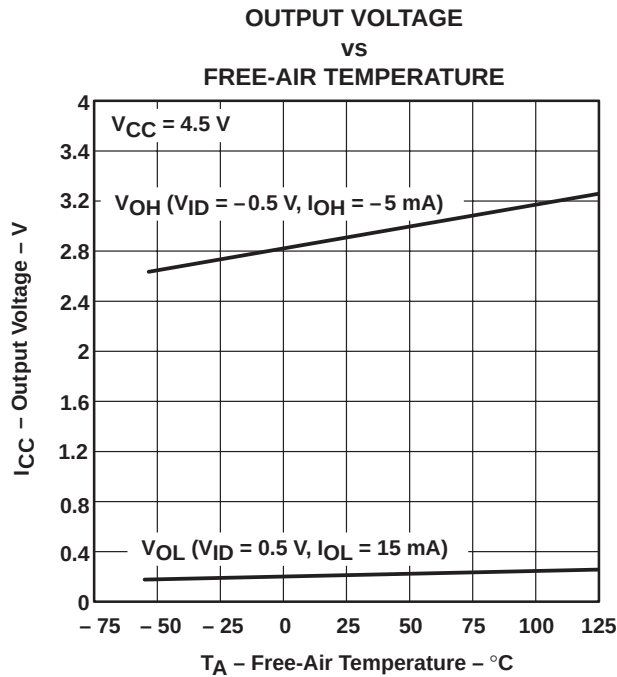


Figure 3

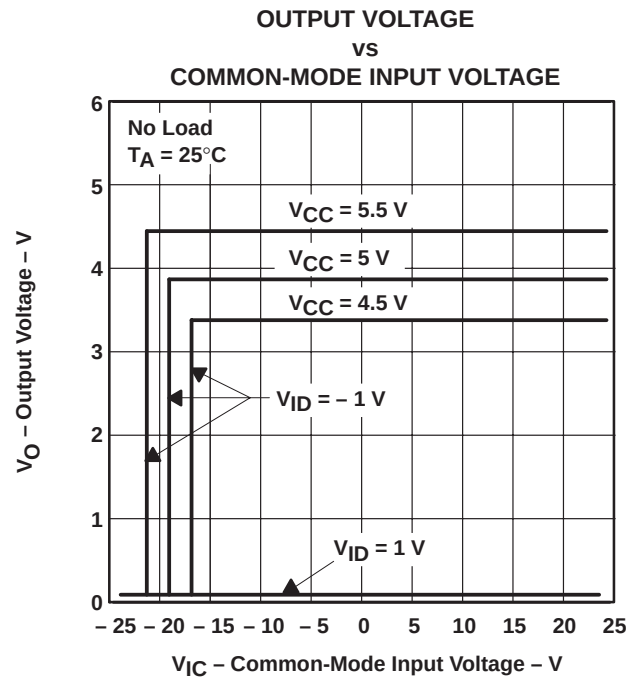


Figure 4

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

SN55115, SN75115
DUAL DIFFERENTIAL RECEIVERS

SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

TYPICAL CHARACTERISTICS

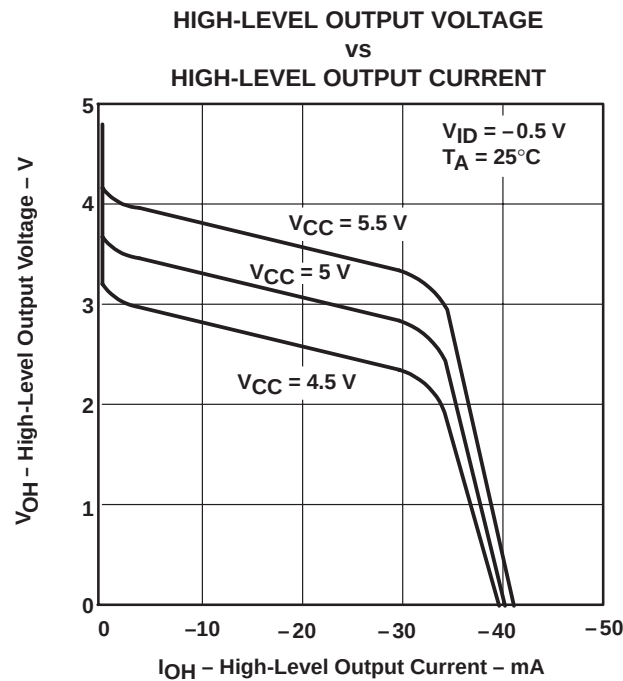


Figure 5

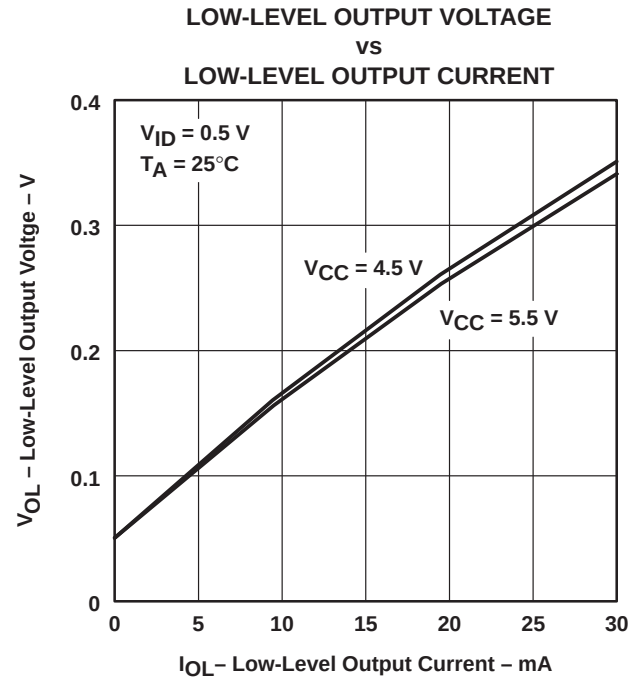


Figure 6

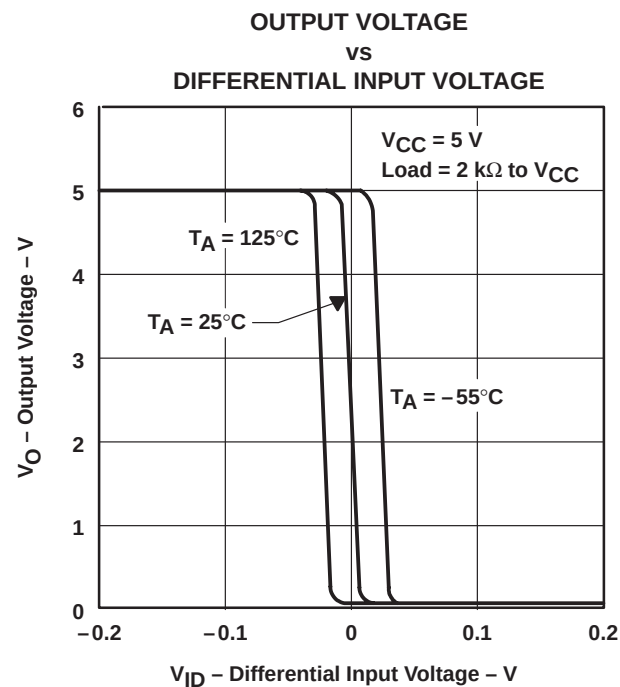


Figure 7

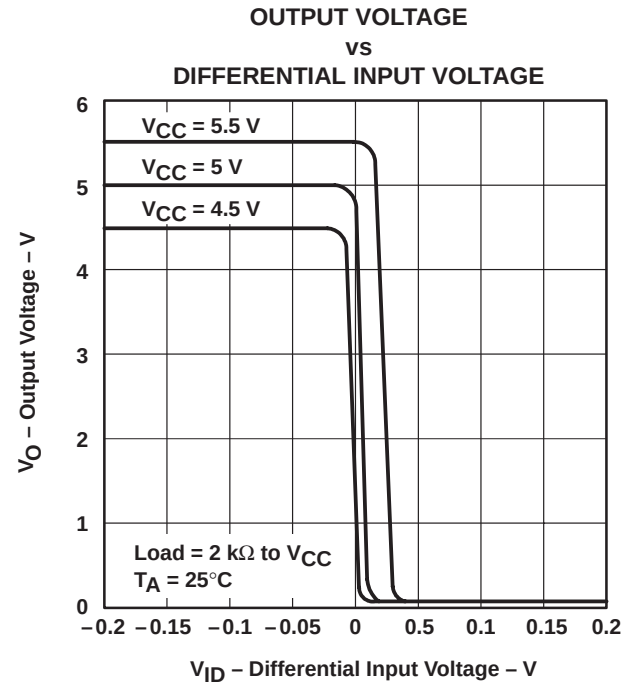


Figure 8

TYPICAL CHARACTERISTICS†

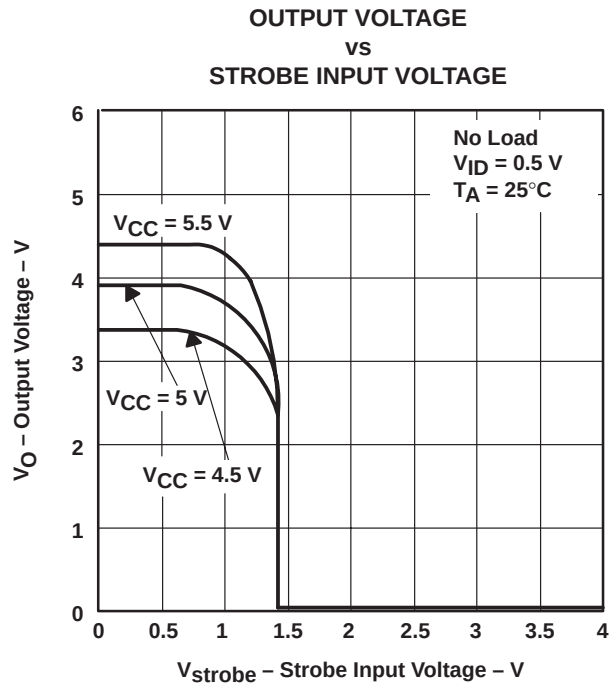


Figure 9

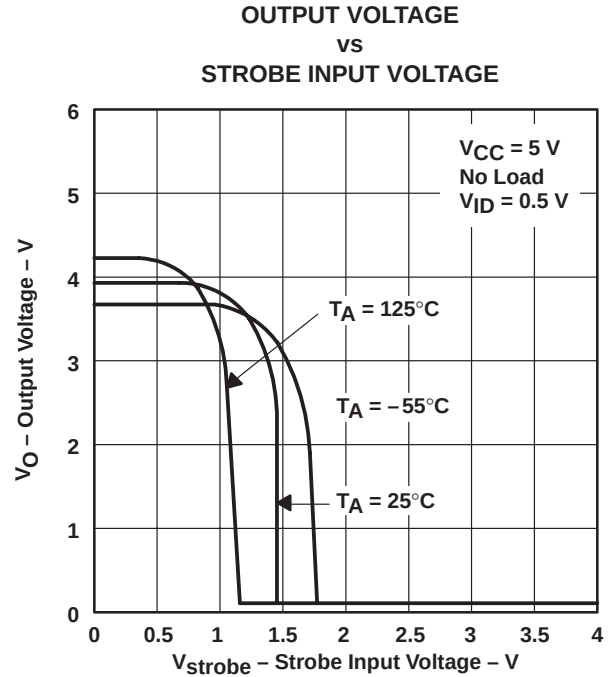


Figure 10

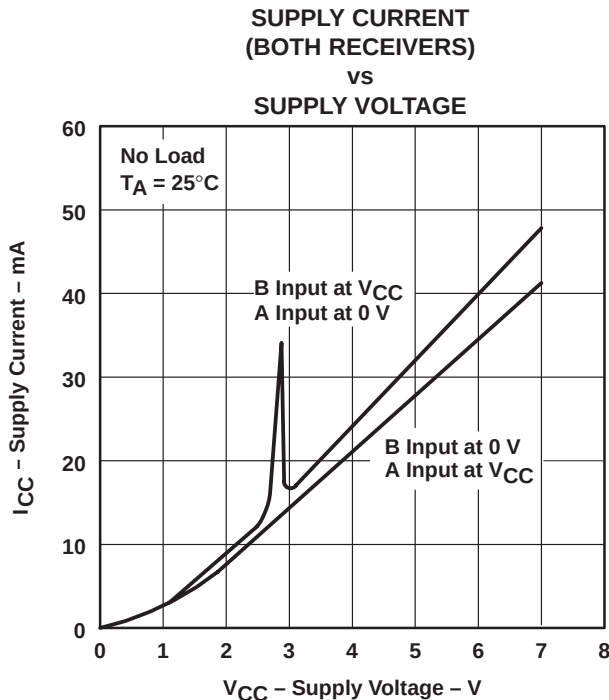


Figure 11

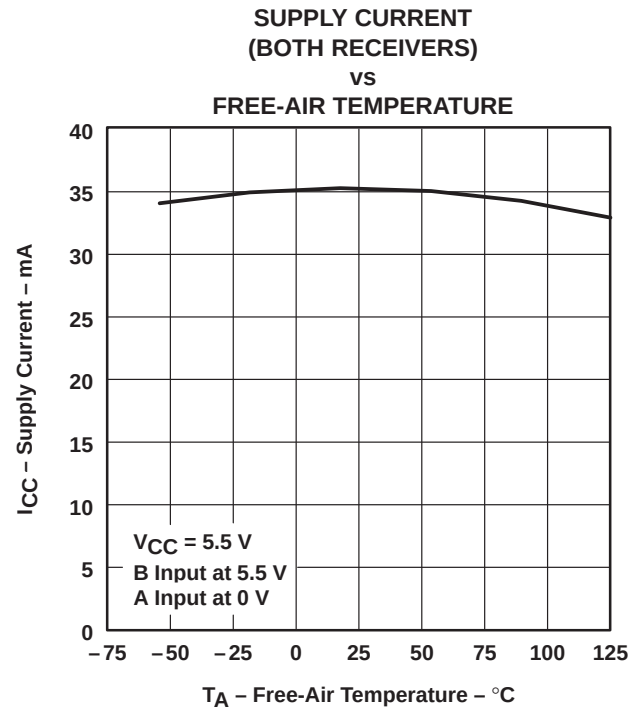


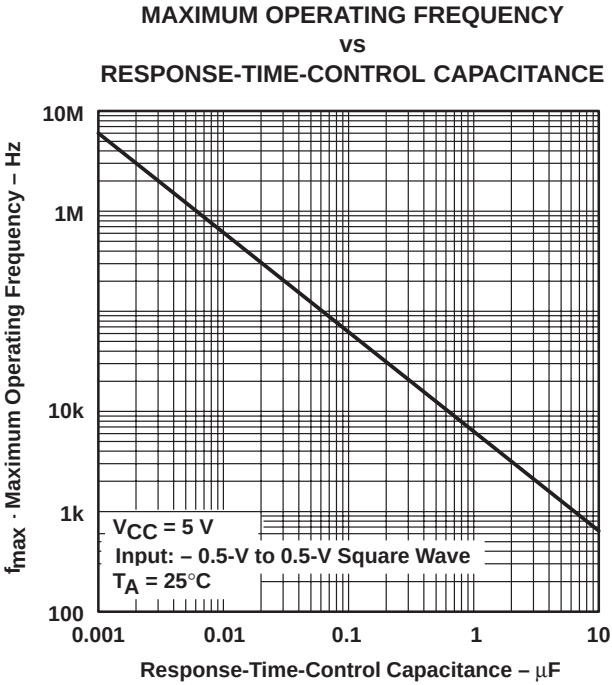
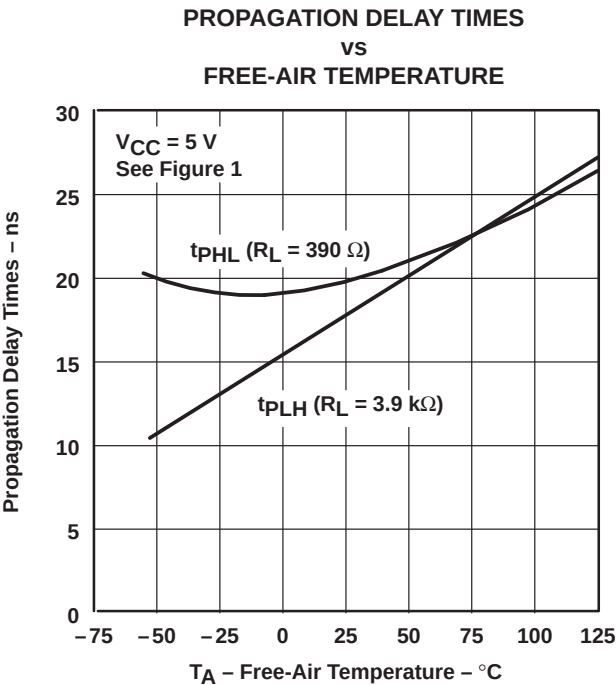
Figure 12

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

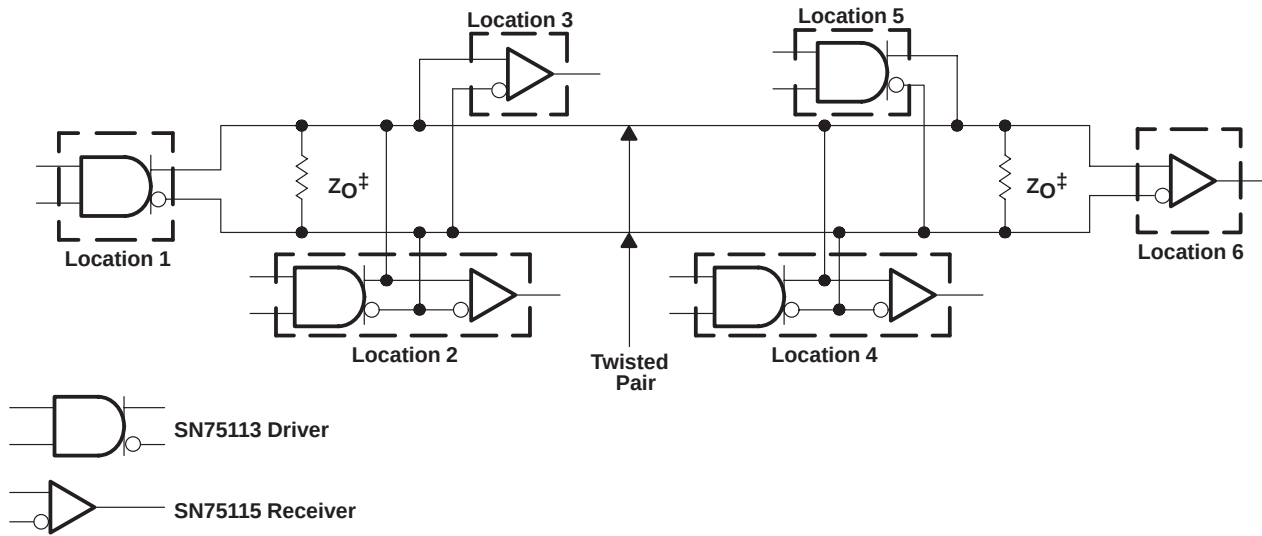
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TYPICAL CHARACTERISTICS†



† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

APPLICATION INFORMATION



‡ $Z_O = R_T$. A capacitor may be connected in series with Z_O to reduce power dissipation.

Figure 15. Basic Party-Line or Data-Bus Differential Data Transmission

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88745012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 88745012A SNJ55 115FK	Samples
5962-88745012A-T	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 88745012A SNJ55115FK	Samples
5962-8874501FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8874501FA SNJ55115W	Samples
JM38510/10404BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /10404BEA	Samples
M38510/10404BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /10404BEA	Samples
SN55115J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55115J	Samples
SN75115D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75115	Samples
SN75115DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75115	Samples
SN75115DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75115	Samples
SN75115DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75115	Samples
SN75115DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75115	Samples
SN75115DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75115	Samples
SN75115N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75115N	Samples
SN75115NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75115N	Samples
SN75115NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75115	Samples
SN75115NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75115	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75115NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75115	Samples
SNJ55115FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 88745012A SNJ55 115FK	Samples
SNJ55115J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ55115J	Samples
SNJ55115W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8874501FA SNJ55115W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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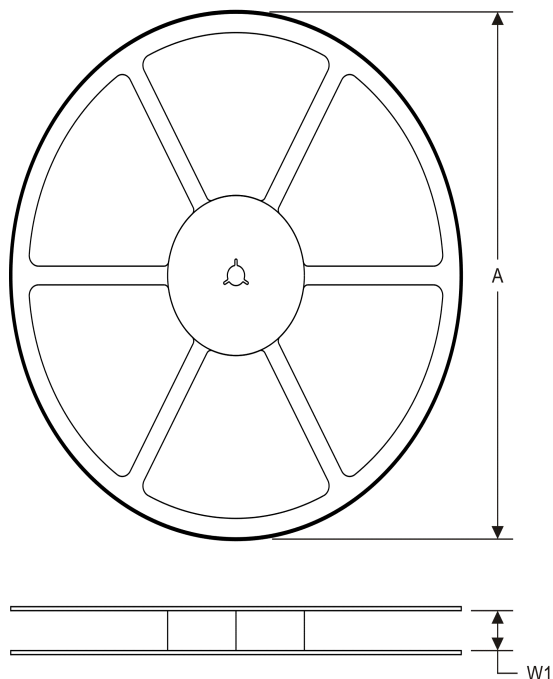
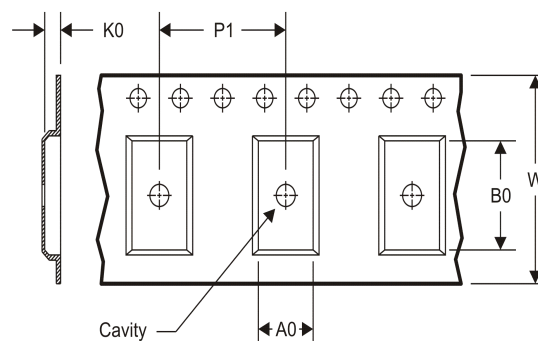
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OTHER QUALIFIED VERSIONS OF SN55115, SN75115 :

- Catalog: [SN75115](#)
- Military: [SN55115](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


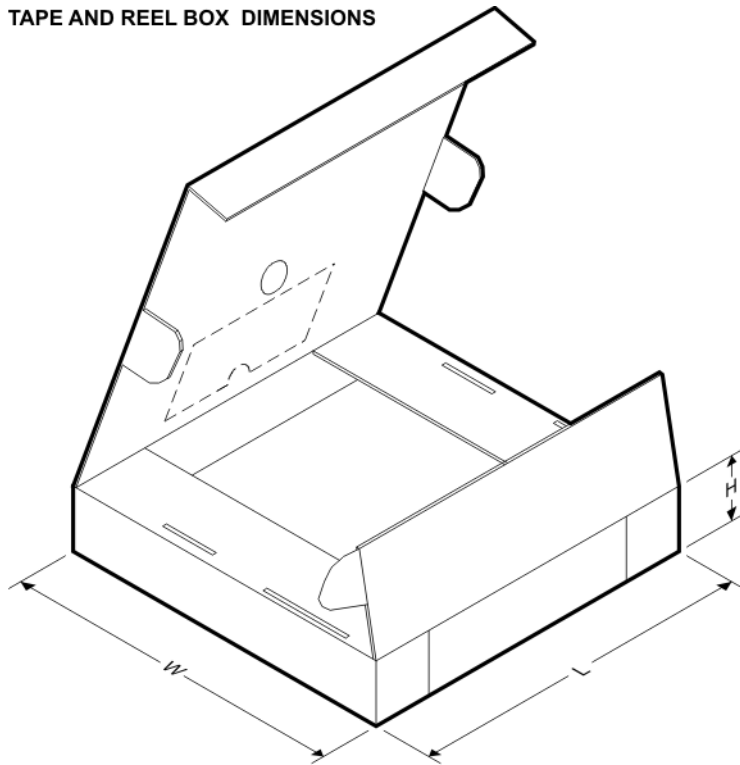
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75115DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75115NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



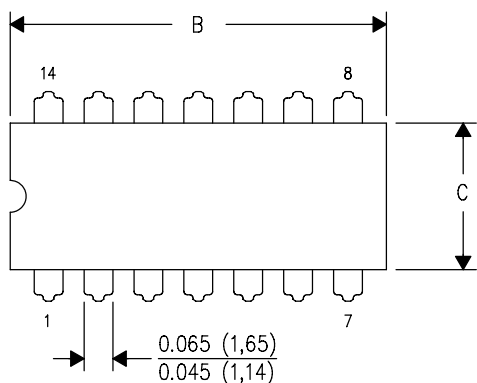
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75115DR	SOIC	D	16	2500	333.2	345.9	28.6
SN75115NSR	SO	NS	16	2000	367.0	367.0	38.0

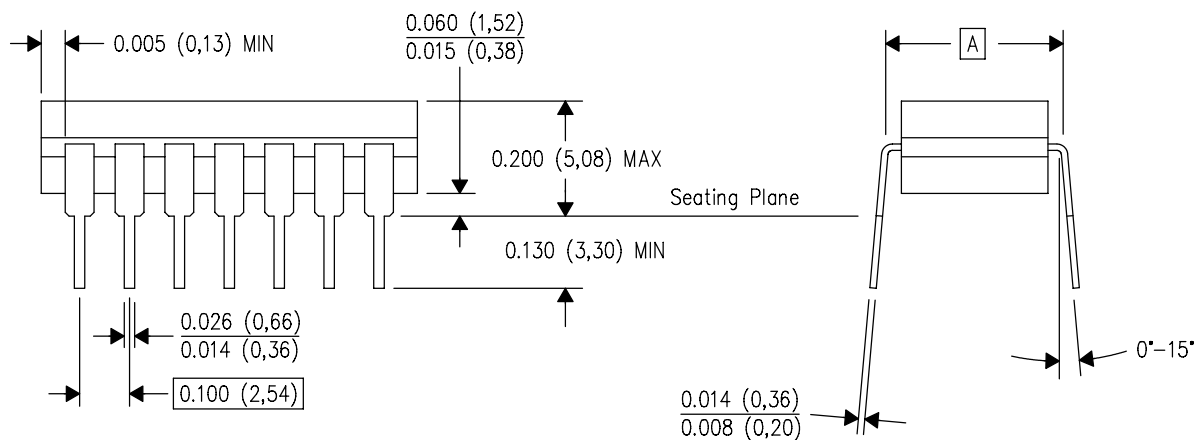
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

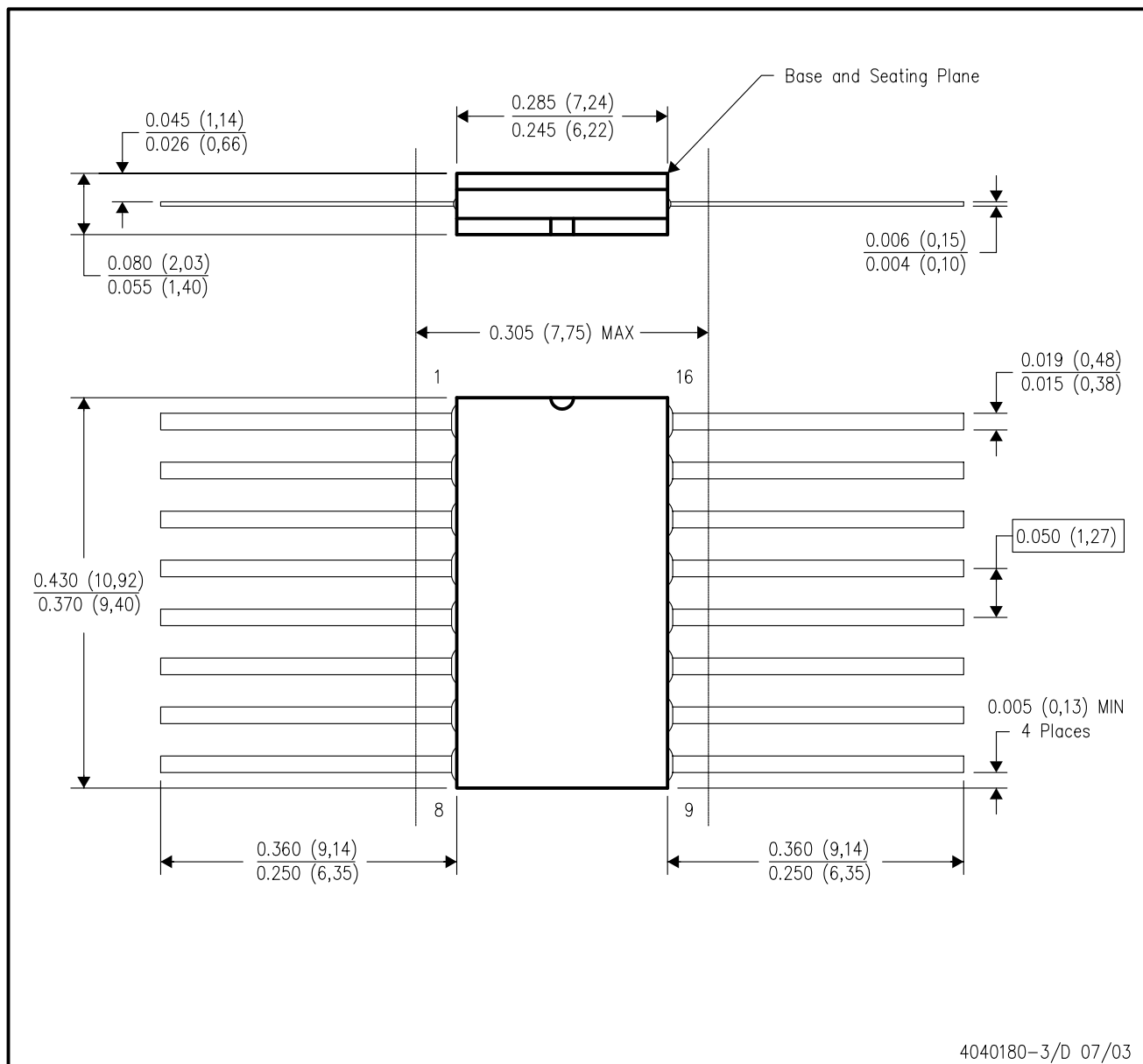


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

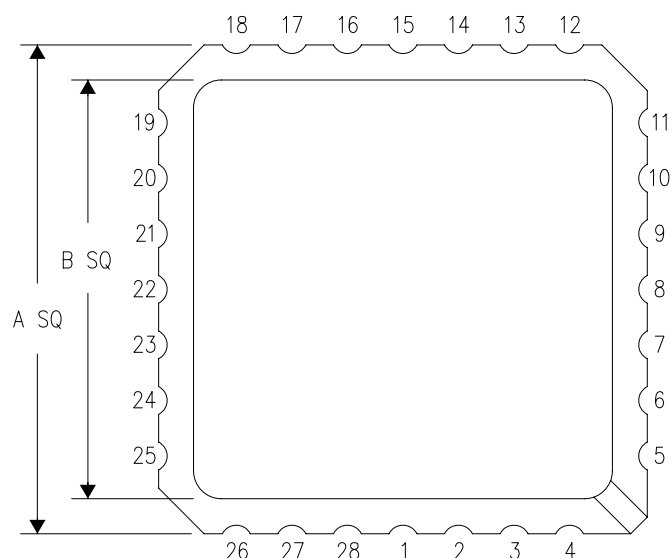


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

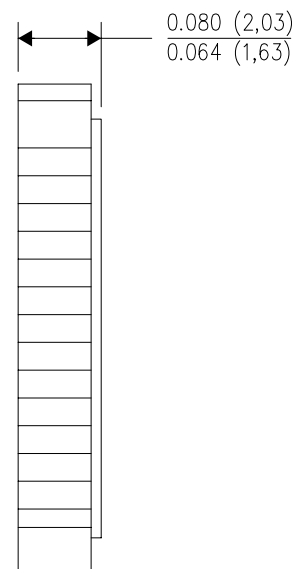
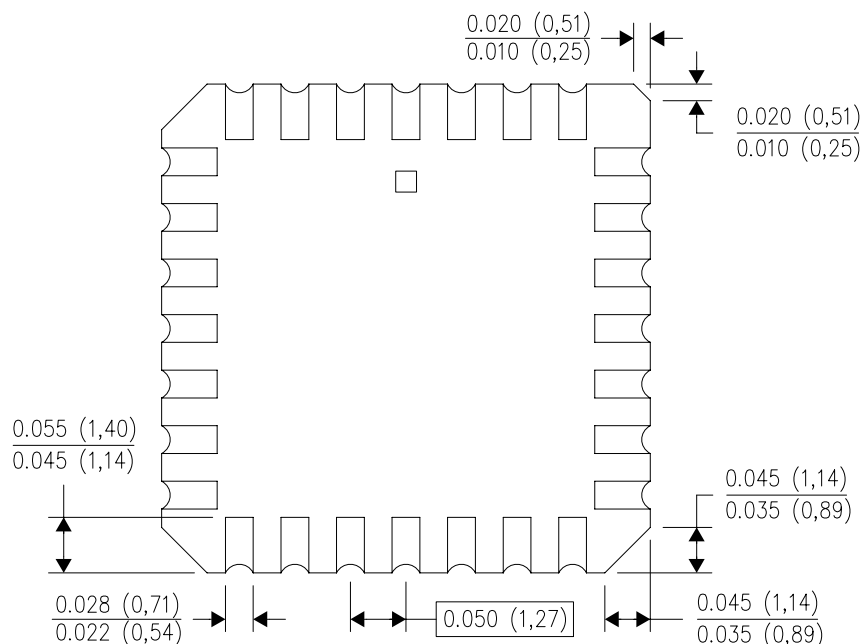
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



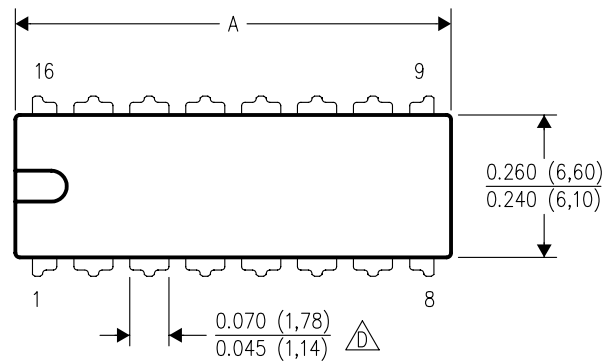
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

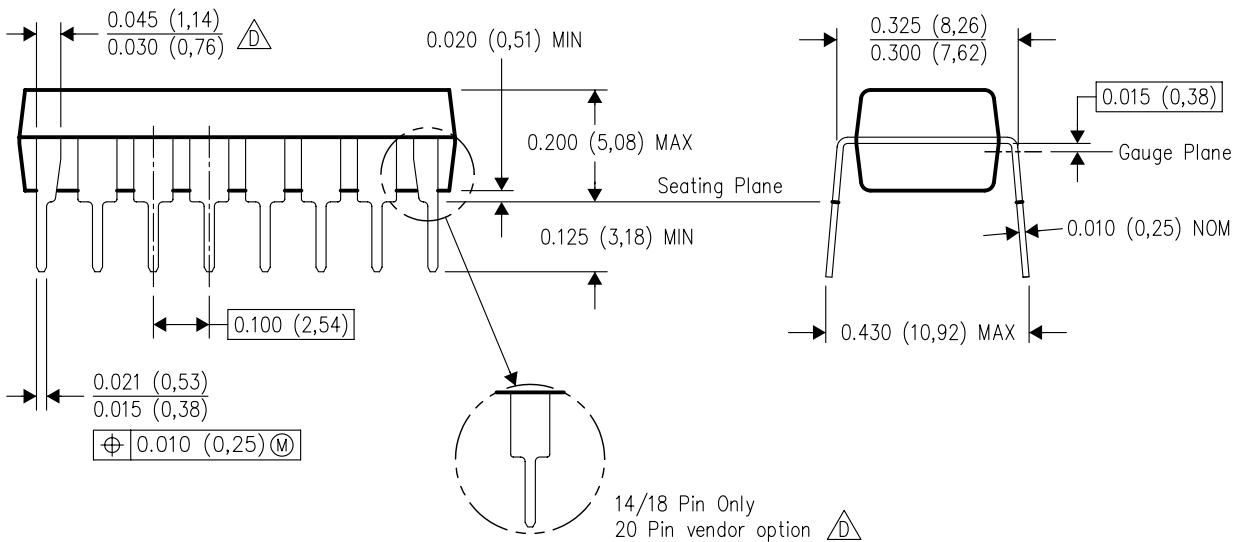
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

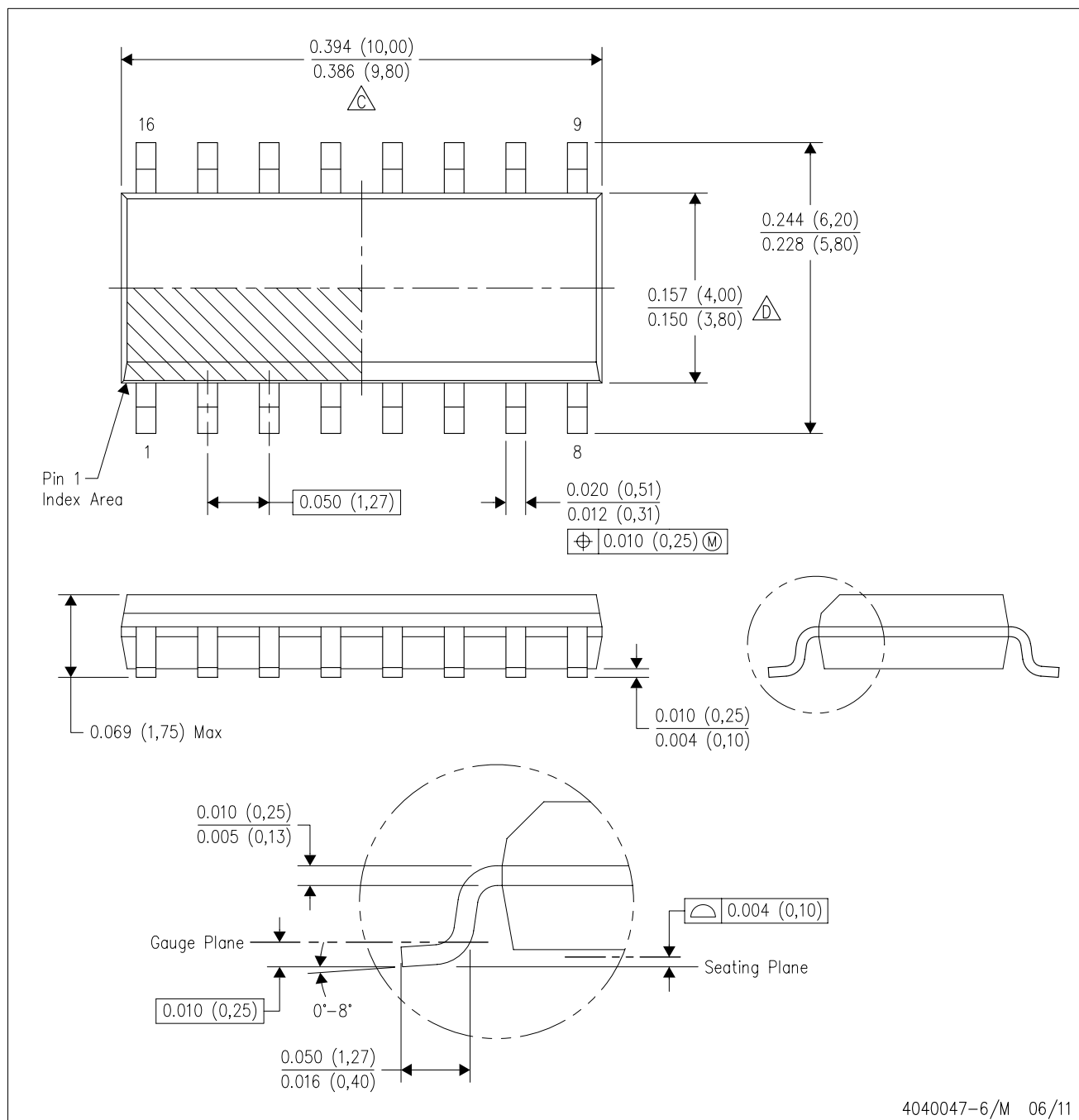


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

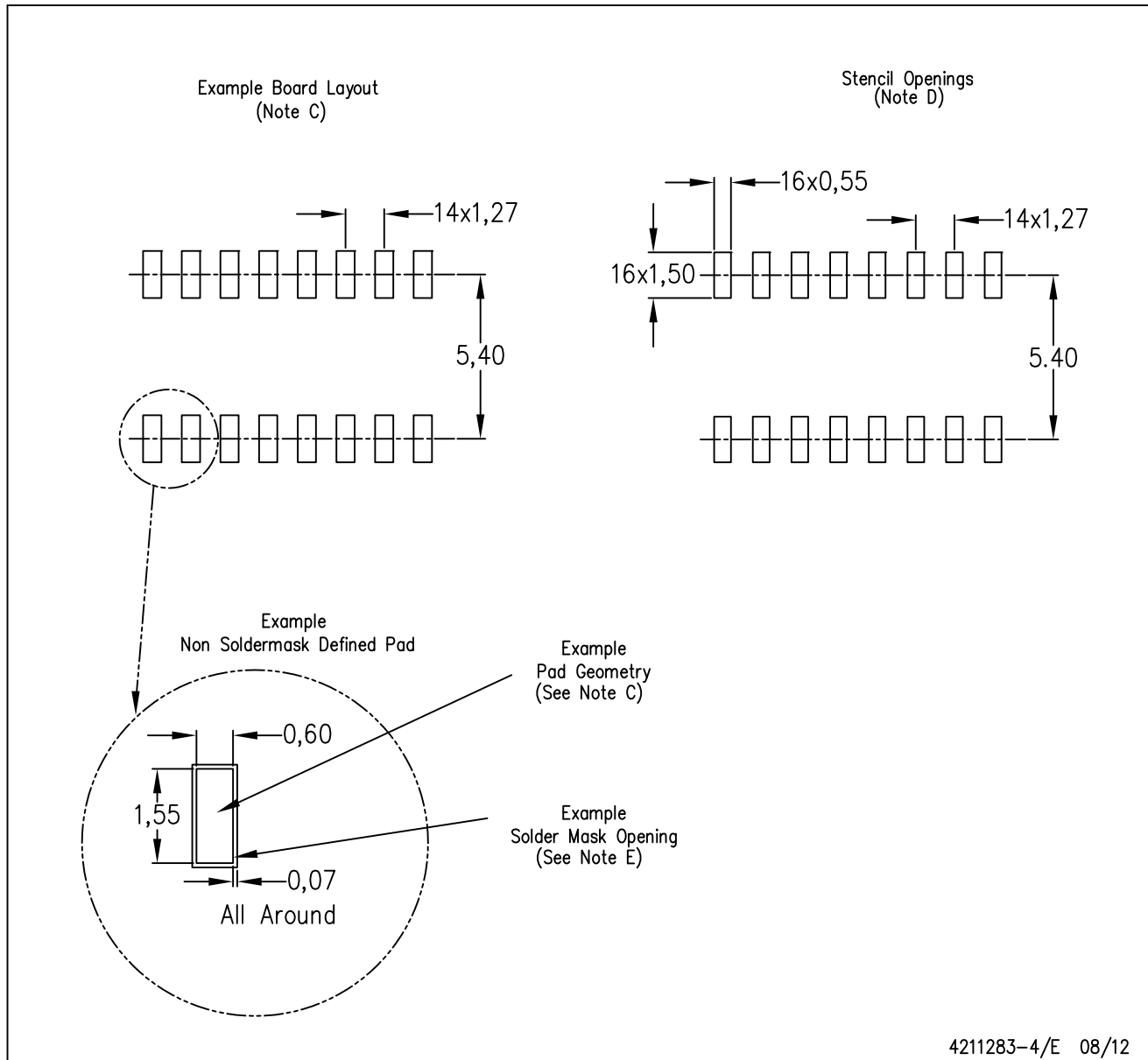
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



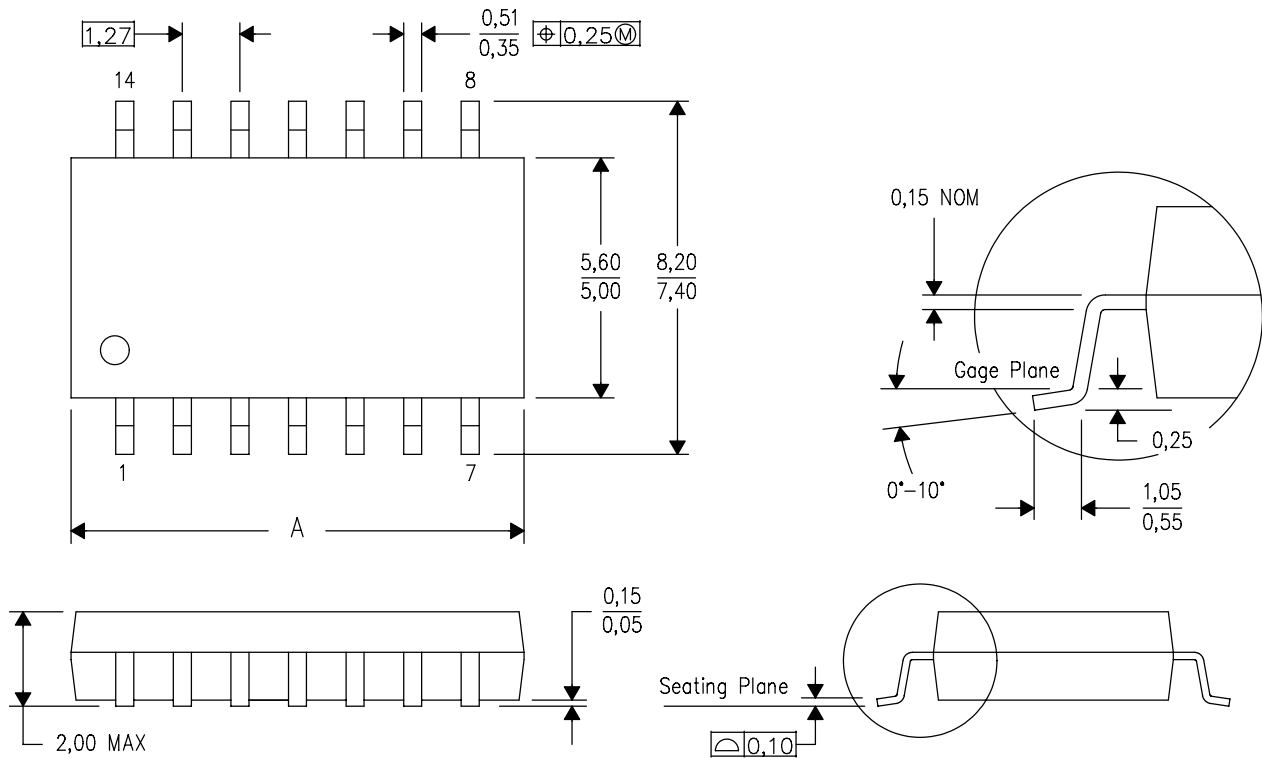
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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