Numbers in parenthesis denote pin numbers for F package (Case 650).



**FUNCTIONS AND CHARACTERISTICS** (continued)

| Function | Type ① | | Propagation Delay ns typ | Power Dissipation mW typ/pkg* | Case |
|---|---|---|---|---|---|
| | -30 to +85°C | -55 to +125°C | | | |
| Universal Decade Counter | MC10137 | MC10537 | f = 150 MHz | 625 | 620,650 |
| Bi-Quinary Counter | MC10138 | – | f = 150 MHz | 370 | 620 |
| 64-Bit Random Access Memory (90 Ω) | MCM10140 | – | $t_{Access}$ = 15 (max) | 420 | 620,690 |
| Four-Bit Universal Shift Register | MC10141 | MC10541 | f = 200 MHz | 425 | 620,648,650 |
| 64-Bit Random Access Memory (50 Ω) | MCM10142 | – | $t_{Access}$ = 10 (max) | 420 | 620 |
| 8 x 2 Multiport Register File (RAM) | MCM10143 | – | $t_{Access}$ = 10 | 610 | 623 |
| 256-Bit Random Access Memory | MCM10144 | – | $t_{Access}$ = 30 (max) | 420 | 620,690 |
| 64-Bit Register File (RAM) | MCM10145 | – | $t_{Access}$ = 10 | 625 | 620 |
| 128-Bit Random Access Memory | MCM10147 | – | $t_{Access}$ = 12 (max) | 420 | 620 |
| 64-Bit Random Access Memory (50 Ω) | MCM10148 | – | $t_{Access}$ = 15 (max) | 420 | 620 |
| 1024-Bit Programmable Read Only Memory | MCM10150 | – | $t_{Access}$ = 20 | – | 690 |
| Quad Latch | MC10153 | – | 4.0 | 310 | 620 |
| 12-Bit Parity Generator-Checker | MC10160 | MC10560 | 5.0 | 320 | 620,648,650 |
| Binary to 1-8 Decoder (Low) | MC10161 | MC10561 | 4.0 | 315 | 620,648,650 |
| Binary to 1-8 Decoder (High) | MC10162 | MC10562 | 4.0 | 315 | 620,648,650 |
| Error Detection-Correction Circuit | MC10163 | – | 5.0 | 520 | 620 |
| 8-Line Multiplexer | MC10164 | MC10564 | 3.0 | 310 | 620,648,650 |
| 8-Input Priority Encoder | MC10165 | – | 7.0 | 545 | 620,648 |
| 5-Bit Magnitude Comparator | MC10166 | – | 6.0 | 440 | 620 |
| Quad Latch | MC10168 | – | 3.0 | 310 | 620 |
| Dual Binary To 1-4 Decoder (Low) | MC10171 | MC10571 | 4.0 | 325 | 620,648,650 |
| Dual Binary To 1-4 Decoder (High) | MC10172 | MC10572 | 4.0 | 325 | 620,648,650 |
| Quad 2-Input Multiplexer/Latch | MC10173 | – | 2.5 | 275 | 620,648 |
| Dual 4 To 1 Multiplexer | MC10174 | MC10574 | 3.5 | 305 | 620,650 |
| Quint Latch | MC10175 | MC10575 | 2.5 | 400 | 620 |
| Hex "D" Master-Slave Flip-Flop | MC10176 | – | f = 250 MHz | 460 | 620 |
| Triple MECL to NMOS Translator | MC10177 | – | – | 1.0 W | 620 |
| Binary Counter | MC10178 | – | f = 150 MHz | 370 | 620 |
| Look-Ahead Carry Block | MC10179 | MC10579 | 3.0 (Cn,P) 4.0 (G) | 300 | 620,648,650 |
| Dual High Speed Adder/Subtractor | MC10180 | MC10580 | 4.5 | 360 | 620,648,650 |
| 4-Bit Arithmetic Logic Unit/Function Generator | MC10181 | MC10581 | See Logic Diag. | 600 | 623,649,652 |
| 2-Bit Arithmetic Logic Unit/Function Generator | MC10182 | – | See Logic Diag. | 575 | 620 |
| Error Detection-Correction Circuit | MC10193 | – | 7.5 | 520 | 620 |
| Hex Inverter/Buffer | MC10195 | – | 2.0 | 200 | 620 |
| Hex "AND" Gate | MC10197 | – | 2.8 | 200 | 620 |
| High Speed Dual 3-Input 3-Output OR Gate | MC10210 | – | 1.5 | 160 | 620 |
| High Speed Dual 3-Input 3-Output NOR Gate | MC10211 | – | 1.5 | 160 | 620 |
| High Speed Dual 3-Input 3-Output OR/NOR Gate | MC10212 | – | 1.5 | 160 | 620 |
| High Speed Triple Line Receiver | MC10216 | MC10616 | 1.8 | 100 | 620,648,650 |
| High Speed Dual Type D Master-Slave Flip-Flop | MC10231 | MC10631 | f = 225 MHz | 270 | 620,648,650 |
| High Speed 2 x 1 Bit Array Multiplier Block | MC10287 | – | – | 400 | 620 |

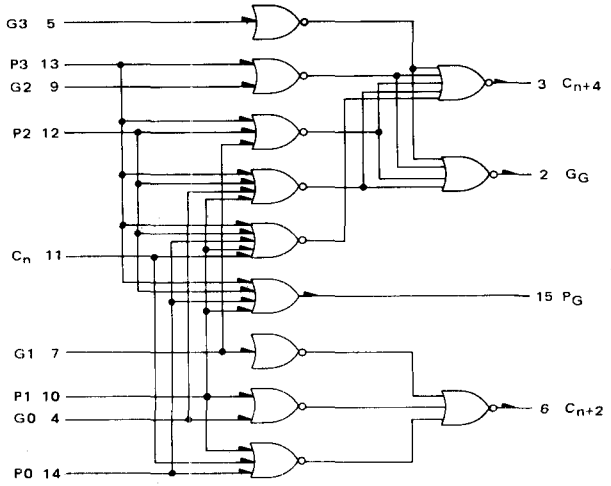
① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

*Load Power not included

2

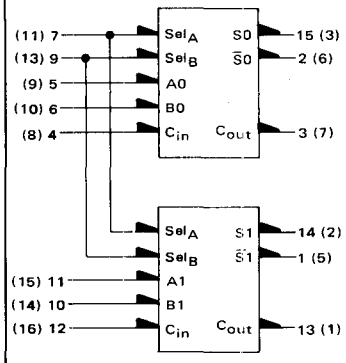
## ADDER AND ARITHMETIC FUNCTIONS

### MC10179
### Look-Ahead Carry Block




$P_D$ = 300 mW typ/pkg
$t_{pd}$ = 3.0 ns typ (Carry, Propagate)
4.0 ns typ (Generate)

### MC10180
### MC10580
### Dual High Speed Adder/Subtractor




$P_D$ = 360 mW typ/pkg

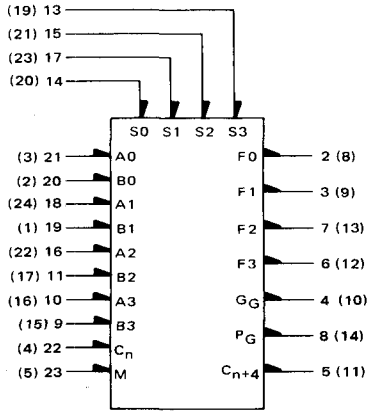
$t_{pd}$ (typ)
$C_{in}$ to $C_{out}$ = 2.2 ns
A0 to S0 = 4.5 ns
A0 to $C_{out}$ = 4.5 ns

Positive Logic Only
$A' = A \oplus Sel_A = A \odot \overline{Sel_A}$
$B' = B \oplus Sel_B = B \odot \overline{Sel_B}$

**FUNCTION SELECT TABLE**

| $Sel_A$ | $Sel_B$ | Function |
|---|---|---|
| H | H | S = A plus B |
| H | L | S = A minus B |
| L | H | S = B minus A |
| L | L | S = 0 minus A minus B |

### MC10181
### MC10581
### 4-Bit Arithmetic Logic Unit/Function Generator




$P_D$ = 600 mW typ/pkg (No Load)
$t_{pd}$ (typ): A1 to F = 6.5 ns
$C_n$ to $C_n$ + 4 = 3.1 ns
A1 to $P_G$ = 5.0 ns
A1 to $G_G$ = 4.5 ns
A1 to $C_{n+4}$ = 5.0 ns

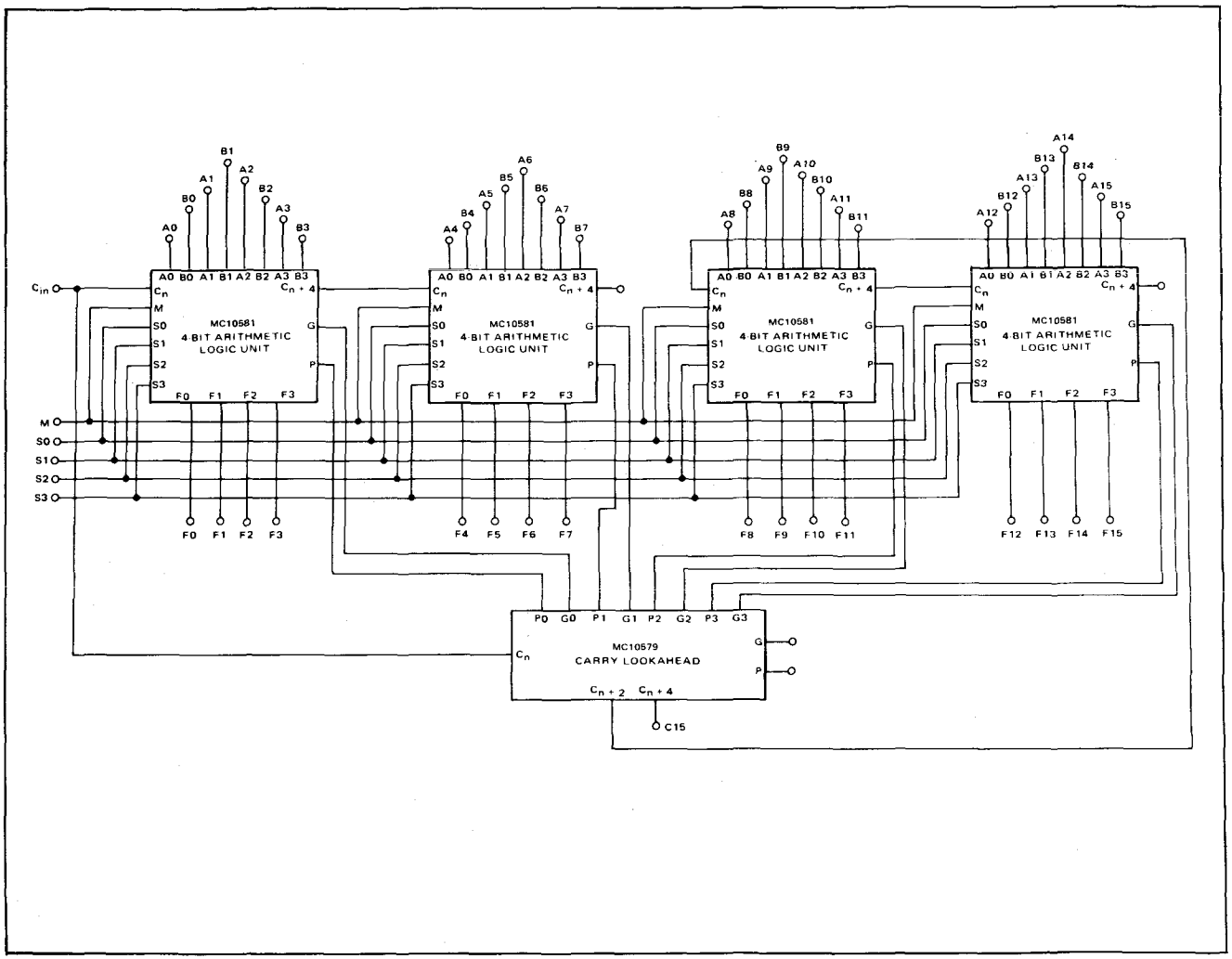



FIGURE 2 – 16-BIT FULL LOOK-AHEAD CARRY ARITHMETIC LOGIC UNIT

# MC10581

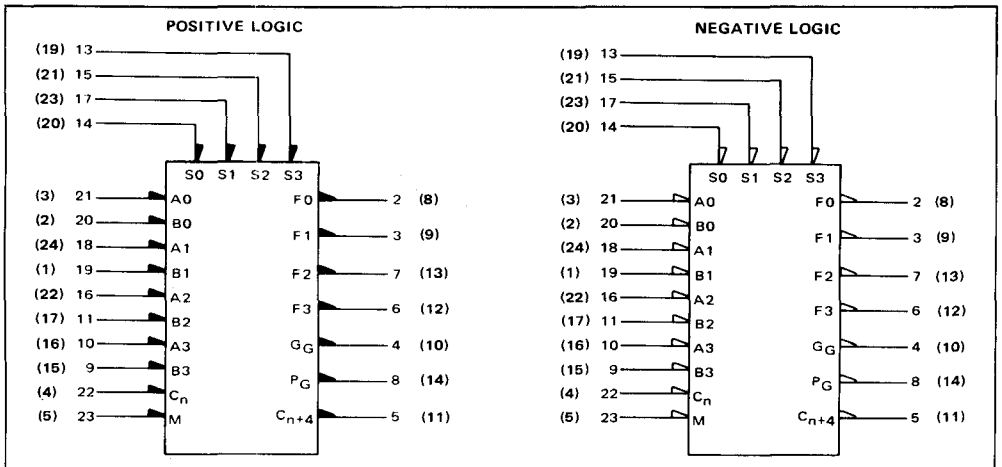
The MC10581 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions.

Group carry propagate ($P_G$) and carry generate ($G_G$) are provided to allow fast addition of very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10579, full-carry look-ahead, as a second order look ahead block, the MC10581 provides high speed arithmetic operations on very long words.






Numbers at end of terminals are pin numbers for L package (Case 620)
Numbers in parenthesis denotes pin numbers for F package (Case 650)

| Case | $V_{CC1}$ | $V_{CC2}$ | $V_{EE}$ |
|---|---|---|---|
| 623 | Pin 1 | Pin 24 | Pin 12 |
| 667 | Pin 7 | Pin 6 | Pin 18 |

$P_D$ = 600 mW typ/pkg (No Load)

$t_{pd}$ (typ): A1 to F = 6.5 ns
$C_n$ to $C_{n+4}$ = 3.1 ns
A1 to $P_G$ = 5.0 ns
A1 to $G_G$ = 4.5 ns
A1 to $C_{n+4}$ = 5.0 ns

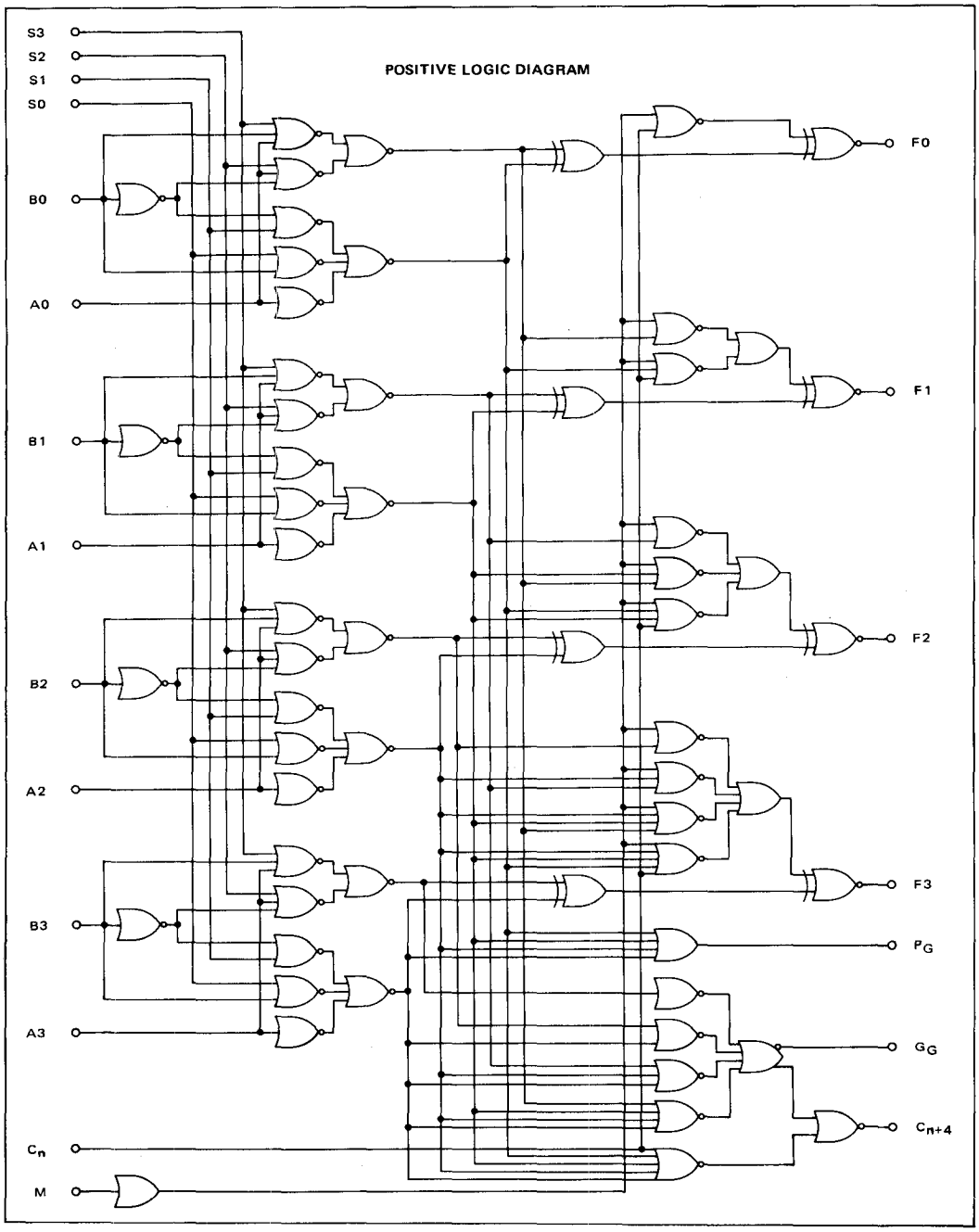
**POSITIVE LOGIC**

| Function Select S3 | S2 | S1 | S0 | Logic Functions M is High C = D.C. F | Arithmetic Operation M is Low $C_n$ is low F |
|---|---|---|---|---|---|
| L | L | L | L | $F = \overline{A}$ | F = A plus 0 |
| L | L | L | H | $F = \overline{A} + \overline{B}$ | F = A plus $(A \cdot \overline{B})$ |
| L | L | H | L | $F = \overline{A} + B$ | F = A plus $(A \cdot B)$ |
| L | L | H | H | F = Logical "1" | F = A times 2 |
| L | H | L | L | $F = \overline{A \cdot B}$ | F = (A + B) plus 0 |
| L | H | L | H | $F = \overline{B}$ | F = (A + B) plus $(A \cdot B)$ |
| L | H | H | L | $F = A \oplus B$ | F = A plus B |
| L | H | H | H | $F = A + \overline{B}$ | F = A plus (A + B) |
| H | L | L | L | $F = \overline{A} \cdot B$ | F = (A + $\overline{B}$) plus 0 |
| H | L | L | H | $F = A \odot B$ | F = A minus B minus 1 |
| H | L | H | L | $F = B$ | F = (A + $\overline{B}$) plus $(A \cdot B)$ |
| H | L | H | H | $F = A + B$ | F = A plus (A + $\overline{B}$) |
| H | H | L | L | F = Logical "0" | F = minus 1 (two's complement) |
| H | H | L | H | $F = A \cdot \overline{B}$ | F = (A • $\overline{B}$) minus 1 |
| H | H | H | L | $F = A \cdot B$ | F = (A • B) minus 1 |
| H | H | H | H | F = A | F = A minus 1 |

**NEGATIVE LOGIC**

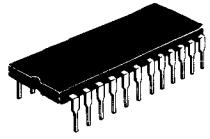
| Function Select S3 | S2 | S1 | S0 | Logic Functions M is High F | Arithmetic Operation M is Low $C_n$ of LSB must be High F |
|---|---|---|---|---|---|
| L | L | L | L | $F = \overline{A}$ | F = A minus 1 |
| L | L | L | H | $F = \overline{A + B}$ | F = A plus (A + $\overline{B}$) |
| L | L | H | L | $F = \overline{A} \cdot B$ | F = A plus (A + B) |
| L | L | H | H | F = Logical "0" | F = A times 2 |
| L | H | L | L | $F = \overline{A \cdot B}$ | F = (A • B) minus 1 |
| L | H | L | H | $F = \overline{B}$ | F = (A • B) plus (A + $\overline{B}$) |
| L | H | H | L | $F = A \oplus B$ | F = A plus B |
| L | H | H | H | $F = A \cdot \overline{B}$ | F = A plus (A • $\overline{B}$) |
| H | L | L | L | $F = \overline{A} + B$ | F = (A • $\overline{B}$) minus 1 |
| H | L | L | H | $F = A \odot B$ | F = A minus B minus 1 |
| H | L | H | L | $F = B$ | F = (A • $\overline{B}$) plus (A + B) |
| H | L | H | H | $F = A \cdot B$ | F = (A • $\overline{B}$) plus A |
| H | H | L | L | F = Logical "1" | F = minus 1 (two's complement) |
| H | H | L | H | $F = A + \overline{B}$ | F = (A + $\overline{B}$) plus 0 |
| H | H | H | L | $F = A + B$ | F = (A + B) plus 0 |
| H | H | H | H | F = A | F = A plus 0 |

See General Information section for packaging and maximum ratings.


POSITIVE LOGIC DIAGRAM
S3
S2
S1
S0
B0
A0
B1
A1
B2
A2
B3
A3
Cn
M
F0
F1
F2
F3
PG
GG
Cn+4

## ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.



**L SUFFIX**
CERAMIC PACKAGE
CASE 623

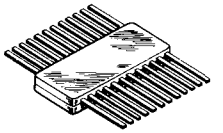
| @ Test Temperature | TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$ | $V_{IL\ min}$ | $V_{IHA\ min}$ | $V_{ILA\ max}$ | $V_{EE}$ |
|---|---|---|---|---|---|
| -55°C | -0.880 | -1.920 | -1.255 | -1.510 | -5.2 |
| +25°C | -0.780 | -1.850 | -1.105 | -1.475 | -5.2 |
| +125°C | -0.630 | -1.820 | -1.000 | -1.400 | -5.2 |

| Characteristic | Symbol | Pin Under Test | MC10581L Test Limits -55°C Min | -55°C Max | +25°C Min | +25°C Typ | +25°C Max | +125°C Min | +125°C Max | Unit | TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$ | $V_{IL\ min}$ | $V_{IHA\ min}$ | $V_{ILA\ max}$ | $V_{EE}$ | ($V_{CC}$) Gnd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power Supply Drain Current | $I_E$ | 12 | – | 160 | – | – | 145 | – | 160 | mAdc | – | – | – | – | 12 | 1,24 |
| Input Current | $I_{inH}$ | 9 | – | 420 | – | – | 245 | – | 245 | µAdc | 9 | – | – | – | 12 | 1,24 |
| | | 10 | – | 375 | – | – | 220 | – | 220 | | 10 | – | – | – | | |
| | | 11 | – | 420 | – | – | 245 | – | 245 | | 11 | – | – | – | | |
| | | 13 | – | 340 | – | – | 200 | – | 200 | | 13 | – | – | – | | |
| | | 14 | – | 450 | – | – | 265 | – | 265 | | 14 | – | – | – | | |
| | | 15 | – | 450 | – | – | 265 | – | 265 | | 15 | – | – | – | | |
| | | 16 | – | 375 | – | – | 220 | – | 220 | | 16 | – | – | – | | |
| | | 17 | – | 450 | – | – | 265 | – | 265 | | 17 | – | – | – | | |
| | | 18 | – | 375 | – | – | 220 | – | 220 | | 18 | – | – | – | | |
| | | 19 | – | 420 | – | – | 245 | – | 245 | | 19 | – | – | – | | |
| | | 20 | – | 420 | – | – | 245 | – | 245 | | 20 | – | – | – | | |
| | | 21 | – | 375 | – | – | 220 | – | 220 | | 21 | – | – | – | | |
| | | 22 | – | 495 | – | – | 290 | – | 290 | | 22 | – | – | – | | |
| | | 23 | – | 340 | – | – | 200 | – | 200 | | 23 | – | – | – | | |
| Input Leakage Current | $I_{inL}$ | 9 | 0.5 | – | 0.5 | – | – | 0.3 | – | µAdc | – | 9 | – | – | 12 | 1,24 |
| | | 10 | | – | | – | – | | – | | – | 10 | – | – | | |
| | | 11 | | – | | – | – | | – | | – | 11 | – | – | | |
| | | 13 | | – | | – | – | | – | | – | 13 | – | – | | |
| | | 14 | | – | | – | – | | – | | – | 14 | – | – | | |
| | | 15 | | – | | – | – | | – | | – | 15 | – | – | | |
| | | 16 | | – | | – | – | | – | | – | 16 | – | – | | |
| | | 17 | | – | | – | – | | – | | – | 17 | – | – | | |
| | | 18 | | – | | – | – | | – | | – | 18 | – | – | | |
| | | 19 | | – | | – | – | | – | | – | 19 | – | – | | |
| | | 20 | | – | | – | – | | – | | – | 20 | – | – | | |
| | | 21 | | – | | – | – | | – | | – | 21 | – | – | | |
| | | 22 | | – | | – | – | | – | | – | 22 | – | – | | |
| | | 23 | | – | | – | – | | – | | – | 23 | – | – | | |
| High Output Voltage | $V_{OH}$ | * | -1.080 | -0.880 | -0.930 | – | -0.780 | -0.825 | -0.630 | Vdc | * | * | – | – | 12 | 1,24 |
| Low Output Voltage | $V_{OL}$ | * | -1.920 | -1.655 | -1.850 | – | -1.620 | -1.820 | -1.545 | Vdc | * | * | – | – | 12 | 1,24 |
| High Threshold Voltage | $V_{OHA}$ | * | -1.100 | – | -0.950 | – | – | -0.845 | – | Vdc | – | – | ** | ** | 12 | 1,24 |
| Low Threshold Voltage | $V_{OLA}$ | * | – | -1.635 | – | – | -1.600 | – | -1.525 | Vdc | – | – | ** | ** | 12 | 1,24 |

*Test all input-output combinations according to Function Table.
**For threshold level test, apply threshold input level to only one input pin at a time.

## ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts.



**F SUFFIX**
CERAMIC PACKAGE
CASE 652

| @ Test Temperature | TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$ | $V_{IL\ min}$ | $V_{IHA\ min}$ | $V_{ILA\ max}$ | $V_{EE}$ |
|---|---|---|---|---|---|
| -55°C | -0.880 | -1.920 | -1.255 | -1.510 | -5.2 |
| +25°C | -0.780 | -1.850 | -1.105 | -1.475 | -5.2 |
| +125°C | -0.630 | -1.820 | -1.000 | -1.400 | -5.2 |

| Characteristic | Symbol | Pin Under Test | MC10581F Test Limits -55°C Min | -55°C Max | +25°C Min | +25°C Typ | +25°C Max | +125°C Min | +125°C Max | Unit | TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$ | $V_{IL\ min}$ | $V_{IHA\ min}$ | $V_{ILA\ max}$ | $V_{EE}$ | ($V_{CC}$) Gnd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power Supply Drain Current | $I_E$ | 18 | – | 160 | – | 116 | 145 | – | 160 | mAdc | – | – | – | – | 18 | 6,7 |
| Input Current | $I_{inH}$ | 15 | – | 420 | – | – | 245 | – | 245 | µAdc | 15 | – | – | – | 18 | 6,7 |
| | | 16 | – | 375 | – | – | 220 | – | 220 | | 16 | – | – | – | | |
| | | 17 | – | 420 | – | – | 245 | – | 245 | | 17 | – | – | – | | |
| | | 19 | – | 340 | – | – | 200 | – | 200 | | 19 | – | – | – | | |
| | | 20 | – | 450 | – | – | 265 | – | 265 | | 20 | – | – | – | | |
| | | 21 | – | 450 | – | – | 265 | – | 265 | | 21 | – | – | – | | |
| | | 22 | – | 375 | – | – | 220 | – | 220 | | 22 | – | – | – | | |
| | | 23 | – | 450 | – | – | 265 | – | 265 | | 23 | – | – | – | | |
| | | 24 | – | 375 | – | – | 220 | – | 220 | | 24 | – | – | – | | |
| | | 1 | – | 420 | – | – | 245 | – | 245 | | 1 | – | – | – | | |
| | | 2 | – | 420 | – | – | 245 | – | 245 | | 2 | – | – | – | | |
| | | 3 | – | 375 | – | – | 220 | – | 220 | | 3 | – | – | – | | |
| | | 4 | – | 495 | – | – | 290 | – | 290 | | 4 | – | – | – | | |
| | | 5 | – | 340 | – | – | 200 | – | 200 | | 5 | – | – | – | | |
| Input Leakage Current | $I_{inL}$ | 15 | 0.5 | – | 0.5 | – | – | 0.3 | – | µAdc | – | 15 | – | – | 18 | 6,7 |
| | | 16 | | – | | – | – | | – | | – | 16 | – | – | | |
| | | 17 | | – | | – | – | | – | | – | 17 | – | – | | |
| | | 19 | | – | | – | – | | – | | – | 19 | – | – | | |
| | | 20 | | – | | – | – | | – | | – | 20 | – | – | | |
| | | 21 | | – | | – | – | | – | | – | 21 | – | – | | |
| | | 22 | | – | | – | – | | – | | – | 22 | – | – | | |
| | | 23 | | – | | – | – | | – | | – | 23 | – | – | | |
| | | 24 | | – | | – | – | | – | | – | 24 | – | – | | |
| | | 1 | | – | | – | – | | – | | – | 1 | – | – | | |
| | | 2 | | – | | – | – | | – | | – | 2 | – | – | | |
| | | 3 | | – | | – | – | | – | | – | 3 | – | – | | |
| | | 4 | | – | | – | – | | – | | – | 4 | – | – | | |
| | | 5 | | – | | – | – | | – | | – | 5 | – | – | | |
| High Output Voltage | $V_{OH}$ | * | -1.080 | -0.880 | -0.930 | – | -0.780 | -0.825 | -0.630 | Vdc | * | * | – | – | 18 | 6,7 |
| Low Output Voltage | $V_{OL}$ | * | -1.920 | -1.655 | -1.850 | – | -1.620 | -1.820 | -1.545 | Vdc | * | * | – | – | 18 | 6,7 |
| High Threshold Voltage | $V_{OHA}$ | * | -1.100 | – | -0.950 | – | – | -0.845 | – | Vdc | – | – | ** | ** | 18 | 6,7 |
| Low Threshold Voltage | $V_{OLA}$ | * | – | -1.635 | – | – | -1.600 | – | -1.525 | Vdc | – | – | ** | ** | 18 | 6,7 |

*Test all input-output combinations according to Function Table.
**For threshold level test, apply threshold input level to only one input pin at a time.

3

## ELECTRICAL CHARACTERISTICS (CONT')

| Characteristic | Symbol | Input | Output | Conditions† | AC Switching Characteristics | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | -55°C * | | +25°C | | | +125°C * | | |
| | | | | | Min | Max | Min | Typ | Max | Min | Max | Unit |
| Propagation Delay | t++, t-- | B1 | $P_G$ | S0, S3 | 1.8 | 7.6 | 2.0 | 6.0 | 7.5 | 1.6 | 7.6 | ns |
| Rise Time, Fall Time | t+, t- | B1 | $P_G$ | S0,S3 | 1.0 | 3.5 | 1.1 | 2.0 | 3.5 | 0.9 | 3.5 | ns |
| Propagation Delay | t++, t-- | B1 | $G_G$ | S3, $C_n$ | 1.9 | 8.1 | 2.0 | 6.0 | 8.0 | 2.0 | 8.1 | ns |
| Rise Time, Fall Time | t+, t- | B1 | $G_G$ | S3,$C_n$ | 1.3 | 5.0 | 1.5 | 3.0 | 5.0 | 1.3 | 5.0 | ns |
| Propagation Delay | t+-, t-+ | B1 | $C_{n+4}$ | S3, $C_n$ | 1.9 | 8.1 | 2.0 | 6.0 | 8.0 | 1.9 | 8.1 | ns |
| Rise Time, Fall Time | t+, t- | B1 | $C_{n+4}$ | S3,$C_n$ | 0.9 | 3.0 | 1.0 | 2.0 | 3.0 | 0.9 | 3.0 | ns |
| Propagation Delay | t++, t+- | M | F1 | – | 2.8 | 10.3 | 3.0 | 6.5 | 10 | 2.8 | 10.2 | ns |
| Rise Time, Fall Time | t+, t- | M | F1 | – | 1.3 | 5.2 | 1.5 | 4.0 | 5.0 | 1.3 | 5.2 | ns |
| Propagation Delay | t+-, t-+ | S1 | F1 | A1, B1 | 2.7 | 10.2 | 3.0 | 6.5 | 10 | 2.6 | 10.2 | ns |
| Rise Time, Fall Time | t+, t- | S1 | F1 | A1, B1 | 1.3 | 5.2 | 1.5 | 3.0 | 5.0 | 1.3 | 5.2 | ns |
| Propagation Delay | t-+, t+- | S1 | $P_G$ | A3, B3 | 1.9 | 8.1 | 2.0 | 6.0 | 8.0 | 1.8 | 8.1 | ns |
| Rise Time, Fall Time | t+, t- | S1 | $P_G$ | A3, B3 | 1.0 | 5.1 | 1.1 | 3.0 | 5.0 | 1.0 | 5.1 | ns |
| Propagation Delay | t+-, t-+ | S1 | $C_{n+4}$ | A3, B3 | 1.9 | 9.1 | 2.0 | 6.0 | 9.0 | 1.8 | 9.1 | ns |
| Rise Time, Fall Time | t+, t- | S1 | $C_{n+4}$ | A3, B3 | 1.0 | 5.1 | 1.1 | 3.0 | 5.0 | 1.0 | 5.1 | ns |
| Propagation Delay | t+-, t-+ | S1 | $G_G$ | A3, B3 | 1.7 | 9.2 | 2.0 | 6.0 | 9.0 | 1.7 | 9.1 | ns |
| Rise Time, Fall Time | t+, t- | S1 | $G_G$ | A3, B3 | 0.8 | 6.2 | 0.8 | 3.0 | 6.0 | 0.8 | 6.2 | ns |
| Propagation Delay | t++, t-- | $C_n$ | $C_{n+4}$ | A0,A1,A2,A3 | 1.0 | 5.1 | 1.1 | 3.1 | 5.0 | 0.9 | 5.1 | ns |
| Rise Time, Fall Time | t+,t- | $C_n$ | $C_{n+4}$ | A0,A1,A2,A3 | 0.9 | 3.1 | 1.0 | 2.0 | 3.0 | 0.3 | 3.1 | ns |
| Propagation Delay | t++, t+- | $C_n$ | F1 | A0 | 1.9 | 7.1 | 2.0 | 4.5 | 7.0 | 2.0 | 7.1 | ns |
| | t-+, t-- | ↓ | ↓ | ↓ | 1.9 | 7.1 | 2.0 | 4.5 | 7.0 | 2.0 | 7.1 | ↓ |
| Rise Time, Fall Time | t+, t- | ↓ | ↓ | ↓ | 1.3 | 5.2 | 1.5 | 3.0 | 5.0 | 1.3 | 5.2 | ↓ |
| Propagation Delay | t++, t+- | A1 | F1 | – | 2.9 | 10.1 | 3.0 | 6.5 | 10 | 2.8 | 10.2 | ns |
| | t-+, t- - | ↓ | ↓ | | 2.9 | 10.1 | 3.0 | 6.5 | 10 | 2.8 | 10.2 | ↓ |
| Rise Time, Fall Time | t+, t- | ↓ | ↓ | – | 1.3 | 5.2 | 1.5 | 3.0 | 5.0 | 1.3 | 5.2 | ↓ |
| Propagation Delay | t++, t-- | A1 | $P_G$ | S0,S3 | 1.8 | 6.6 | 2.0 | 5.0 | 6.5 | 1.8 | 6.5 | ns |
| Rise Time, Fall Time | t+, t- | A1 | $P_G$ | S0,S3 | 0.9 | 3.5 | 1.1 | 2.0 | 3.5 | 1.0 | 3.6 | ns |
| Propagation Delay | t++, t-- | A1 | $G_G$ | A0,A2,A3,$C_n$ | 1.9 | 7.1 | 2.0 | 4.5 | 7.0 | 2.0 | 7.1 | ns |
| Rise Time, Fall Time | t+, t- | A1 | $G_G$ | A0,A2,A3,$C_n$ | 1.3 | 5.2 | 1.5 | 4.0 | 5.0 | 1.3 | 5.2 | ns |
| Propagation Delay | t+-, t-+ | A1 | $C_{n+4}$ | A0,A2,A3,$C_n$ | 2.0 | 7.1 | 2.0 | 5.0 | 7.0 | 1.9 | 7.1 | ns |
| Rise Time, Fall Time | t+, t- | A1 | $C_{n+4}$ | A0,A2,A3,$C_n$ | 0.9 | 3.0 | 1.0 | 2.0 | 3.0 | 0.9 | 3.1 | ns |
| Propagation Delay | t++, t-+ | B1 | F1 | S3, $C_n$ | 2.9 | 11.1 | 3.0 | 8.0 | 11 | 2.7 | 11.2 | ns |
| Rise Time, Fall Time | t+, t- | B1 | F1 | S3,$C_n$ | 1.3 | 5.2 | 1.5 | 3.5 | 5.0 | 1.3 | 5.2 | ns |

†Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
$V_{CC1} = V_{CC2} = +2.0$ Vdc, $V_{EE} = -3.2$ Vdc

*For L Suffix only.

## SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C