



HIGH SPEED DUAL CHANNEL OPTICALLY COUPLED ISOLATOR PHOTOTRANSISTOR OUTPUT

APPROVALS

- UL recognised, File No. E91231

DESCRIPTION

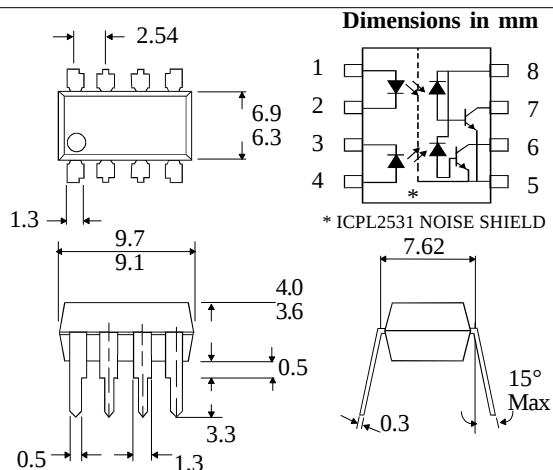
These dual channel diode-transistor optocouplers use a light emitting diode and an integrated photon detector to provide 2500Volts_{RMS} electrical isolation between input and output. Separate connection for the photodiode bias and output transistor collector improve the speed up to a hundred times that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

FEATURES

- High speed - 1 MBits/s
- High Common Mode Transient Immunity 1000V/ μ s
- TTL Compatible
- 3 MHz Bandwidth
- Open Collector Outputs
- 2500V_{RMS} Withstand Test Voltage, 1 Min
- ICPL2531 has improved noise shield which gives superior common mode rejection
- Options :-
10mm lead spread - add G after part no.
Surface mount - add SM after part no.
Tape&reel - add SMT&R after part no.
- All electrical parameters 100% tested
- Custom electrical selections available

APPLICATIONS

- Line receivers
- Pulse transformer replacement
- Wide bandwidth analog coupling
- Output interface to CMOS-LSTTL-TTL



ABSOLUTE MAXIMUM RATINGS (25°C unless otherwise specified)

Storage Temperature _____ -55°C to + 125°C
Operating Temperature _____ -55°C to + 100°C
Lead Soldering Temperature
(1/16 inch (1.6mm) from case for 10 secs) 260°C

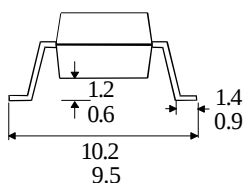
INPUT DIODE

Average Forward Current _____ 25mA (1)
Peak Forward Current _____ 50mA (2)
(50% duty cycle, 1ms pulse width)
Peak Transient Current _____ 1.0A
(equal to or less than 1 μ s P.W., 300 pps)
Reverse Voltage _____ 5V
Power Dissipation _____ 45mW (3)

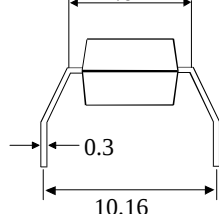
DETECTOR

Average Output Current _____ 8mA
Peak Output Current _____ 16mA
Supply Voltage _____ -0.5 to +30V
Output Voltage _____ -0.5 to +20V
Power Dissipation _____ 35mW (4)

OPTION SM SURFACE MOUNT



OPTION G



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ELECTRICAL CHARACTERISTICS ($T_A = 0^{\circ}\text{C}$ to 70°C Unless otherwise noted)

PARAMETER	SYM	DEVICE	MIN	TYP*	MAX	UNITS	TEST CONDITION
Current Transfer Ratio (note 5,6)	CTR	ICPL2530	7	18		%	$I_F = 16\text{mA}$, $V_O = 0.5\text{V}$ $V_{CC} = 4.5\text{V}$, $T_A = 25^{\circ}\text{C}$
		ICPL2531	19			%	
Logic Low Output Voltage (note 5)	V_{OL}	ICPL2530	5	13		%	$I_F = 16\text{mA}$, $V_O = 0.5\text{V}$ $V_{CC} = 4.5\text{V}$
		ICPL2531	15			%	
Logic High Output Current (note 5)	I_{OH}	ICPL2530		0.1	0.5	V	$I_F = 16\text{mA}$, $I_O = 1.1\text{mA}$ $V_{CC} = 4.5\text{V}$, $T_A = 25^{\circ}\text{C}$
		ICPL2531		0.1	0.5	V	
Logic Low Supply Current	I_{CCL}			0.02	500	nA	$I_{F1} = I_{F2} = 0\text{mA}$, $T_A = 25^{\circ}\text{C}$ $V_{O1} = V_{O2} = V_{CC} = 5.5\text{V}$ $I_{F1} = I_{F2} = 0\text{mA}$ $V_{O1} = V_{O2} = V_{CC} = 15\text{V}$
				0.01	10	μA	
Logic High Supply Current	I_{CCH}			80		μA	$I_{F1} = I_{F2} = 16\text{mA}$, $V_{CC} = 15\text{V}$ $V_{O1} = V_{O2} = \text{open}$
Input Forward Voltage (note 5)	V_F			0.01	4	μA	$I_{F1} = I_{F2} = 0\text{mA}$, $V_{CC} = 15\text{V}$ $V_{O1} = V_{O2} = \text{open}$
Temperature Coefficient of Forward Voltage (note 5)	$\frac{\Delta V_F}{\Delta T_A}$			1.5	1.7	V	$I_F = 16\text{mA}$, $T_A = 25^{\circ}\text{C}$
Input Reverse Voltage (note 5)	V_R		5			V	$I_F = 16\text{mA}$
Input Capacitance (note 5)	C_{IN}			60		pF	$I_R = 10\mu\text{A}$, $T_A = 25^{\circ}\text{C}$
Input-output Isolation Voltage (note 7)	V_{ISO}		2500	5000		V_{RMS}	$f = 1\text{MHz}$, $V_F = 0$
Resistance (Input to Output) (note 7)	R_{IO}			10^{12}		Ω	R.H.equal to or less than 50%, $t = 1\text{min}$. $T_A = 25^{\circ}\text{C}$
Capacitance (Input to Output) (note 7)	C_{IO}			0.6		pF	$V_{IO} = 500\text{V dc}$
Input-Input Insulation Leakage Current (note 8)	I_{I-I}			0.005		μA	$f = 1\text{MHz}$
Resistance (Input to Input)(note8)	R_{I-I}			10^{11}		Ω	45 % Relative Humidity $t = 5\text{s}$, $V_{I-I} = 500\text{V dc}$
Capacitance (Input to Input)(note8)	C_{I-I}			0.25		pF	$V_{I-I} = 500\text{V dc}$

* All typicals at $T_A = 25^{\circ}\text{C}$

SWITCHING SPECIFICATIONS AT $T_A = 25^\circ\text{C}$ ($V_{CC} = 5\text{V}$, $I_F = 16\text{mA}$ Unless otherwise noted)

PARAMETER	SYM	DEVICE	MIN	TYP	MAX	UNITS	TEST CONDITION
Propagation Delay Time to Logic Low at Output (fig 1)	t_{PHL}	ICPL2530 ICPL2531		0.5 0.2	1.5 0.8	μs μs	$R_L = 4.1\text{k}\Omega$, (note11) $R_L = 1.9\text{k}\Omega$, (note10)
Propagation Delay Time to Logic High at Output (fig 1)	t_{PLH}	ICPL2530 ICPL2531		0.5 0.2	1.5 0.8	μs μs	$R_L = 4.1\text{k}\Omega$, (note11) $R_L = 1.9\text{k}\Omega$, (note10)
Common Mode Transient Immunity at Logic High Level Output (fig 2)	CM_H	ICPL2530		1000		$\text{V}/\mu\text{s}$	$I_F = 0\text{mA}$, $V_{CM} = 10V_{PP}$ $R_L = 4.1\text{k}\Omega$, (note9,11)
		ICPL2531		1000		$\text{V}/\mu\text{s}$	$I_F = 0\text{mA}$, $V_{CM} = 10V_{PP}$ $R_L = 1.9\text{k}\Omega$, (note9,10)
Common Mode Transient Immunity at Logic Low Level Output (fig 2)	CM_L	ICPL2530		-1000		$\text{V}/\mu\text{s}$	$V_{CM} = 10V_{PP}$ $R_L = 4.1\text{k}\Omega$, (note9,11)
		ICPL2531		-1000		$\text{V}/\mu\text{s}$	$V_{CM} = 10V_{PP}$ $R_L = 1.9\text{k}\Omega$, (note9,10)
Bandwidth	BW			3		MHz	$R_L = 100\Omega$, (note 12)

NOTES:-

1. Derate linearly above 70°C free air temperature at a rate of $0.8 \text{ mA}/^\circ\text{C}$.
2. Derate linearly above 70°C free air temperature at a rate of $1.6 \text{ mA}/^\circ\text{C}$.
3. Derate linearly above 70°C free air temperature at a rate of $0.9 \text{ mW}/^\circ\text{C}$.
4. Derate linearly above 70°C free air temperature at a rate of $1.0 \text{ mW}/^\circ\text{C}$.
5. Each channel.
6. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F times 100%.
7. Device considered a two-terminal device: pins 1,2,3, and 4 shorted together and pins 5,6,7 and 8 shorted together.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM} to assure that the output will remain in a Logic High state (i.e. $V_O > 2.0\text{V}$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} to assure that the output will remain in Logic Low state (i.e. $V_O < 0.8\text{V}$).
10. The $1.9\text{k}\Omega$ load represents 1 TTL unit load of 1.6mA and the $5.6\text{k}\Omega$ pull-up resistor.
11. The $4.1\text{k}\Omega$ load represents 1 LSTTL unit load of 0.36mA and the $6.1\text{k}\Omega$ pull-up resistor.
12. The frequency at which the a.c. output voltage is 3dB below the low frequency asymptote.

FIG.1 SWITCHING TEST CIRCUIT

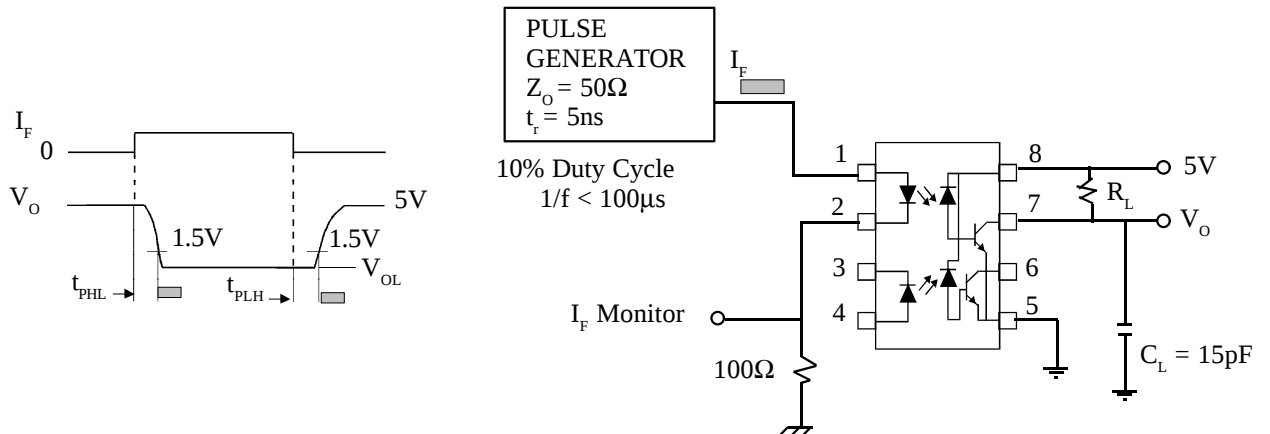


FIG. 2 TEST CIRCUIT FOR TRANSIENT IMMUNITY AND TYPICAL WAVEFORMS

